Design Example Report

Title	***13 W Triple Output Automotive Inverter Power Supply Using InnoSwitch™3-AQ INN3996CQ***
Specification	40 VDC – 530 VDC Input; 7.5 V 1.3 A, 17 V 0.14 A, -4 V 0.14 A Outputs
Application	Traction Inverter Power supply
Author	Applications Engineering Department
Document Number	DER-926Q
Date	March 10, 2022
Revision	1.1

Summary and Features

- 13 W output from 40 VDC to 530 VDC
- Startup from 40 V with no additional parts
- Built in synchronous rectification drive delivers >82% efficiency at 13 W and flat efficiency curve delivers >75% at 3 W load
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a triple output embedded power supply utilizing INN3996CQ from the InnoSwitch™3-AQ family of ICs. It contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

Figure 1 – Populated Circuit Board Photograph (88 mm x 43 mm), Top.

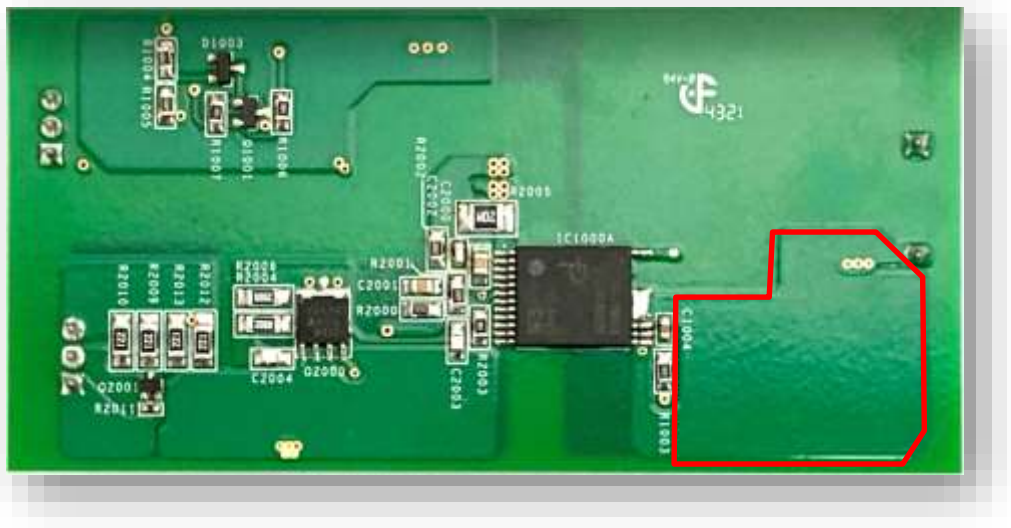


Figure 2 – Populated Circuit Board Photograph, Bottom with PCB heatsink area highlighted

The power supply is targeted for 400 V automotive traction inverter applications as shown in figure 3.

The HVDC input referenced 17 V and -4 V outputs provide the gate power for the low side devices. These voltages were selected for driving the current generation of SiC MOSFETs.

The 7.5 V isolated output provides the backup source to maintain inverter operation on failure of the 12 V system, a functional safety requirement.

By providing the low side gate voltages directy eliminates another conversion stage, saving space and cost.

InnoSwitch3-AQ is able to provide the necessary regulation because it directly senses and regulates the output voltage, with communication to the primary side provided via FluxLink. Secondary-side control also enables the use of synchronous rectification increasing efficiency >10% vs diode rectification, saving cost and space by eliminating heat sinking.

The design provides basic isolation from the HVDC input to the isolated 7.5 V output. The InnoSwitch3-AQ IC meets the requirements for reinforced isolation so a reinforced isolation solution can be achieved with a wider spacing transformer and associated PCB creepage distances.

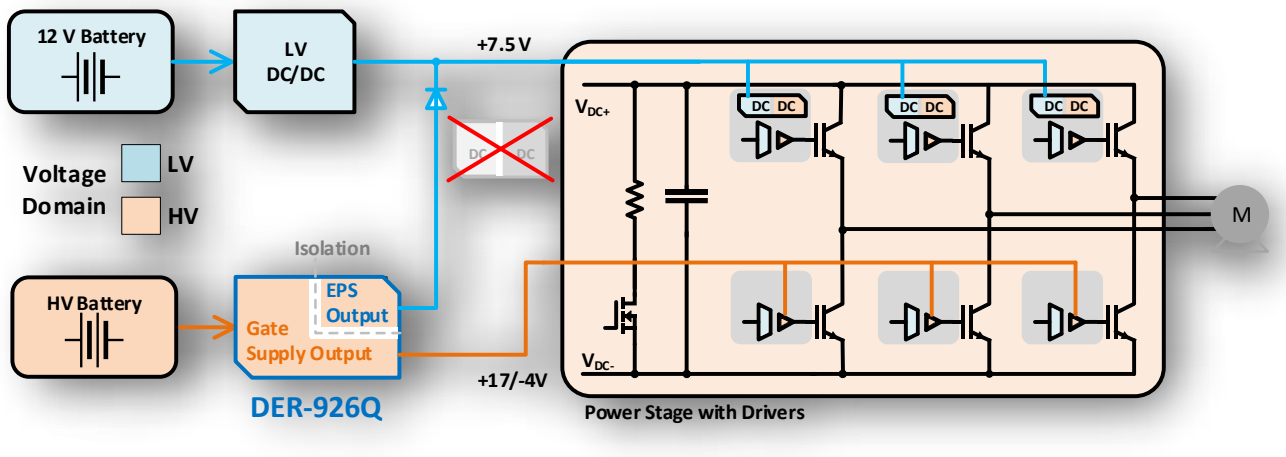


Figure 3 – Inverter Power Architecture Example using DER-926Q.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	40	375	530	VDC	
Isolated Output						
Output Voltage 1	V_{OUT1}	6.53	7.5	8.03	V	+7 / -13 %
Output Ripple Voltage	V_{RIPPLE}			500	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0.065	1.13	1.3	A	
Non-Isolated Outputs						
Output Voltage 2	V_{OUT2}	15.47	17	20.74	V	+22 / -9 %
Output Ripple Voltage	V_{RIPPLE}			150	mV	20 MHz Bandwidth.
Output Current 2	I_{OUT2}	20	120	140	mA	
Output Voltage 3	V_{OUT3}	-3.72	-4	-4.28	V	±7 %
Output Ripple Voltage	V_{RIPPLE}			50	mV	20 MHz Bandwidth.
Output Current 3	I_{OUT3}	20	120	140	mA	
Efficiency	η	75			%	Input Voltage: Nominal (375 VDC) Load Condition: 5
			85			Load Condition: 4
Environmental						
Ambient Temperature	T_{AMB}	-40		85	°C	Free Convection, Sea Level.
Isolation	$V_{ISO(P-S)}$	3000			VAC	V_{IN}, $V_{OUT2,3} \leftrightarrow V_{OUT1}$

Loading Conditions	7.5 V Load Current (A)	17 V Load Current (mA)	-4 V Load Current (mA)
1	0.065	20	20
2	1.3	140	140
3	1.13	20	20
4	1.13	120	120
5	0.065	120	120

3 Schematic

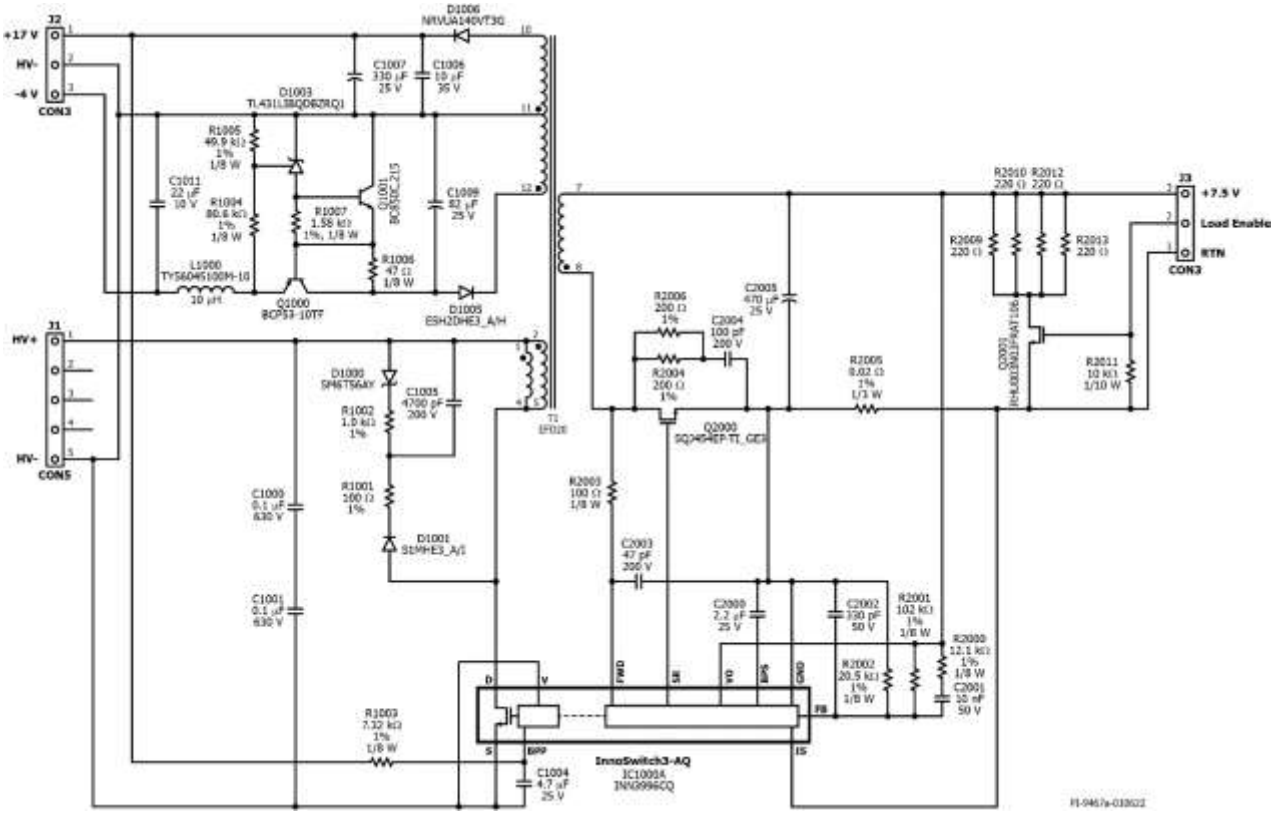


Figure 4 – Schematic.

4 Circuit Description

The InnoSwitch3-AQ IC combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates the primary MOSFET, the primary-side controller, the secondary-side controller for synchronous rectification and Fluxlink™ technology that eliminates the optocoupler needed for secondary sensed feedback. The elimination of the optocoupler but retaining direct sensing of the output gives excellent load, line and transient performance.

4.1 *Input Filtering*

DER-926Q is a HVDC to LVDC triple output flyback power supply designed for integration into the tranction inverter of a PHEV or BEV vehicle.

Due to the high transient currents during inverter operation the HV+ input can have significant high frequency voltage variations. These are reduced via filtering by C1000 and C1001 which also act as local decoupling for primary switching current. Two series capacitors are used to prevent shorting of the input DC in the event one of the two capacitors fails but also increase the effective creepage distance between HV+ and HV-. These are specific considerations due to the high fault energy available from the vehicle battery.

4.2 *Primary-Side Circuit*

The primary winding of T1 (pins 1, 2) is connected to HV+, while the other (pins 4, 5) is connected to the drain terminal of integrated 900 V power MOSFET inside the INN3996CQ (IC1000A).

Primary clamp circuit formed by diode D1001, resistors R1001 and R1002, capacitor C1005, and TVS diode D1000 limits the peak drain voltage of the InnoSwitch IC at the turn-off of the internal power MOSFET due to the leakage inductance energy of the transformer. This energy is dissipated by D1000 and R1002.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C1004, when DC input voltage is first applied. The part is guaranteed to start-up from 30 V but typically will start below this level.

During normal operation the primary-side block is powered from the 17 V non-isolated output. This output is configured as a flyback winding, which is rectified and filtered using diode D1006 and capacitors C1006 and C1007, and the current fed into the BPP pin via a current limiting resistor R1003. The 17 V output is designed as the positive supply for the main gate driver.

An additional -4 V non-isolated output is designed as the negative supply for the main gate driver (SiC MOSFET). This is configured as a flyback winding which is rectified and filtered using diode D1005 and C1009. To achieve tight regulation, a linear regulator was

connected after C1009. The linear regulator circuit comprises resistors R1004, R1005, R1006 and R1007, transistors Q1001 and Q1000, and a shunt regulator D1003. Additional output LC filter L1000 and C1011 is connected after linear regulator to further reduce high frequency ripple voltage. High accuracy is required due to the narrow acceptable range for the negative gate voltage on SiC MOSFETs.

In this design the input primary under and overvoltage features were disabled by connecting the V pin to source. This saves the voltage sensing resistor chain required, saving cost and space. However with no UV feature the output may fail to reach regulation at voltages <40 V, causing the outputs to rise but fail to reach regulation. The timing is determined by the auto-restart feature, giving a 50 ms start-up attempt followed by a 2s off time.

If this is not acceptable at a system level (there is no increased stress on the power supply) then the UV feature can be implemented. Please refer to the data sheet for the recommended circuits.

4.3 *Secondary-Side Circuit*

The secondary-side of the IC provides output voltage, output current sensing and gate drive for the MOSFET providing synchronous rectification (SR). Secondary winding of the transformer is rectified by MOSFET Q2000 and filtered by capacitors C2005. RC snubber R2004, R2006, and C2004 connected to MOSFET helps to reduce high frequency ringing during switching transients.

The gate of Q2000 is turned on by the secondary-side controller inside InnoSwitch IC, based on the winding voltage sensed via resistor R2003 and fed into the FWD pin of the IC. Capacitor C2003 reduces voltage spike on the FWD pin to meet derating to the 150 V rating.

In continuous conduction mode operation, the primary-side power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the SR MOSFET is turned off when the voltage drop across it falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on during the synchronous rectification MOSFET on time. This secondary-side based control avoids all of the issue normall associated with SR, especially during fault conditions. The SR MOSFET drive signal is the output on the SR pin.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage (FWD pin) when VO is below VBPS or the output voltage (VO pin) when above VBPS. In both cases energy is used to charge the decoupling capacitor C2000 via an internal regulator.

Resistors R2001 and R2002 form a voltage divider network that senses the output voltage. The INN3996CQ IC has a FB pin internal reference of 1.265 V. Capacitor C2002 provides

decoupling from high frequency noise affecting power supply operation, and C2001 and R2000 is a feedforward network to speed up the response time and lower the output ripple.

The output current is sensed by R2005 with a threshold of approximately 35 mV to reduce losses. Once the output current limit threshold is exceeded, the device will enter into the auto-restart feature until the load current is reduced below the threshold.

Optional active load components R2009, R2010, R2011, R20212, R2013, and Q2001 are placed in the output section as part of the inverter built in self-test. This allows the system controller to load the power supply and definitively determine the supply is operating even when diode-OR connected to the second 7.5 V output derived from the 12 V vehicle supply.

5 PCB Layout

PCB Material FR4 copper 2oz with thickness of 0.062”

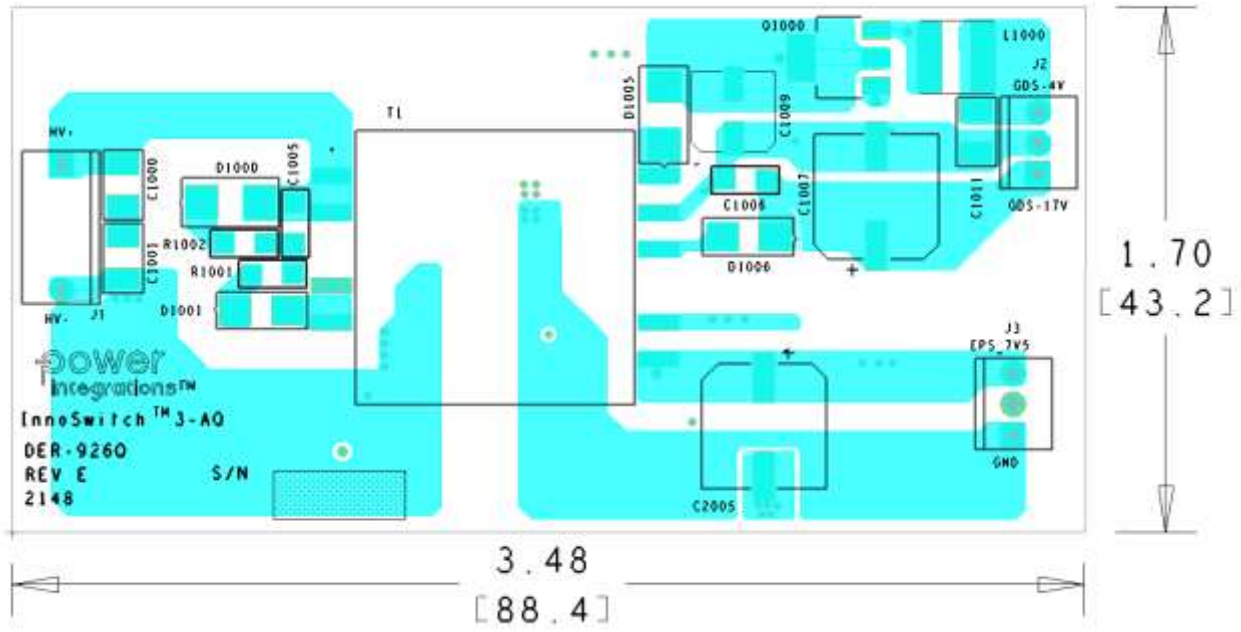


Figure 5 – Printed Circuit Layout, Top.

Figure 6 – Printed Circuit Layout, Bottom.

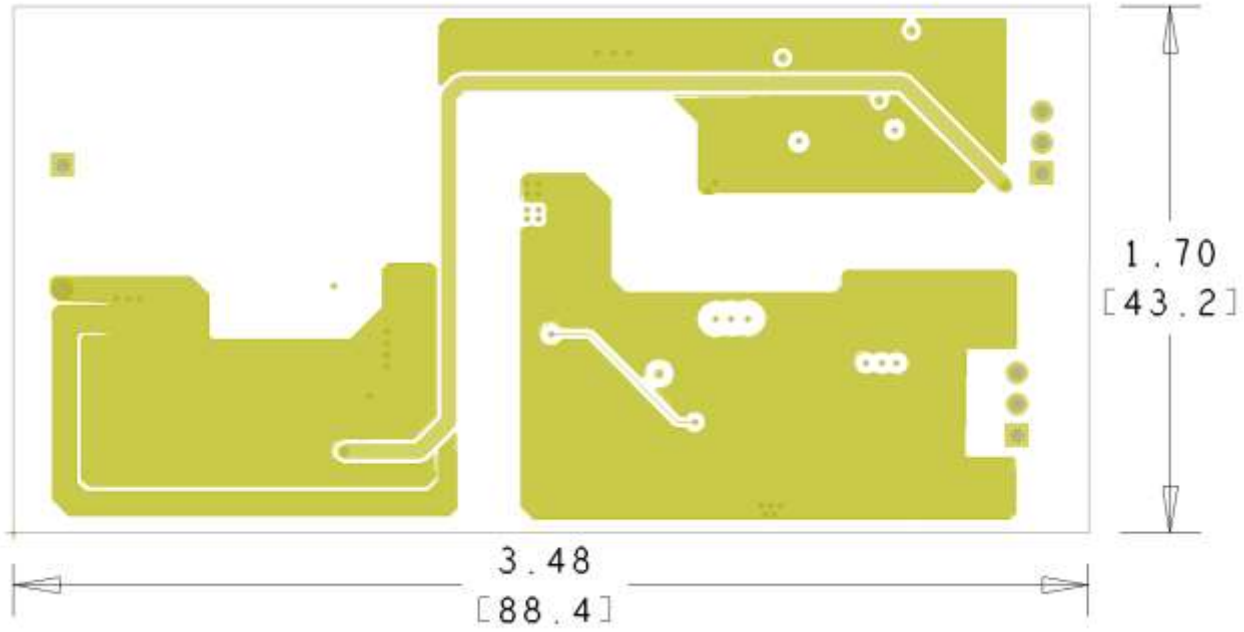


Figure 7 – Printed Circuit Layout, Inner Layer 1.

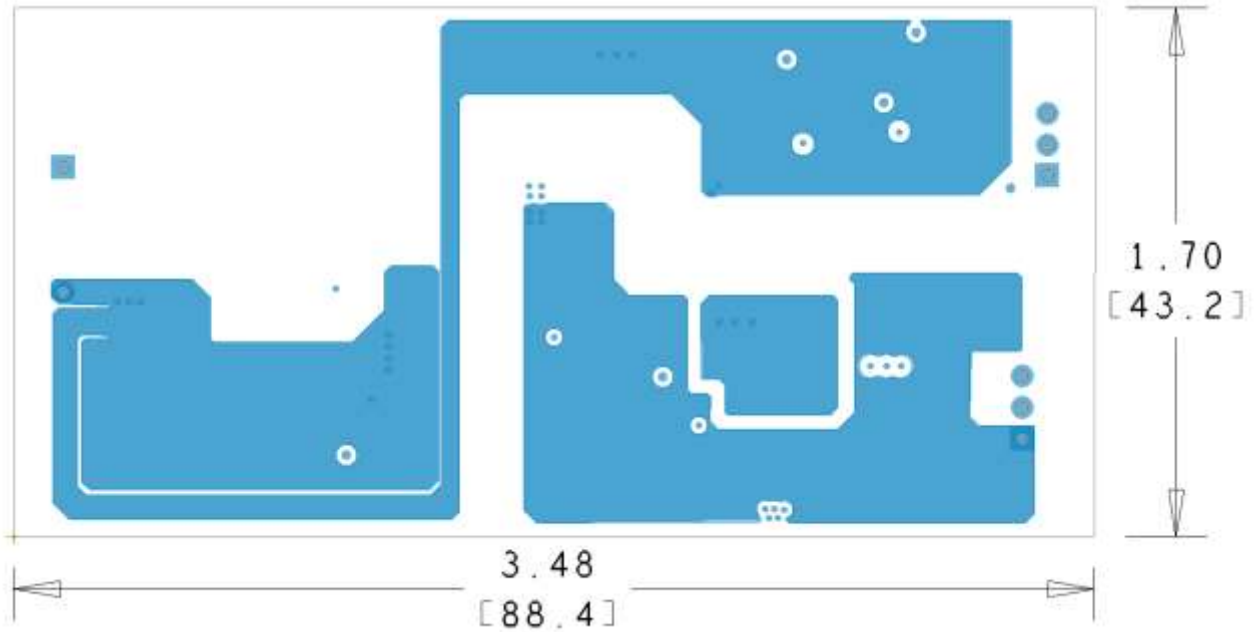


Figure 8 – Printed Circuit Layout, Inner Layer 2.

7 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1000 C1001	0.1 µF, ±10%, 630 V, Low ESL, High Voltage, Ceramic, X7R, 1210 (3225 Metric)	C1210C104KBRACAUTO	Kemet
2	1	C1004	4.7 µF ±20% 25V Ceramic X5R 0603 (1608 Metric)	GRT188R61E475ME13D	Murata
3	1	C1005	4700 pF ±5% 200 V Ceramic C0G, NP0 1206 (3216 Metric)	CGJ5H3C0G2D472J115AA	TDK
4	1	C1006	10 µF, ±10%, 35 V, Ceramic, X7R, 1206 (3216 Metric)	GMJ316BB7106KLHT	Taiyo Yuden
5	1	C1007	330 µF, ±20%, 25 V, Aluminum - Polymer, 0.406" L x 0.406" W (10.30 mm x 10.30 mm),Height 0.413" (10.50 mm), SMD, 4000 Hrs @ 125°C	HHXC250ARA331MJA0G	United Chemi-Con
6	1	C1009	82 µF, ±20%, 25 V, Aluminum - Polymer, 0.260" L x 0.260" W (6.60 mm x 6.60 mm) x Height 0.236" (6.00 mm), SMD	A768EB826M1ELAS036	KEMET
7	1	C1011	22 µF, ±10%, 10 V, Ceramic, X7R, 1210 (3225 Metric)	CL32B226KPJVPNE	Samsung
8	1	C2000	2.2 µF ±10% 25 V Ceramic X7R 0805 (2012 Metric)	GCM21BR71E225KA73L	Murata
9	1	C2001	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
10	1	C2002	330 pF, ±5%, 50 V, Ceramic, C0G, NP0, 0603 (1608 Metric)	C0603C331J5GACAUTO	KEMET
11	1	C2003	47 pF, ±5%, 200 V, C0G_NP0, -55°C ~ 125°C, 0805 (2012 Metric)	C0805C470J2GACAUTO	Kemet
12	1	C2004	100 pF,±10%, 200 V, Ceramic, C0G,NP0, 0805 (2012 Metric)	C0805C101K2GACAUTO	KEMET
13	1	C2005	470 µF, ±20%, 25 V, Aluminum - Polymer, 0.406" L x 0.406" W (10.30 mm x 10.30 mm), Height 0.504" (12.80 mm), SMD, 4000 Hrs @ 125°C	B40900B5477M000	EPCOS
14	1	D1000	TVS DIODE, 56 V (1 mA), 100 V (40 A, 8/20 µs, Ipp), SMT, SMB, (DO-214AA)	SM6T56AY	ST Micro
15	1	D1001	Diode Standard 1000 V 1 A SMT DO-214AC (SMA)	S1MHE3_A/I	Vishay
16	1	D1003	IC, VREF, SHUNT, 36 V, 0.5%, -40°C ~ 125°C (TA), SOT23-3, TO-236-3, SC-59, SOT-23-3	TL431LIBQDBZRQ1	Texas Instruments
17	1	D1005	Diode, Standard, 200 V, 2 A, SMT, DO-214AA (SMB), DO214AA (SMB)(SMBJ)	ESH2DHE3_A/H	Vishay
18	1	D1006	Diode, Standard, 400 V, 2 A, SMT, SMA, DO-214AC (SMA)	NRVUA140VT3G	ON Semi
19	1	IC1000 A	InnoSwitch3-AQ, 900 V, InSOP-24D	INN3996CQ	Power Integrations
20	1	J1	CONN, POLARIZED HEADER, 5POS, 0.100" PITCH	0022232051	Molex
21	2	J2 J3	CONN, POLARIZED HEADER, 3POS, 0.100" PITCH, TIN	0022232031	Molex
22	1	L1000	10 µH, Shielded Inductor, 2.45A, 48 mΩ, Nonstandard	TYS6045100M-10	Laird-Signal Integrity Products
23	1	Q1000	PNP, Bipolar (BJT) Transistor 80V 1A 100 MHz 1.8 W, Surface Mount, SOT-223, SC-73, TO-261AA	Nexperia USA Inc.	BCP53-10TF
24	1	Q1001	Bipolar (BJT) Transistor, NPN, 45V, 100mA, 100MHz, 250mW, Surface Mount,SOT23, TO-236AB	NXP USA Inc.	BC850C,215
25	1	Q2000	MOSFET, N-Channel, 200 V, 13 A (Tc), 68W (Tc), Automotive, AEC-Q101, PowerPAK® SO-8, PowerPAK SO-8	SQJ454EP-T1_GE3	Visha
26	1	Q2001	MOSFET,N-Channel, 30V, 300mA (Ta), 200mW, Surface Mount, UMT3, SC-70, SOT-323	RHU003N03FRAT106	Rohm Semi
27	1	R1001	RES, 100 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1000V	Panasonic
28	1	R1002	RES, 1.0 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1001V	Panasonic
29	1	R1003	RES, 7.32 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7321V	Panasonic
30	1	R1004	RES, 80.6 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF8062V	Panasonic
31	1	R1005	RES, 49.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4992V	Panasonic

32	1	R1006	RES, 47 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ470V	Panasonic
33	1	R1007	RES, 1.58 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1581V	Panasonic
34	1	R2000	RES, 12.1 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1212V	Panasonic
35	1	R2001	RES, 102 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1023V	Panasonic
36	1	R2002	RES, 20.5 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2052V	Panasonic
37	1	R2003	RES, 100 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ101V	Panasonic
38	2	R2004 R2006	RES, 200 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2000V	Panasonic
39	1	R2005	RES, SMD, 0.02 Ω, 1%, 0.333 W, 1210, Current Sense, Moisture Resistant	ERJ-L14KF20MU	Panasonic
40	4	R2009 R2010 R2012 R2013	RES, 220 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ221V	Panasonic
41	1	R2011	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ103X	Panasonic
42	1	T1	Custom Flyback Transfomer, EFD20, 12pins	ZC1826-AL	COILCRAFT

8 Transformer (T1) Specification

8.1 *Electrical Diagram*

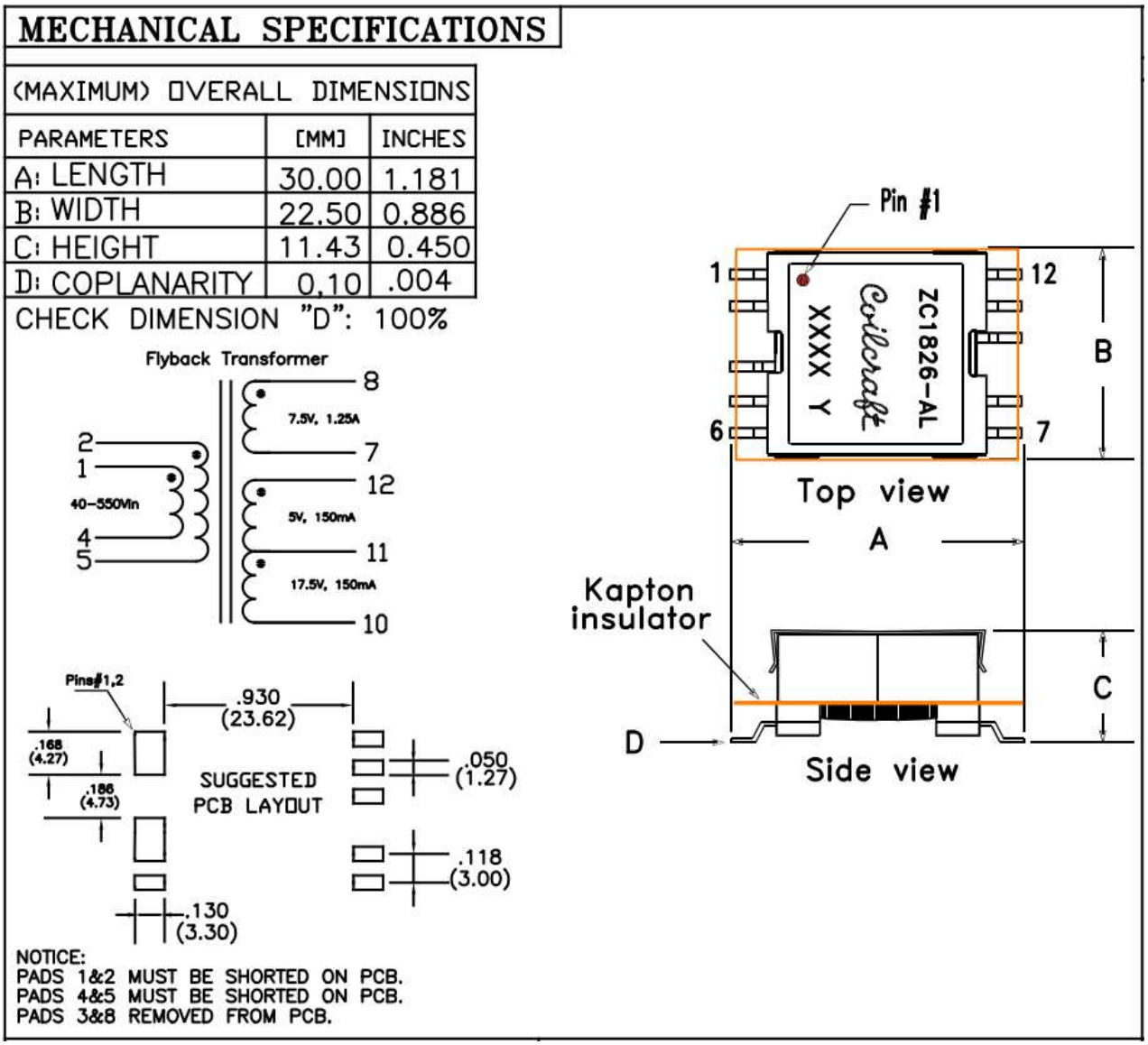


Figure 9 – Transformer Mechanical Specifications.

8.2 *Electrical Specifications*

ELECTRICAL SPECIFICATIONS "ALL ELECTRICAL SPECIFICATIONS @ 25°C"

INDUCTANCE(uH) (CSC) 100%
100 KHZ, 0.1 VRMS, 0 ADC

PINS	MIN	MAX
1–4	256	284

INDUCTANCE(uH) 100%
100KHZ, 0.1 VRMS, 1 ADC

PINS	MIN	
1,2,–4,5	230	

HI POT(3mA) 100%
(VRMS, Applied for 1 minute)

VOLTAGE:	FROM PINS (shorted)	TO PINS (shorted)
3000	1,2,4,5	7,8,10,11,12
1500	ALL PINS	CORE
500	8,7	12,11,10

DC RESISTANCE (OHMS) 100%

PINS		MAX
1–4		1.36
12–11		.075
11–10		.210
8–7		.026
2–5		1.67

TURNS RATIO 100%
Apply 0.05 Vrms, 30 KHZ to pins 1–4

MEASURE PINS:	MIN	MAX
12–11	.135	.144
11–10	.388	.412
8–7	.174	.185
2–5	.970	1.03

LEAKAGE INDUCTANCE(uH) 100%
100 KHZ, 0.1 VRMS

PINS	SHORT PINS	MAX
1,2–4,5	7,8,10,11,12	2.5

Figure 10 – Transformer Electrical Specifications.

NOTE:
Vendor: Coilcraft
Power Integrations P/N: ZC1826-AL
Date Released: 10.18.21

9 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_110321; Rev.2.2; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	7.50		7.50	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	530.00		530.00	V	Input DC voltage 1
6	IOUT1	1.740		1.740	A	Output current 1
7	POUT1			13.05	W	Output power 1
8	EFFICIENCY1	0.85		0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
10	**OPERATING CONDITION 2**					
11	VINDC2	375.00		375.00	V	Input DC voltage 2
12	IOUT2	1.740		1.740	A	Output current 2
13	POUT2			13.05	W	Output power 2
14	EFFICIENCY2			0.85		Converter efficiency for output 2
15	Z_FACTOR2			0.50		Z-factor for output 2
16	**OPERATING CONDITION 3**					
17	VINDC3	40.00		40.00	V	Input DC voltage 3
18	IOUT3	1.740		1.740	A	Output current 3
19	POUT3		Info	13.05	W	The device is capable of delivering 7W at the specified input voltage. Verify thermal performance.
20	EFFICIENCY3			0.85		Converter efficiency for output 3
21	Z_FACTOR3			0.50		Z-factor for output 3
22	**PRIMARY CONTROLLER SELECTION**					
23	ENCLOSURE			ADAPTER		Power supply enclosure
24	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
25	VDRAIN_BREAKDOWN			900	V	Device breakdown voltage
26	DEVICE_GENERIC			INN39X6		Device selection
27	DEVICE_CODE	INN3996CQ		INN3996CQ		Device code
28	PDEVICE_MAX			20	W	Device maximum power capability
29	RDSON_25DEG			2.80	Ω	Primary switch on-time resistance at 25°C
30	RDSON_100DEG			4.50	Ω	Primary switch on-time resistance at 100°C
31	ILIMIT_MIN			1.232	A	Primary switch minimum current limit
32	ILIMIT_TYP			1.450	A	Primary switch typical current limit
33	ILIMIT_MAX			1.633	A	Primary switch maximum current limit
34	VDRAIN_ON_PRSW			1.67	V	Primary switch on-time voltage drop
35	VDRAIN_OFF_PRSW			610	V	Peak drain voltage on the primary switch during turn-off
36	**WORST CASE ELECTRICAL PARAMETERS**					
37	FSWITCHING_MAX	79000		79000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
38	VOR	40.0		40.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
39	KP			0.780		Measure of continuous/discontinuous mode of operation
40	MODE_OPERATION			CCM		Mode of operation
41	DUTYCYCLE			0.511		Primary switch duty cycle
42	TIME_ON_MIN			0.59	us	Minimum primary switch on-time

43	TIME_ON_MAX			10.93	us	Maximum primary switch on-time
44	TIME_OFF			6.19	us	Primary switch off-time
45	LPRIMARY_MIN			260.5	uH	Minimum primary magnetizing inductance
46	LPRIMARY_TYP			274.2	uH	Typical primary magnetizing inductance
47	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
48	LPRIMARY_MAX			287.9	uH	Maximum primary magnetizing inductance
49	**PRIMARY CURRENT**					
50	IAVG_PRIMARY			1.477	A	Primary switch average current
51	IPEAK_PRIMARY			1.477	A	Primary switch peak current
52	IPEDESTAL_PRIMARY			0.370	A	Primary switch current pedestal
53	IRIPPLE_PRIMARY			1.477	A	Primary switch ripple current
54	IRMS_PRIMARY			0.604	A	Primary switch RMS current
55	**TRANSFORMER CONSTRUCTION PARAMETERS**					
56	CORE SELECTION					
57	CORE	CUSTOM		CUSTOM		Core selection
58	CORE NAME	EFD20		EFD20		Core code
59	AE	31.0		31.0	mm^2	Core cross sectional area
60	LE	47.0		47.0	mm	Core magnetic path length
61	AL	1440		1440	nH	Ungapped core effective inductance per turns squared
62	VE	1460		1460	mm^3	Core volume
63	BOBBIN NAME	EFD20		EFD20		Bobbin name
64	AW	28.1		28.1	mm^2	Bobbin window area
65	BW	13.20		13.20	mm	Bobbin width
66	MARGIN	0.0		0.0	mm	Bobbin safety margin
67	**PRIMARY WINDING**					
68	NPRIMARY			43		Primary winding number of turns
69	BPEAK			3610	Gauss	Peak flux density
70	BMAX			3142	Gauss	Maximum flux density
71	BAC			1571	Gauss	AC flux density (0.5 x Peak to Peak)
72	ALG			148	nH	Typical gapped core effective inductance per turns squared
73	LG			0.236	mm	Core gap length
74	**SECONDARY WINDING**					
75	NSECONDARY	8		8		Secondary winding number of turns
76	**BIAS WINDING**					
77	NBIAS			19		Bias winding number of turns
78	**PRIMARY COMPONENTS SELECTION**					
79	BIAS WINDING					
80	VBIAS	17.00		17.00	V	Rectified bias voltage
81	VF_BIAS			0.70	V	Bias winding diode forward drop
82	VREVERSE_BIASDIODE			251.19	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
83	CBIAS			22	uF	Bias winding rectification capacitor
84	CBPP			4.70	uF	BPP pin capacitor
85	**SECONDARY COMPONENTS SELECTION**					
86	FEEDBACK COMPONENTS					
87	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
88	RFB_LOWER			20.50	kΩ	Lower feedback resistor
89	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
90	**MULTIPLE OUTPUT PARAMETERS**					
91	**OUTPUT 1**					
92	VOUT1			7.50	V	Output 1 voltage
93	IOUT1	1.300		1.300	A	Output 1 current

94	POUT1			9.75	W	Output 1 power
95	IRMS_SECONDARY1			2.374	A	Root mean squared value of the secondary current for output 1
96	IRIPPLE_CAP_OUTPUT1			1.987	A	Current ripple on the secondary waveform for output 1
97	NSECONDARY1			8		Number of turns for output 1
98	VREVERSE_RECTIFIER1			106.10	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
99	SRFET1	SQJ454EP		SQJ454EP		Secondary rectifier (Logic MOSFET) for output 1
100	VF_SRFET1			0.83	V	SRFET on-time drain voltage for output 1
101	VBREAKDOWN_SRFET1			200	V	SRFET breakdown voltage for output 1
102	RDSON_SRFET1			150	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
103	**OUTPUT 2**					
104	VOUT2	17.00		17.00	V	Output 2 voltage
105	IOUT2	0.140		0.140	A	Output 2 current
106	POUT2			2.38	W	Output 2 power
107	IRMS_SECONDARY2			0.256	A	Root mean squared value of the secondary current for output 2
108	IRIPPLE_CAP_OUTPUT2			0.214	A	Current ripple on the secondary waveform for output 2
109	NSECONDARY2			19		Number of turns for output 2
110	VREVERSE_RECTIFIER2			251.19	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2
111	SRFET2	AUTO	Info	SQJ454EP		The voltage stress (including the parasitic ring) on the secondary MOSFET selected may exceed the device BVDSS: pick a MOSFET with a higher BVDSS
112	VF_SRFET2			0.83	V	SRFET on-time drain voltage for output 2
113	VBREAKDOWN_SRFET2			200	V	SRFET breakdown voltage for output 2
114	RDSON_SRFET2			150.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 2
115	**OUTPUT 3**					
116	VOUT3	4.00		4.00	V	Output 3 voltage
117	IOUT3	0.140		0.140	A	Output 3 current
118	POUT3			0.56	W	Output 3 power
119	IRMS_SECONDARY3			0.256	A	Root mean squared value of the secondary current for output 3
120	IRIPPLE_CAP_OUTPUT3			0.214	A	Current ripple on the secondary waveform for output 3
121	NSECONDARY3			5		Number of turns for output 3
122	VREVERSE_RECTIFIER3			65.63	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 3
123	SRFET3	AUTO		SQSA80ENW		Secondary rectifier (Logic MOSFET) for output 3
124	VF_SRFET3			0.82	V	SRFET on-time drain voltage for output 3
125	VBREAKDOWN_SRFET3			80	V	SRFET breakdown voltage for output 3
126	RDSON_SRFET3			27.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 3

127	PO_TOTAL		Info	12.69	W	The total power of all outputs does not add up to the total power of the design
128	NEGATIVE OUTPUT	3		3		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
129	**INPUT VOLTAGE SET-POINTS ANALYSIS**					
130	**TOLERANCE CORNER**					
131	USER_VINDC	40		40	V	Input DC voltage corner to be evaluated
132	USER_ILIMIT	TYP		1.450	A	Current limit corner to be evaluated
133	USER_LPRIMARY	TYP		274.2	uH	Primary inductance corner to be evaluated
134	**OPERATING CONDITION SELECTION**					
135	POUT			13.05	W	Output power to be evaluated
136	EFFICIENCY			0.85		Converter efficiency to be evaluated
137	Z FACTOR			0.50		Z-factor to be evaluated
138	FSWITCHING			57385	Hz	Maximum switching frequency at full load
139	KP			0.923		Measure of continuous/discontinuous mode of operation
140	MODE_OPERATION			CCM		Mode of operation
141	DUTYCYCLE			0.511		Primary switch duty cycle
142	TIME_ON			8.90	us	Primary switch on-time
143	TIME_OFF			8.53	us	Primary switch off-time
144	**PRIMARY CURRENT**					
145	IAVG_PRIMARY			0.370	A	Primary switch average current
146	IPEAK_PRIMARY			1.347	A	Primary switch peak current
147	IPEDESTAL_PRIMARY			0.104	A	Primary switch current pedestal
148	IRIPPLE_PRIMARY			1.244	A	Primary switch ripple current
149	IRMS_PRIMARY			0.578	A	Primary switch RMS current
150	**MAGNETIC FLUX DENSITY**					
151	BPEAK			3053	Gauss	Peak flux density
152	BMAX			2772	Gauss	Maximum flux density
153	BAC			1279	Gauss	AC flux density (0.5 x Peak to Peak)

NOTE: Non-isolated output 17 V and -4 V can only use schottky diodes.

10 Performance Data

10.1 *Efficiency and Output Voltage Regulation*

10.1.1 Ambient Temperature: -40 ºC

Input Measurement		7.5 V Measurement				17 V Measurement				-4 V Measurement					
V_{IN} (VDC)	**P_{IN} (W)**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**V Reg (%)**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**V Reg (%)**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**V Reg (%)**	**Total P_{OUT} (W)**	**Eff (%)**
40	1.11	7.62	65	0.50	1.54	16.23	19	0.30	-4.54	4.02	19	0.08	0.56	0.88	79.0
	14.80	7.45	1297	9.67	-0.61	16.41	139	2.29	-3.46	3.93	140	0.55	-1.80	12.50	85.0
	10.26	7.52	1128	8.48	0.28	17.78	19	0.33	4.57	4.04	19	0.08	1.00	8.89	86.5
	12.79	7.48	1128	8.43	-0.31	16.43	120	1.98	-3.34	3.94	121	0.48	-1.49	10.89	85.5
	3.54	7.62	65	0.50	1.61	15.85	121	1.91	-6.78	3.92	121	0.48	-1.89	2.88	79.9
130	1.12	7.61	65	0.50	1.52	16.24	19	0.30	-4.46	4.02	19	0.08	0.51	0.88	79.1
	14.33	7.60	1297	9.86	1.31	16.70	140	2.34	-1.76	3.95	141	0.55	-1.27	12.75	87.1
	10.14	7.66	1128	8.63	2.08	18.12	19	0.34	6.58	4.04	19	0.08	1.05	9.05	87.6
	12.36	7.62	1128	8.59	1.61	16.74	120	2.02	-1.51	3.96	121	0.48	-1.04	11.09	87.1
	3.38	7.60	65	0.50	1.40	15.79	121	1.90	-7.13	3.92	121	0.47	-2.06	2.87	80.4
300	1.20	7.62	65	0.50	1.61	16.28	19	0.30	-4.25	4.02	19	0.08	0.56	0.88	72.9
	14.49	7.65	1297	9.92	1.95	16.84	140	2.35	-0.92	3.91	140	0.55	-2.36	12.82	85.9
	10.19	7.69	1128	8.67	2.55	18.39	18	0.34	8.17	4.04	19	0.08	0.97	9.09	86.3
	12.89	7.66	1128	8.64	2.10	16.86	120	2.03	-0.80	3.92	121	0.47	-2.03	11.14	85.7
	3.43	7.60	65	0.50	1.36	15.79	120	1.90	-7.10	3.90	121	0.47	-2.49	2.87	78.1
375	1.32	7.62	65	0.50	1.63	16.29	19	0.30	-4.20	4.02	19	0.08	0.56	0.88	69.1
	15.11	7.65	1297	9.93	2.06	16.88	139	2.35	-0.70	3.90	140	0.55	-2.58	12.83	86.3
	10.45	7.70	1128	8.68	2.64	18.50	18	0.34	8.83	4.04	19	0.08	0.99	9.09	85.5
	13.05	7.66	1128	8.64	2.17	16.89	120	2.03	-0.62	3.91	121	0.47	-2.20	11.14	84.8
	3.58	7.60	65	0.50	1.32	15.79	120	1.90	-7.12	3.90	121	0.47	-2.44	2.87	76.4
530	1.46	7.62	65	0.50	1.55	16.28	19	0.30	-4.24	4.02	19	0.08	0.59	0.88	64.3
	15.21	7.67	1297	9.95	2.25	16.94	139	2.36	-0.35	3.90	140	0.55	-2.43	12.85	82.6
	10.90	7.71	1128	8.69	2.76	18.61	18	0.34	9.44	4.04	19	0.08	1.04	9.11	83.0
	13.16	7.67	1128	8.65	2.29	16.94	120	2.04	-0.35	3.92	121	0.47	-2.01	11.16	82.8
	4.06	7.59	65	0.49	1.26	15.78	120	1.90	-7.16	3.90	121	0.47	-2.40	2.87	72.3
			Max %Reg		**2.76**		Max %Reg		**9.44**		Max %Reg		**1.05**		
			Min %Reg		**-0.61**		Min %Reg		**-7.16**		Min %Reg		**-2.58**		
			Limit %		**+7 / -13**		Limit %		**+22 / -9**		Limit %		**±7**		
			Result		**PASS**		Result		**PASS**		Result		**PASS**		

10.1.2 Ambient Temperature: 25 ºC

Input Measurement		7.5 V Measurement				17 V Measurement				-4 V Measurement					
V_{IN} (VDC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V Reg (%)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V Reg (%)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V Reg (%)	Total P_{OUT} (W)	Eff (%)
	1.10	7.52	65	0.49	0.20	16.22	19	0.30	-4.62	4.03	19	0.08	0.79	0.87	79.4
	14.80	7.35	1297	9.54	-1.96	16.58	140	2.32	-2.49	3.93	140	0.55	-1.69	12.41	83.8
40	10.26	7.41	1128	8.36	-1.19	17.76	19	0.33	4.46	4.05	19	0.08	1.25	8.77	85.5
	12.79	7.38	1128	8.32	-1.58	16.59	120	2.00	-2.40	3.94	121	0.48	-1.41	10.80	84.5
	3.54	7.52	65	0.49	0.26	15.74	121	1.90	-7.42	3.92	121	0.47	-2.08	2.86	81.0
	1.12	7.52	65	0.49	0.23	16.23	19	0.30	-4.56	4.03	19	0.08	0.76	0.87	77.9
	14.33	7.51	1297	9.74	0.11	16.86	140	2.36	-0.83	3.94	141	0.55	-1.54	12.65	88.3
130	10.14	7.55	1128	8.52	0.69	18.08	19	0.34	6.35	4.05	19	0.08	1.31	8.93	88.1
	12.36	7.52	1128	8.48	0.29	16.88	120	2.03	-0.71	3.95	121	0.48	-1.31	10.99	88.9
	3.38	7.51	65	0.49	0.14	15.69	121	1.89	-7.74	3.91	121	0.47	-2.19	2.85	84.4
	1.20	7.53	65	0.49	0.34	16.27	19	0.30	-4.31	4.03	19	0.08	0.76	0.87	72.4
	14.49	7.55	1297	9.79	0.66	16.99	140	2.38	-0.04	3.93	141	0.55	-1.67	12.72	87.8
300	10.19	7.58	1128	8.55	1.10	18.30	19	0.34	7.62	4.05	19	0.08	1.22	8.97	88.0
	12.89	7.56	1128	8.52	0.75	17.00	121	2.05	0.00	3.94	121	0.48	-1.43	11.05	85.7
	3.43	7.51	65	0.49	0.13	15.68	121	1.89	-7.74	3.91	121	0.47	-2.36	2.85	83.2
	1.32	7.53	65	0.49	0.37	16.29	19	0.30	-4.17	4.03	19	0.08	0.80	0.87	66.4
	15.11	7.56	1297	9.80	0.78	17.04	140	2.38	0.21	3.88	140	0.55	-2.91	12.73	84.3
375	10.45	7.59	1128	8.56	1.19	18.37	19	0.34	8.07	4.05	19	0.08	1.16	8.98	85.9
	13.05	7.56	1128	8.53	0.85	17.04	120	2.05	0.23	3.90	121	0.47	-2.46	11.05	84.7
	3.58	7.51	65	0.49	0.11	15.68	121	1.89	-7.75	3.90	121	0.47	-2.61	2.85	79.7
	1.46	7.54	65	0.49	0.48	16.34	19	0.30	-3.88	0.00	19	0.08	0.88	0.88	59.9
	15.21	7.57	1297	9.81	0.89	17.09	140	2.39	0.55	3.88	140	0.54	-3.04	12.75	83.8
530	10.90	7.61	1128	8.58	1.43	18.59	19	0.34	9.32	4.05	19	0.08	1.18	9.00	82.6
	13.16	7.57	1128	8.54	0.96	17.11	120	2.06	0.62	3.90	121	0.47	-2.57	11.07	84.2
	4.06	7.51	65	0.49	0.08	15.69	121	1.89	-7.71	3.90	121	0.47	-2.48	2.85	70.3
			Max %Reg		**1.43**		Max %Reg		**9.32**		Max %Reg		**1.31**		
			Min %Reg		**-1.96**		Min %Reg		**-7.75**		Min %Reg		**-3.04**		
			Limit %		**+7 / -13**		Limit %		**+22 / -9**		Limit %		**±7**		
			Result		**PASS**		Result		**PASS**		Result		**PASS**		

10.1.3 Ambient Temperature: 85 ºC

Input Measurement		7.5 V Measurement				17 V Measurement				-4 V Measurement					
V_{IN} (VDC)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V Reg (%)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V Reg (%)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V Reg (%)	Total P_{OUT} (W)	Eff (%)
40	1.15	7.46	65	0.49	-0.49	16.29	19	0.30	-4.21	4.04	19	0.08	0.95	0.87	75.3
	15.56	7.28	1297	9.44	-2.97	16.72	140	2.34	-1.63	3.92	140	0.55	-2.04	12.33	79.3
	10.67	7.37	1128	8.31	-1.74	17.80	19	0.33	4.72	4.06	19	0.08	1.46	8.72	81.7
	13.29	7.31	1128	8.25	-2.49	16.73	121	2.02	-1.58	3.92	121	0.47	-1.91	10.74	80.8
	3.65	7.47	65	0.49	-0.43	15.73	121	1.90	-7.45	3.91	121	0.47	-2.38	2.86	78.3
130	1.12	7.46	65	0.49	-0.48	16.28	19	0.30	-4.24	4.04	19	0.08	0.89	0.87	77.9
	14.60	7.45	1297	9.66	-0.73	17.00	140	2.38	-0.02	3.92	141	0.55	-1.88	12.59	86.2
	10.35	7.50	1128	8.46	0.01	18.09	19	0.34	6.41	4.06	19	0.08	1.51	8.88	85.8
	12.70	7.47	1128	8.43	-0.38	17.04	121	2.05	0.24	3.94	121	0.48	-1.58	10.96	86.3
	3.42	7.46	65	0.49	-0.53	15.66	121	1.89	-7.87	3.90	121	0.47	-2.48	2.85	83.2
300	1.24	7.47	65	0.49	-0.37	16.32	19	0.30	-3.99	4.04	19	0.08	0.88	0.87	70.3
	14.85	7.50	1297	9.73	-0.01	17.16	140	2.40	0.92	3.93	140	0.55	-1.84	12.68	85.4
	10.13	7.53	1128	8.50	0.45	18.27	19	0.34	7.48	4.06	19	0.08	1.53	8.91	88.0
	12.84	7.51	1128	8.47	0.13	17.17	120	2.07	0.99	3.94	121	0.48	-1.54	11.01	85.8
	3.43	7.46	65	0.49	-0.53	15.65	120	1.89	-7.93	3.90	121	0.47	-2.53	2.84	82.9
375	1.36	7.48	65	0.49	-0.32	16.35	19	0.31	-3.81	4.04	19	0.08	0.93	0.87	64.0
	14.87	7.51	1297	9.74	0.13	17.21	140	2.41	1.23	3.88	141	0.54	-3.08	12.70	85.4
	10.35	7.54	1128	8.50	0.54	18.35	19	0.34	7.93	4.05	19	0.08	1.25	8.92	86.2
	12.93	7.52	1128	8.48	0.24	17.22	121	2.08	1.27	3.89	121	0.47	-2.67	11.03	85.3
	3.56	7.46	65	0.49	-0.53	15.66	121	1.89	-7.91	3.88	121	0.47	-3.03	2.84	79.9
530	1.38	7.49	65	0.49	-0.13	16.43	19	0.31	-3.36	4.04	19	0.08	1.03	0.87	63.4
	15.41	7.52	1297	9.76	0.27	17.28	140	2.42	1.65	3.85	140	0.54	-3.79	12.71	82.5
	10.96	7.56	1128	8.52	0.75	18.54	19	0.34	9.04	4.05	19	0.08	1.34	8.94	81.6
	13.62	7.53	1128	8.49	0.42	17.30	120	2.08	1.76	3.87	121	0.47	-3.20	11.04	81.1
	3.79	7.46	65	0.49	-0.55	15.67	120	1.89	-7.85	3.88	121	0.47	-2.99	2.84	75.1
			Max %Reg		**0.75**		Max %Reg		**9.04**		Max %Reg		**1.53**		
			Min %Reg		**-2.97**		Min %Reg		**-7.93**		Min %Reg		**-3.79**		
			Limit %		**+7 / -13**		Limit %		**+22 / -9**		Limit %		**±7**		
			Result		**PASS**		Result		**PASS**		Result		**PASS**		

10.2 *Output Voltage Ripple*

10.2.1 Output Voltage Ripple Measurement Set-Up

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The Teledyne Lecroy PP026 probe adapter is affixed with once capacitor tied in parallel across the probe tip. The capacitor include one (1) 1 μF / 50 V ceramic type. Noise filter setting is oscilloscope should be set to -3dB at 3.125 MHz.

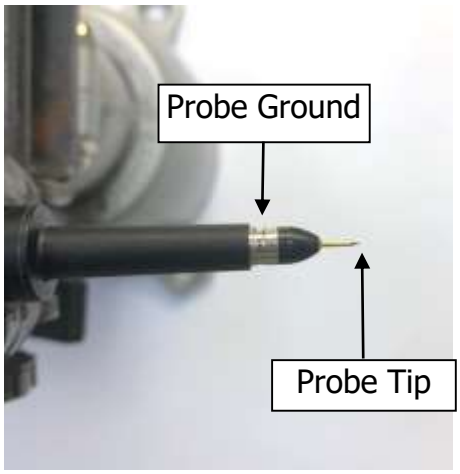


Figure 11 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

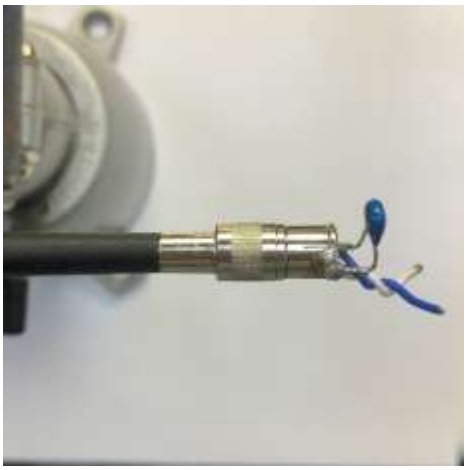


Figure 12 – Oscilloscope Probe with BNC Adapter.

10.2.2 Test Data at Ambient Temperature: -40 ºC

V_{IN}	7.5 V I_{OUT} (mA)	7.5 V Ripple (mV_{PP})	17 V I_{OUT} (mA)	17 V Ripple (mV_{PP})	4 V I_{OUT} (mA)	4 V Ripple (mV_{PP})
40	65	**62**	19	**52**	19	**7**
	1297	**179**	139	**82**	140	**24**
	1128	**151**	19	**81**	19	**7**
	1128	**125**	120	**78**	121	**17**
	65	**79**	121	**84**	121	**23**
130	65	**84**	19	**51**	19	**10**
	1297	**139**	140	**85**	141	**9**
	1128	**168**	19	**78**	19	**9**
	1128	**136**	120	**81**	121	**9**
	65	**95**	121	**73**	121	**13**
300	65	**112**	19	**60**	19	**14**
	1297	**165**	140	**96**	140	**29**
	1128	**202**	18	**93**	19	**17**
	1128	**165**	120	**96**	121	**30**
	65	**120**	120	**79**	121	**43**
375	65	**113**	19	**64**	19	**14**
	1297	**173**	139	**101**	140	**32**
	1128	**209**	18	**99**	19	**21**
	1128	**169**	120	**100**	121	**31**
	65	**124**	120	**82**	121	**44**
530	65	**145**	19	**80**	19	**19**
	1297	**186**	139	**115**	140	**35**
	1128	**222**	18	**110**	19	**25**
	1128	**183**	120	**108**	121	**37**
	65	**134**	120	**92**	121	**47**
	7.5 V mV_{PP} (Limit)	**7.5 V mV_{PP} (Max.)**	**17 V mV_{PP} (Limit)**	**17 V mV_{PP} (Max.)**	**4 V mV_{PP} (Limit)**	**4 V mV_{PP} (Max.)**
Data	500	**222**	150	**115**	50	**44**
Result	**PASS**		**PASS**		**PASS**	

10.2.3 Test Data at Ambient Temperature: 25 ºC

V_{IN}	7.5 V I_{OUT} (mA)	7.5 V Ripple (mV_{PP})	17 V I_{OUT} (mA)	17 V Ripple (mV_{PP})	4 V I_{OUT} (mA)	4 V Ripple (mV_{PP})
40	65	**60**	19	**44**	19	**6**
	1297	**153**	140	**70**	140	**12**
	1128	**143**	19	**69**	19	**7**
	1128	**157**	120	**69**	121	**13**
	65	**83**	121	**72**	121	**15**
130	65	**81**	19	**44**	19	**9**
	1297	**141**	140	**73**	141	**9**
	1128	**167**	19	**69**	19	**9**
	1128	**14**	120	**73**	121	**9**
	65	**92**	121	**62**	121	**10**
300	65	**104**	19	**51**	19	**13**
	1297	**170**	140	**83**	141	**24**
	1128	**198**	19	**80**	19	**18**
	1128	**167**	121	**81**	121	**20**
	65	**116**	121	**67**	121	**28**
375	65	**114**	19	**56**	19	**16**
	1297	**177**	140	**88**	140	**33**
	1128	**208**	19	**84**	19	**20**
	1128	**179**	120	**85**	121	**31**
	65	**125**	121	**68**	121	**36**
530	65	**112**	19	**68**	19	**17**
	1297	**187**	140	**96**	140	**38**
	1128	**222**	19	**97**	19	**24**
	1128	**182**	120	**95**	121	**40**
	65	**125**	121	**78**	121	**33**
	7.5 V mV_{PP} (Limit)	**7.5 V mV_{PP} (Max.)**	**17 V mV_{PP} (Limit)**	**17 V mV_{PP} (Max.)**	**4 V mV_{PP} (Limit)**	**4 V mV_{PP} (Max.)**
Data	500	**222**	150	**97**	50	**40**
Result	**PASS**		**PASS**		**PASS**	

10.2.4 Test Data at Ambient Temperature: 85 ºC

V_{IN}	7.5 V I_{OUT} (mA)	7.5 V Ripple (mV_{PP})	17 V I_{OUT} (mA)	17 V Ripple (mV_{PP})	4 V I_{OUT} (mA)	4 V Ripple (mV_{PP})
40	65	**63**	19	**39**	19	**6**
	1297	**24**	19	**63**	140	**12**
	1128	**150**	19	**59**	19	**7**
	1128	**234**	19	**62**	121	**9**
	65	**88**	19	**63**	121	**12**
130	65	**84**	19	**39**	19	**9**
	1297	**151**	19	**67**	141	**10**
	1128	**172**	19	**63**	19	**10**
	1128	**149**	19	**65**	121	**10**
	65	**101**	19	**60**	121	**10**
300	65	**110**	19	**46**	19	**14**
	1297	**182**	19	**75**	140	**18**
	1128	**203**	19	**71**	19	**18**
	1128	**179**	19	**73**	121	**18**
	65	**129**	19	**63**	121	**18**
375	65	**117**	19	**52**	19	**16**
	1297	**192**	19	**83**	141	**31**
	1128	**212**	19	**79**	19	**21**
	1128	**185**	19	**79**	121	**32**
	65	**134**	19	**66**	121	**43**
530	65	**110**	19	**63**	19	**18**
	1297	**193**	19	**90**	140	**41**
	1128	**217**	19	**88**	19	**27**
	1128	**195**	19	**89**	121	**44**
	65	**137**	19	**71**	121	**46**
	7.5 V mV_{PP} (Limit)	**7.5 V mV_{PP} (Max.)**	**17 V mV_{PP} (Limit)**	**17 V mV_{PP} (Max.)**	**4 V mV_{PP} (Limit)**	**4 V mV_{PP} (Max.)**
Data	500	**234**	150	**90**	50	**44**
Result	**PASS**		**PASS**		**PASS**	

11 Thermal Performance

The thermal data presented below are open frame with no thermal mitigation applied.

The worst case device temperature occurs at 40 VDC input, maximum load, with a rise of 65 °C above ambient. This indicates at an ambient of 85 °C the InnoSwitch IC device would be close or at the maximum recommended operating temperature of 125 °C.

The full load 40 VDC input condition may not be a valid operating point in many designs. It is a transient, occuring during a fault where the 12 V system has been lost, which also results in the gate supply power dramatically reducing after a few seconds (inverter enters a fault state, such as active short-circuit, where the power devices are driven statically).

However if additional thermal margin is required then a thermal pad can be placed between the outer enclosure and the SOURCE (HV-) connected area of the PCB (see Figure 2).

If considered during the design phase, the enclosure casting can have a feature grown underneath the PCB area to reduce the pad thickness required, reducing the cost and thermal impedance. This typically reduces IC temperatures by 10-15 °C. It is not necessary to place the thermal pad on the IC package itself – most heat is conducted through the SOURCE pin tab and not the package. This also avoids oversizing the thermal pad to meet primary to secondary creepage distances.

11.1 *IR Camera Reading at 25 ºC Ambient Temperature after 1 Hour Soak Time*

11.1.1 Input: 40 VDC; Output: 7.5 V / 0.65 mA, 17 V / 120 mA, -4 V 120 mA

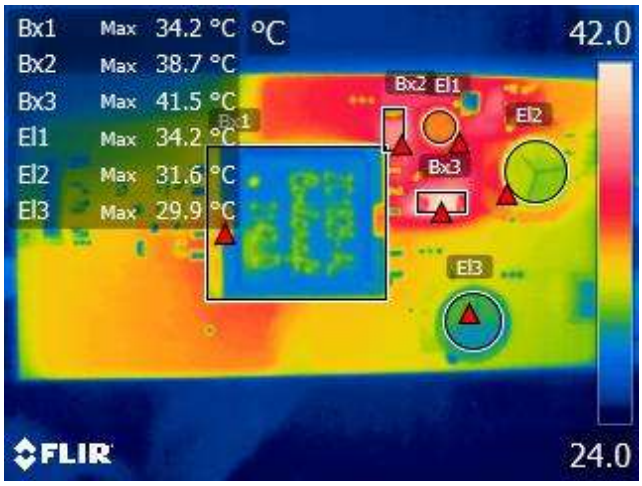


Figure 13 – Component Side.

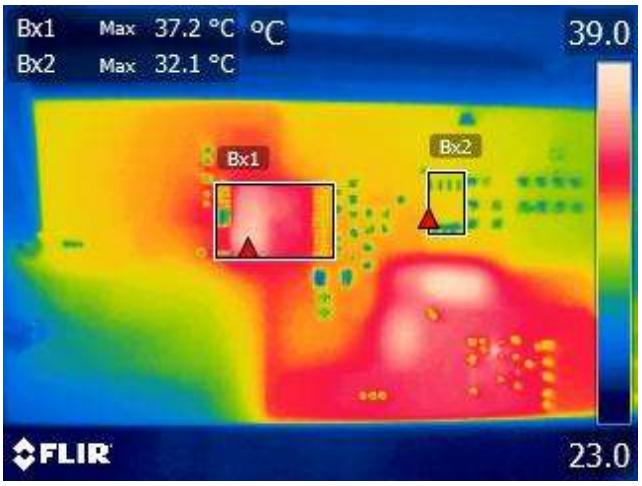


Figure 14 – Solder Side.

	Reference	ºC
Ambient		25.6
Transformer Core	T1	34.2
-4 V Diode	D1005	38.7
17 V Diode	D1006	41.5
-4 V Capacitor	C1009	34.2
17 V Capacitor	C1007	31.6
7.5 V Capacitor	C2005	29.9

	Reference	ºC
Ambient		25.6
InnoSwitch	IC1000A	37.2
7.5 V SRFET	Q2000	32.1

11.1.2 Input: 40 VDC; Output: 7.5 V / 1.3 A, 17 V / 140 mA, -4 V 140 mA

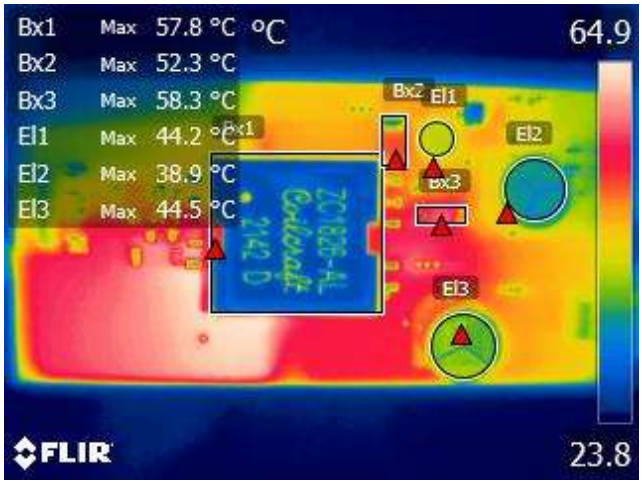


Figure 15 – Component Side.

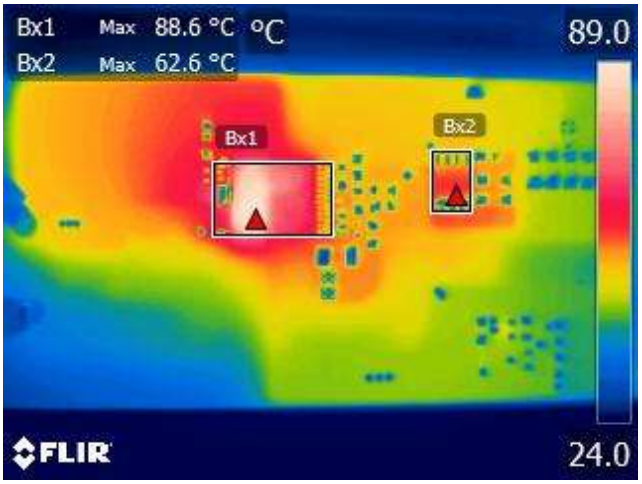


Figure 16 – Solder Side.

	Reference	ºC
Ambient		26.6
Transformer Core	T1	57.8
-4 V Diode	D1005	52.3
17 V Diode	D1006	58.3
-4 V Capacitor	C1009	44.2
17 V Capacitor	C1007	38.9
7.5 V Capacitor	C2005	44.5

	Reference	ºC
Ambient		26.6
InnoSwitch	IC1000A	88.6
7.5 V SRFET	Q2000	62.6

11.1.3 Input: 375 VDC; Output: 7.5 V / 0.65 mA, 17 V / 120 mA, -4 V 120 mA

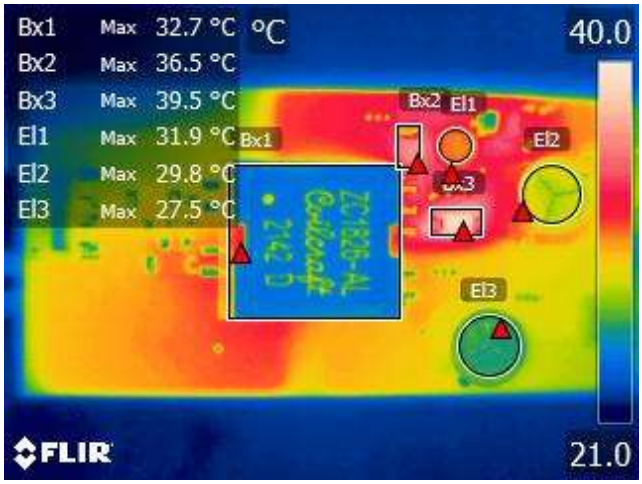


Figure 17 – Component Side.

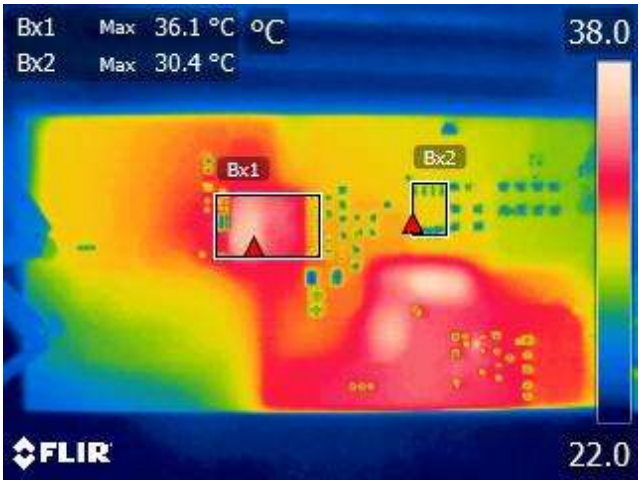


Figure 18 – Solder Side.

	Reference	ºC
Ambient		23.9
Transformer Core	T1	32.8
-4 V Diode	D1005	36.5
17 V Diode	D1006	39.5
-4 V Capacitor	C1009	31.9
17 V Capacitor	C1007	29.8
7.5 V Capacitor	C2005	27.5

	Reference	ºC
Ambient		23.9
InnoSwitch	IC1000A	36.1
7.5 V SRFET	Q2000	30.4

11.1.4 Input: 375 VDC; Output: 7.5 V / 1.3 A, 17 V / 140 mA, -4 V 140 mA

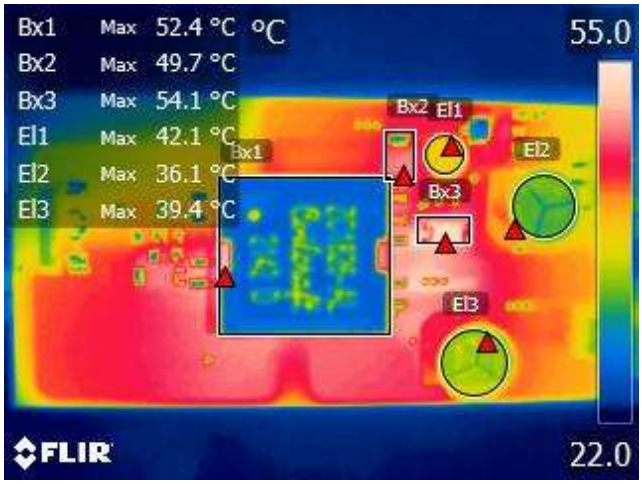


Figure 19 – Component Side.

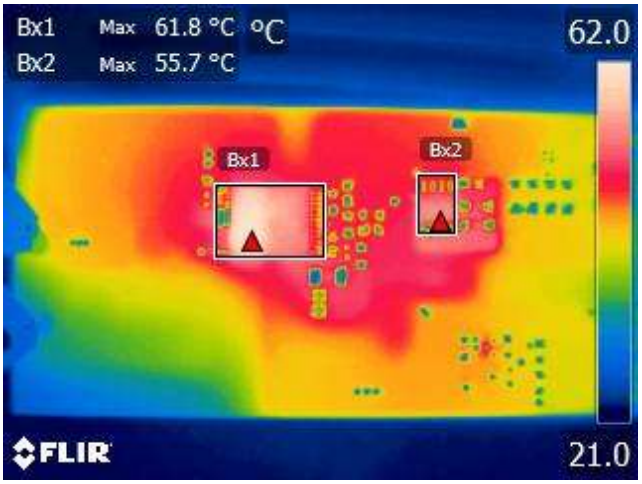


Figure 20 – Solder Side.

	Reference	ºC
Ambient		24.8
Transformer Core	T1	52.4
-4 V Diode	D1005	49.7
17 V Diode	D1006	54.1
-4 V Capacitor	C1009	42.1
17 V Capacitor	C1007	36.1
7.5 V Capacitor	C2005	39.4

	Reference	ºC
Ambient		24.8
InnoSwitch	IC1000A	61.8
7.5 V SRFET	Q2000	55.7

11.1.5 Input: 530 VDC; Output: 7.5 V / 0.65 mA, 17 V / 120 mA, -4 V 120 mA

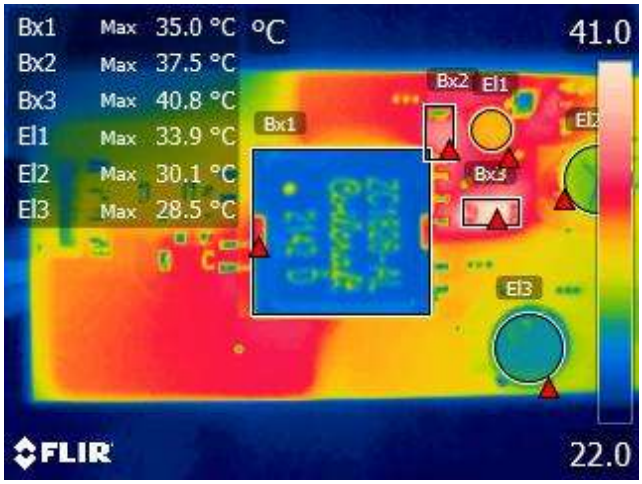


Figure 21 – Component Side.

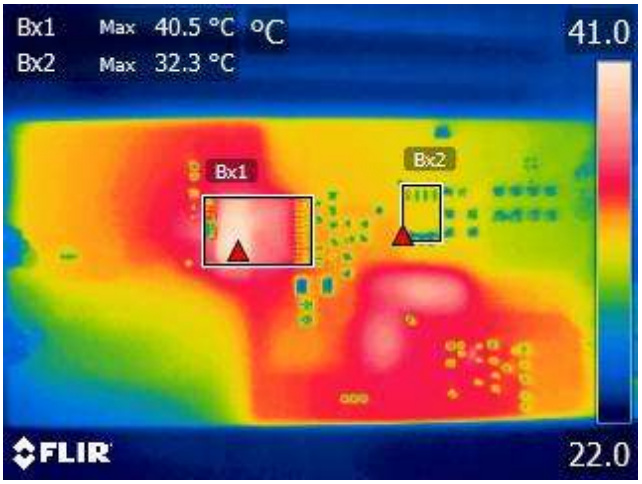


Figure 22 – Solder Side.

	Reference	ºC
Ambient		24.2
Transformer Core	T1	35.0
-4 V Diode	D1005	37.5
17 V Diode	D1006	40.8
-4 V Capacitor	C1009	33.9
17 V Capacitor	C1007	30.1
7.5 V Capacitor	C2005	28.5

	Reference	ºC
Ambient		24.2
InnoSwitch	IC1000A	40.5
7.5 V SRFET	Q2000	32.3

11.1.6 Input: 530 VDC; Output: 7.5 V / 1.3 A, 17 V / 140 mA, -4 V 140 mA

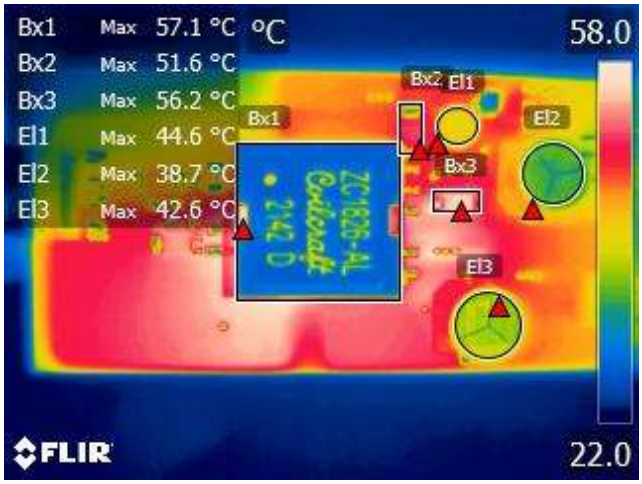


Figure 23 – Component Side.

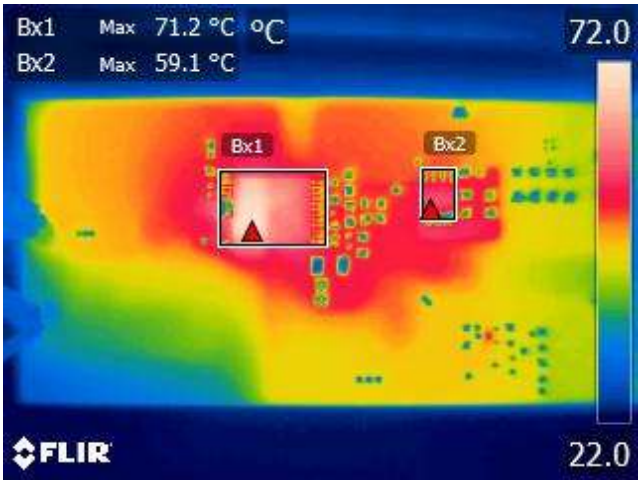


Figure 24 – Solder Side.

	Reference	°C
Ambient		25.1
Transformer Core	T1	57.1
-4 V Diode	D1005	51.6
17 V Diode	D1006	56.2
-4 V Capacitor	C1009	44.6
17 V Capacitor	C1007	38.7
7.5 V Capacitor	C2005	42.6

	Reference	°C
Ambient		25.1
InnoSwitch	IC1000A	71.2
7.5 V SRFET	Q2000	59.1

12 Waveforms

12.1 *Output Voltage Start-Up Waveforms*

Supply is able to start-up at full load and 40 V input.

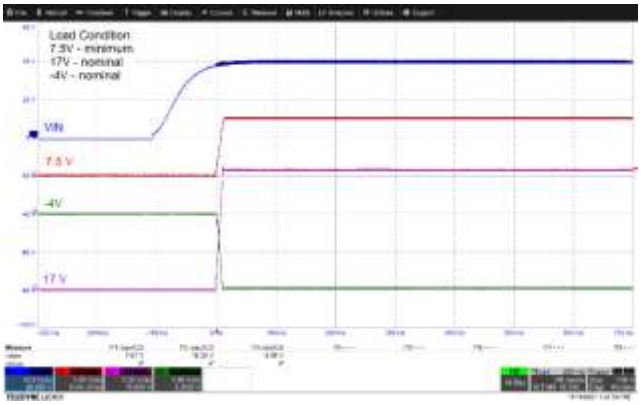


Figure 25 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

Time per Division: 100 ms / div.
CH1, V_{INPUT}, 20 V / div.
CH2, $V_{OUT\_7.5V}$, 5 V / div.
CH3, V_{OUT_17V}, 5 V / div.
CH4, V_{OUT_-4V}, 2 V / div.

$V_{OUT\_7.5V}$ (Maximum): 7.67 V.
V_{OUT_17V} (Maximum): 16.2 V.
V_{OUT_-4V} (Maximum): -3.98 V.

Figure 26 – Input: 40 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

Time per Division: 100 ms / div.
CH1, V_{INPUT}, 20 V / div.
CH2, $V_{OUT\_7.5V}$, 5 V / div.
CH3, V_{OUT_17V}, 5 V / div.
CH4, V_{OUT_-4V}, 2 V / div.

$V_{OUT\_7.5V}$ (Maximum): 7.72 V.
V_{OUT_17V} (Maximum): 16.69 V.
V_{OUT_-4V} (Maximum): -3.99 V.

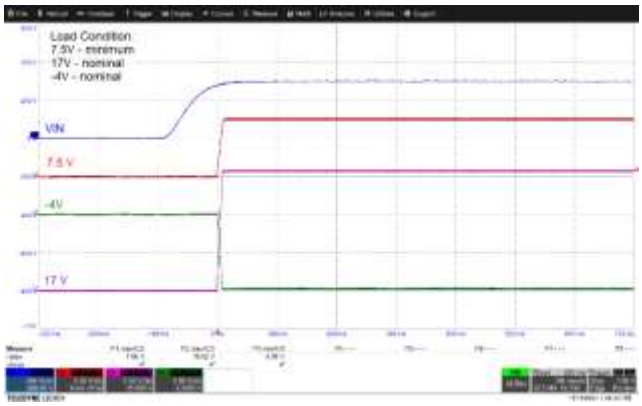


Figure 27 – Input: 300 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

Time per Division: 100 ms / div.
CH1, V_{INPUT}, 200 V / div.
CH2, $V_{OUT\_7.5V}$, 5 V / div.
CH3, V_{OUT_17V}, 5 V / div.
CH4, V_{OUT_-4V}, 2 V / div.

$V_{OUT\_7.5V}$ (Maximum): 7.66 V.
V_{OUT_17V} (Maximum): 16.02 V.

Figure 28 – Input: 300 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

Time per Division: 100 ms / div.
CH1, V_{INPUT}, 200 V / div.
CH2, $V_{OUT\_7.5V}$, 5 V / div.
CH3, V_{OUT_17V}, 5 V / div.
CH4, V_{OUT_-4V}, 2 V / div.

$V_{OUT\_7.5V}$ (Maximum): 7.72 V.
V_{OUT_17V} (Maximum): 16.69 V.

V_{OUT_-4V} (Maximum): - 3.96 V.

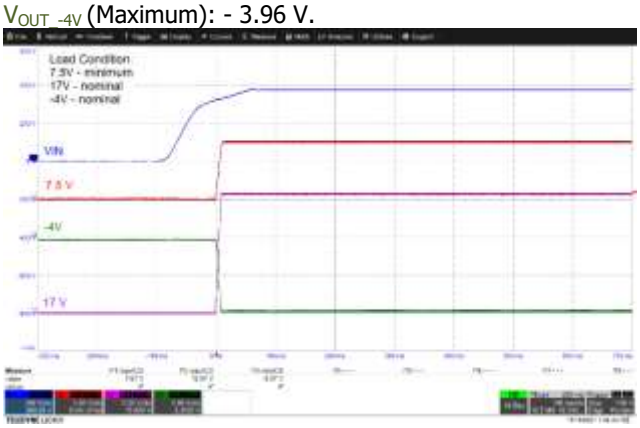


Figure 29 – Input: 375 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

Time per Division: 100 ms / div.
CH1, V_{INPUT}, 200 V / div.
CH2, $V_{OUT\_7.5V}$, 5 V / div.
CH3, V_{OUT_17V}, 5 V / div.
CH4, V_{OUT_-4V}, 2 V / div.

$V_{OUT\_7.5V}$ (Maximum): 7.67 V.
V_{OUT_17V} (Maximum): 15.97 V.
V_{OUT_-4V} (Maximum): -3.97 V.

V_{OUT_-4V} (Maximum): - 3.99 V.

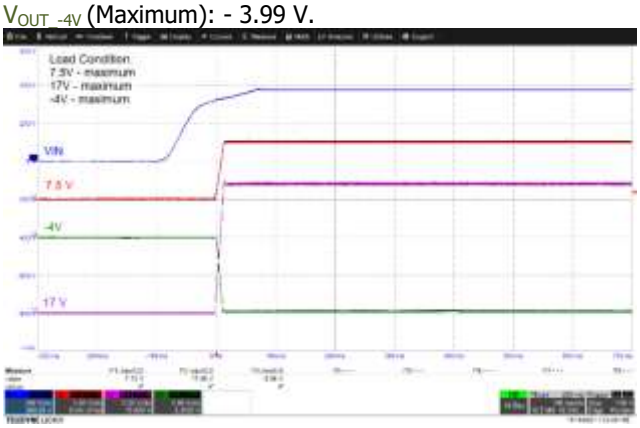


Figure 30 – Input: 375 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

Time per Division: 100 ms / div.
CH1, V_{INPUT}, 200 V / div.
CH2, $V_{OUT\_7.5V}$, 5 V / div.
CH3, V_{OUT_17V}, 5 V / div.
CH4, V_{OUT_-4V}, 2 V / div.

$V_{OUT\_7.5V}$ (Maximum): 7.73 V.
V_{OUT_17V} (Maximum): 17.46 V.
V_{OUT_-4V} (Maximum): -3.96 V.

Figure 31 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

Time per Division: 100 ms / div.
CH1, V_{INPUT}, 200 V / div.
CH2, $V_{OUT\_7.5V}$, 5 V / div.
CH3, V_{OUT_17V}, 5 V / div.
CH4, V_{OUT_-4V}, 2 V / div.

$V_{OUT\_7.5V}$ (Maximum): 7.69 V.
V_{OUT_17V} (Maximum): 15.89 V.
V_{OUT_-4V} (Maximum): -3.95 V.

Figure 32 – Input: 530 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

Time per Division: 100 ms / div.
CH1, V_{INPUT}, 200 V / div.
CH2, $V_{OUT\_7.5V}$, 5 V / div.
CH3, V_{OUT_17V}, 5 V / div.
CH4, V_{OUT_-4V}, 2 V / div.

$V_{OUT\_7.5V}$ (Maximum): 7.75 V.
V_{OUT_17V} (Maximum): 17.42 V.
V_{OUT_-4V} (Maximum): -3.98 V.

12.2 *Load Transient Response*

12.2.1 Fix Load at 7.5 V; Transient Loading at 17 V and -4 V

Figure 33 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 20 mA – 120 mA @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 500 mV / div., -16.235 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.72 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.577 V.
$V_{OUT\_7.5V}$ (Minimum): 7.486 V.
V_{OUT_17V} (Maximum): 16.189 V.
V_{OUT_17V} (Minimum): 15.697 V.
V_{OUT_-4V} (Maximum): -4.0481 V.
V_{OUT_-4V} (Minimum): -3.8798 V.

Figure 34 – Input: 40 VDC; 7.5 V Load: 1.13 A; 17 V and -4 V Load: 20 mA – 120 mA @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.23 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -18.035 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.72 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.51 V.
$V_{OUT\_7.5V}$ (Minimum): 7.361 V.
V_{OUT_17V} (Maximum): 17.648 V.
V_{OUT_17V} (Minimum): 16.545 V.
V_{OUT_-4V} (Maximum): -4.0639 V.
V_{OUT_-4V} (Minimum): -3.932 V.

Figure 35 – Input: 300 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 20 mA – 120 mA @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 500 mV / div., -16.235 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.72 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.573 V.
$V_{OUT\_7.5V}$ (Minimum): 7.495 V.
V_{OUT_17V} (Maximum): 16.244 V.
V_{OUT_17V} (Minimum): 15.620 V.
V_{OUT_-4V} (Maximum): -4.0485 V.
V_{OUT_-4V} (Minimum): -3.8638 V.

Figure 36 – Input: 300 VDC; 7.5 V Load: 1.13 A; 17 V and -4 V Load: 20 mA – 120 mA @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.23 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -18.035 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.72 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.693 V.
$V_{OUT\_7.5V}$ (Minimum): 7.511 V.
V_{OUT_17V} (Maximum): 18.145 V.
V_{OUT_17V} (Minimum): 16.938 V.
V_{OUT_-4V} (Maximum): -4.0659 V.
V_{OUT_-4V} (Minimum): -3.9251 V.

Figure 37 – Input: 375 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 20 mA – 120 mA @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 500 mV / div., -16.235 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.72 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.586 V.
$V_{OUT\_7.5V}$ (Minimum): 7.494 V.
V_{OUT_17V} (Maximum): 16.263 V.
V_{OUT_17V} (Minimum): 15.606 V.
V_{OUT_-4V} (Maximum): -4.0522 V.
V_{OUT_-4V} (Minimum): -3.8588 V.

Figure 38 – Input: 375 VDC; 7.5 V Load: 1.13 A; 17 V and -4 V Load: 20 mA – 120 mA @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.23 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -18.035 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.72 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.693 V.
$V_{OUT\_7.5V}$ (Minimum): 7.515 V.
V_{OUT_17V} (Maximum): 18.247 V.
V_{OUT_17V} (Minimum): 16.945 V.
V_{OUT_-4V} (Maximum): -4.0614 V.
V_{OUT_-4V} (Minimum): -3.8925 V.

Figure 39 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 20 mA – 120 mA @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 500 mV / div., -16.235 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.72 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.601 V.
$V_{OUT\_7.5V}$ (Minimum): 7.478 V.
V_{OUT_17V} (Maximum): 16.314 V.
V_{OUT_17V} (Minimum): 15.603 V.
V_{OUT_-4V} (Maximum): -4.0608 V.
V_{OUT_-4V} (Minimum): -3.855 V.

Figure 40 – Input: 530 VDC; 7.5 V Load: 1.13 A; 17 V and -4 V Load: 20 mA – 120 mA @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.23 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -18.035 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.72 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.709 V.
$V_{OUT\_7.5V}$ (Minimum): 7.527 V.
V_{OUT_17V} (Maximum): 18.48 V.
V_{OUT_17V} (Minimum): 16.99 V.
V_{OUT_-4V} (Maximum): -4.0742 V.
V_{OUT_-4V} (Minimum): -3.8733 V.

12.2.2 Fix Load at 17 V and -4 V; Transient loading at 7.5 V

Figure 41 – Input: 40 VDC; 17 V and -4 V Load: 20 mA; 7.5 V Load: 65 mA – 1.13 A @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -17.67 V Offset.
CH4, V_{OUT_-4V}, 50 mV / div., 3.908 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.61 V.
$V_{OUT\_7.5V}$ (Minimum): 7.342 V.
V_{OUT_17V} (Maximum): 17.701 V.
V_{OUT_17V} (Minimum): 16.167 V.
V_{OUT_-4V} (Maximum): -4.0638 V.
V_{OUT_-4V} (Minimum): -4.0111 V.

Figure 42 – Input: 40 VDC; 17 V and -4 V Load: 120 mA; 7.5 V Load: 65 mA – 1.13 A @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -16.63 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.648 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.576 V.
$V_{OUT\_7.5V}$ (Minimum): 7.289 V.
V_{OUT_17V} (Maximum): 16.619 V.
V_{OUT_17V} (Minimum): 15.711 V.
V_{OUT_-4V} (Maximum): -3.9625 V.
V_{OUT_-4V} (Minimum): -3.8691 V.

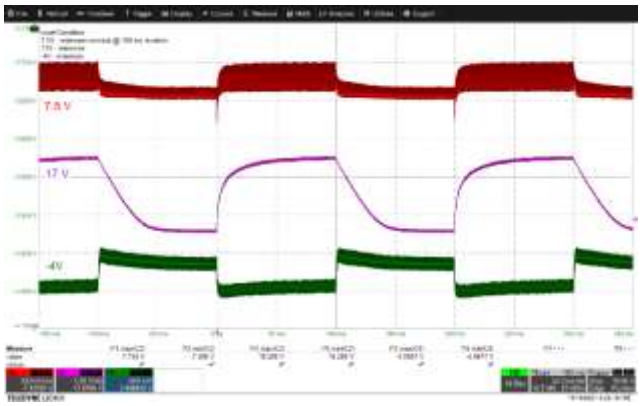


Figure 43 – Input: 300 VDC; 17 V and -4 V Load: 20 mA; 7.5 V Load: 65 mA – 1.13 A @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -17.67 V Offset.
CH4, V_{OUT_-4V}, 50 mV / div., 3.908 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.734 V.
$V_{OUT\_7.5V}$ (Minimum): 7.386 V.
V_{OUT_17V} (Maximum): 18.2 V.
V_{OUT_17V} (Minimum): 16.209 V.
V_{OUT_-4V} (Maximum): -4.0677 V.
V_{OUT_-4V} (Minimum): -4.0007 V.

Figure 44 – Input: 300 VDC; 17 V and -4 V Load: 120 mA; 7.5 V Load: 65 mA – 1.13 A @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -16.63 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.648 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.672 V.
$V_{OUT\_7.5V}$ (Minimum): 7.352 V.
V_{OUT_17V} (Maximum): 17.011 V.
V_{OUT_17V} (Minimum): 15.641 V.
V_{OUT_-4V} (Maximum): -3.9713 V.
V_{OUT_-4V} (Minimum): -3.7906 V.

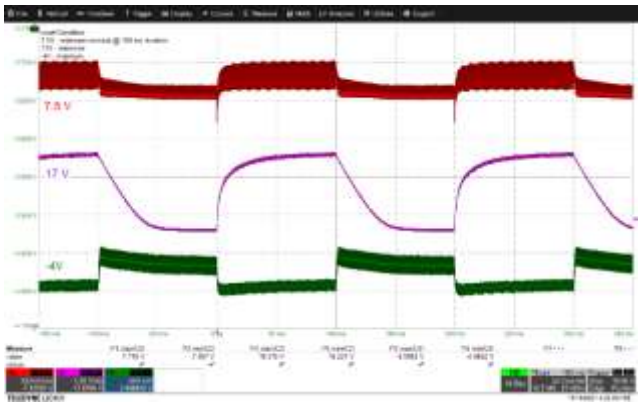


Figure 45 – Input: 375 VDC; 17 V and -4 V Load: 20 mA; 7.5 V Load: 65 mA – 1.13 A @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -17.67 V Offset.
CH4, V_{OUT_-4V}, 50 mV / div., 3.908 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.718 V.
$V_{OUT\_7.5V}$ (Minimum): 7.387 V.
V_{OUT_17V} (Maximum): 18.315 V.
V_{OUT_17V} (Minimum): 16.231 V.
V_{OUT_-4V} (Maximum): -4.0652 V.
V_{OUT_-4V} (Minimum): -3.9983 V.

Figure 46 – Input: 375 VDC; 17 V and -4 V Load: 120 mA; 7.5 V Load: 65 mA – 1.13 A @ 100 ms duration with 100 ms / µA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -16.63 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.648 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.676 V.
$V_{OUT\_7.5V}$ (Minimum): 7.375 V.
V_{OUT_17V} (Maximum): 17.067 V.
V_{OUT_17V} (Minimum): 15.623 V.
V_{OUT_-4V} (Maximum): -3.9624 V.
V_{OUT_-4V} (Minimum): -3.79 V.

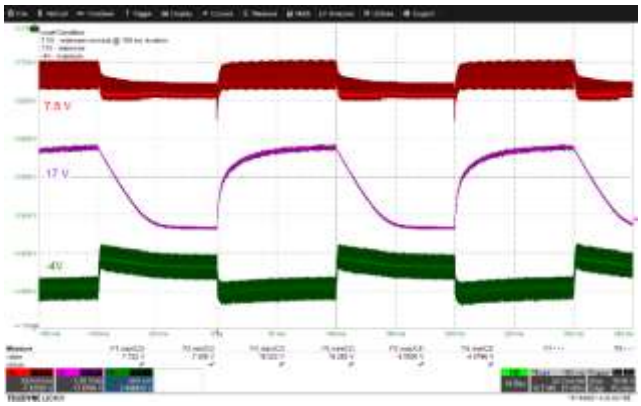


Figure 47 – Input: 530 VDC; 17 V and -4 V Load: 20 mA; 7.5 V Load: 65 mA – 1.13 A @ 100 ms duration with 100 ms / μA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -17.67 V Offset.
CH4, V_{OUT_-4V}, 50 mV / div., 3.908 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.722 V.
$V_{OUT\_7.5V}$ (Minimum): 7.396 V.
V_{OUT_17V} (Maximum): 18.523 V.
V_{OUT_17V} (Minimum): 16.285 V.
V_{OUT_-4V} (Maximum): -4.0766 V.
V_{OUT_-4V} (Minimum): -3.9959 V.

Figure 48 – Input: 530 VDC; 17 V and -4 V Load: 120 mA; 7.5 V Load: 65 mA – 1.13 A @ 100 ms duration with 100 ms / μA slew rate.

Time per Division: 50 ms / div.
CH2, $V_{OUT\_7.5V}$, 200 mV / div., -7.105 V Offset.
CH3, V_{OUT_17V}, 1 V / div., -16.63 V Offset.
CH4, V_{OUT_-4V}, 100 mV / div., 3.648 V Offset.

$V_{OUT\_7.5V}$ (Maximum): 7.687 V.
$V_{OUT\_7.5V}$ (Minimum): 7.372 V.
V_{OUT_17V} (Maximum): 17.162 V.
V_{OUT_17V} (Minimum): 15.617 V.
V_{OUT_-4V} (Maximum): -3.9746 V.
V_{OUT_-4V} (Minimum): -3.801 V.

12.3 *InnoSwitch3-AQ Waveforms*

12.3.1 Start-Up Waveforms

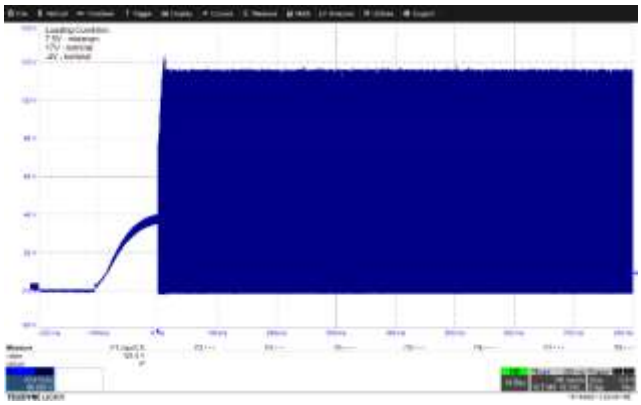


Figure 49 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 20 V / div., 100 ms / div.
V_{DS} (Maximum): 124.4 V.
Derating: 13.82 %.

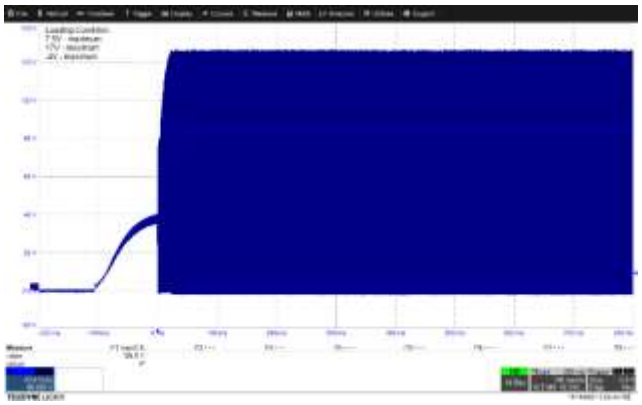


Figure 50 – Input: 40 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 20 V / div., 100 ms / div.
V_{DS} (Maximum): 126.8 V.
Derating: 14.09 %.

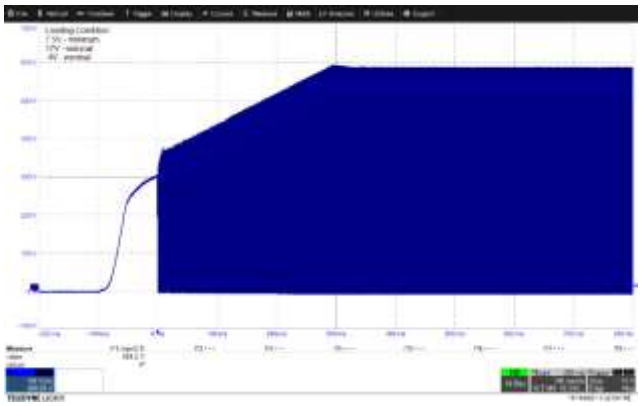


Figure 51 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 100 V / div., 100 ms / div.
V_{DS} (Maximum): 593.2 V.
Derating: 65.91 %.

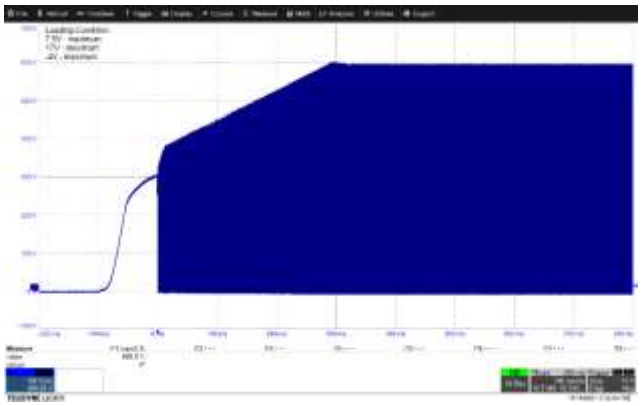


Figure 52 – Input: 530 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 100 V / div., 100 ms / div.
V_{DS} (Maximum): 600.8 V.
Derating: 66.76 %.

12.3.2 Steady-State Waveforms

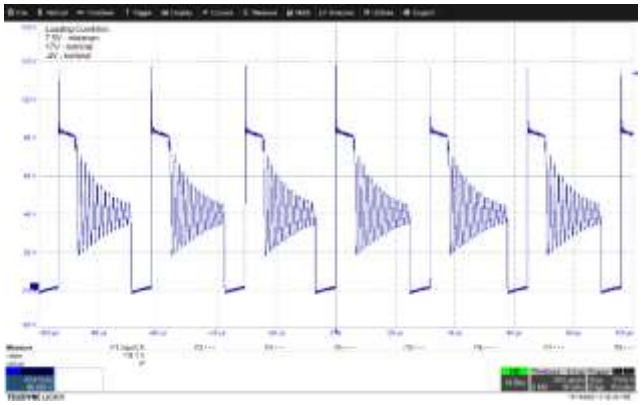


Figure 53 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 20 V / div., 20 µs / div.
V_{DS} (Maximum): 118.1 V.
Derating: 13.12 %.

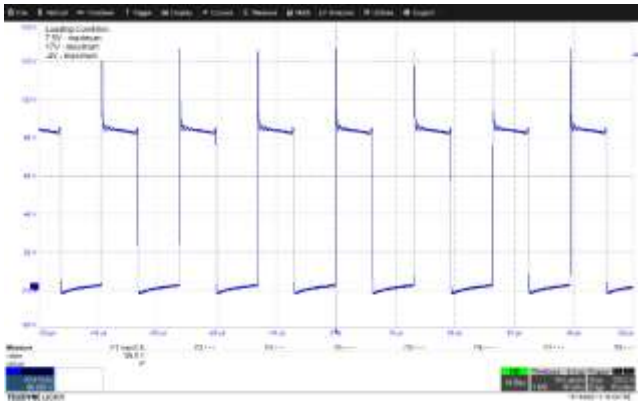


Figure 54 – Input: 40 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 20 V / div., 10 µs / div.
V_{DS} (Maximum): 126.8 V.
Derating: 14.09 %.

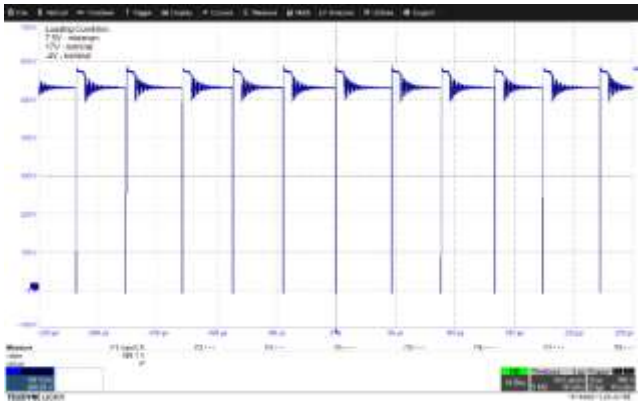


Figure 55 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 100 V / div., 50 µs / div.
V_{DS} (Maximum): 589.1 V.
Derating: 65.46 %.

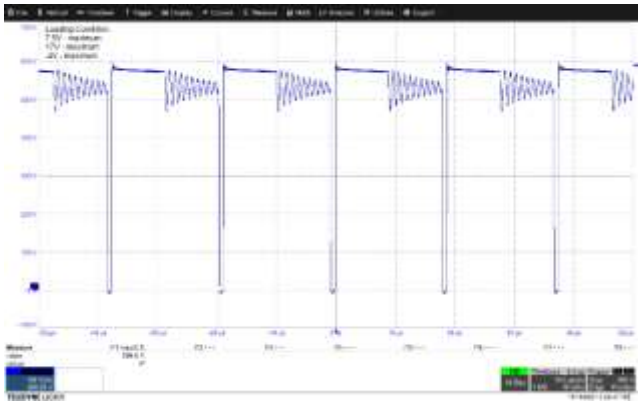


Figure 56 – Input: 530 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 100 V / div., 10 µs / div.
V_{DS} (Maximum): 596.6 V.
Derating: 66.29 %.

12.4 *SR FET Waveforms*

12.4.1 Start-Up Waveforms

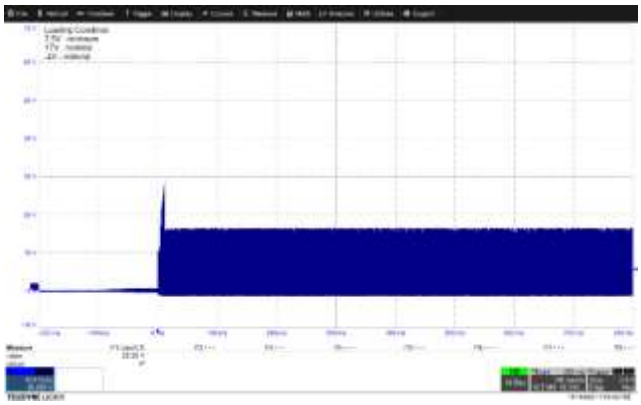


Figure 57 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 10 V / div., 100 ms / div.
V_{DS} (Maximum): 29.28 V.
Derating: 14.64 %.

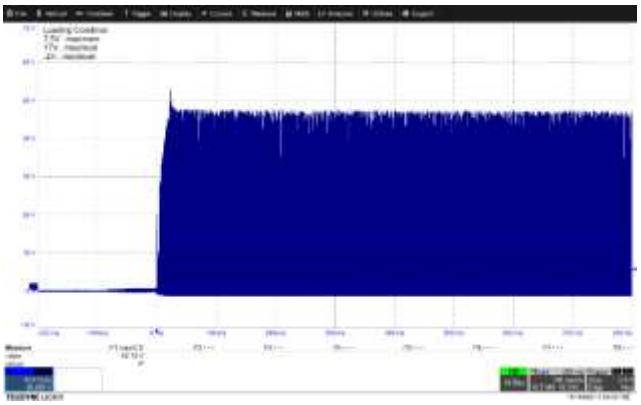


Figure 58 – Input: 40 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 10 V / div., 100 ms / div.
V_{DS} (Maximum): 53.74 V.
Derating: 26.87 %.

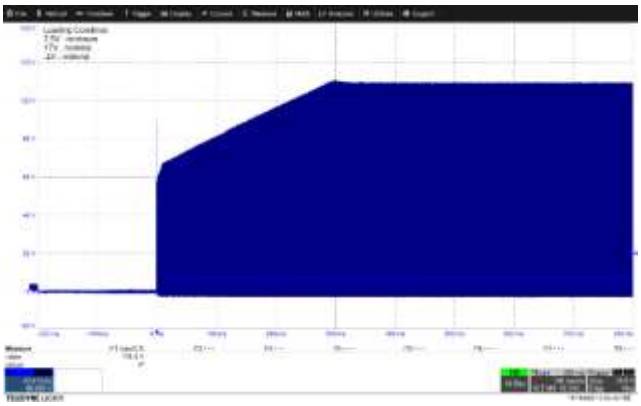


Figure 59 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 20 V / div., 100 ms / div.
V_{DS} (Maximum): 110.4 V.
Derating: 55.2 %.

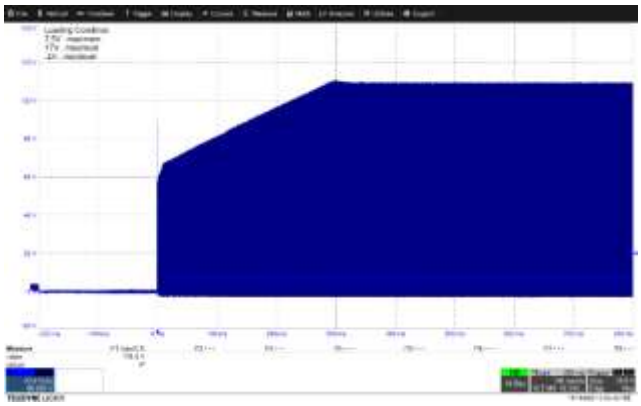


Figure 60 – Input: 530 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 2s0 V / div., 100 ms / div.
V_{DS} (Maximum): 110.4 V.
Derating: 55.2 %.

12.4.2 Steady-State Waveforms

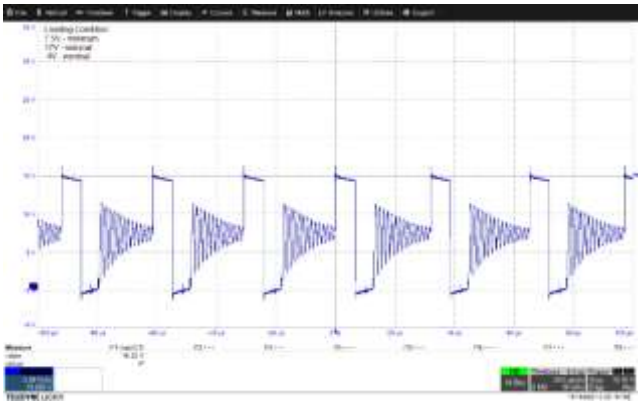


Figure 61 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 5 V / div., 20 µs / div.
V_{DS} (Maximum): 16.32 V.
Derating: 8.16 %.

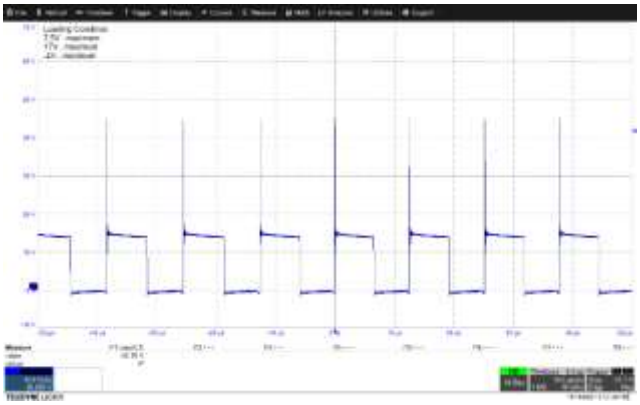


Figure 62 – Input: 40 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 10 V / div., 10 µs / div.
V_{DS} (Maximum): 45.18 V.
Derating: 22.59 %.

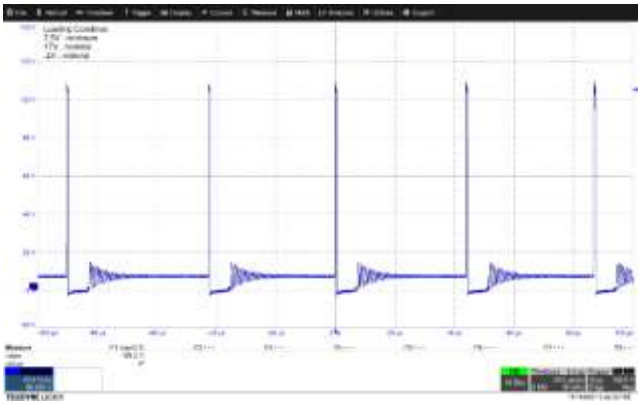


Figure 63 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 20 V / div., 20 µs / div.
V_{DS} (Maximum): 109.2 V.
Derating: 54.6 %.

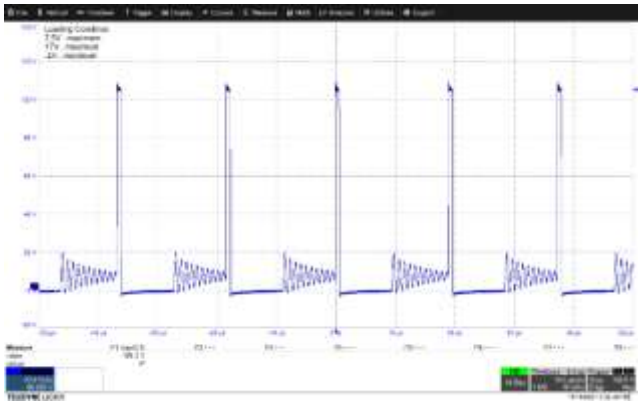


Figure 64 – Input: 530 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 20 V / div., 10 µs / div.
V_{DS} (Maximum): 109.3 V.
Derating: 54.65%.

12.5 *17 V Diode Waveforms*

12.5.1 Start-Up Waveforms

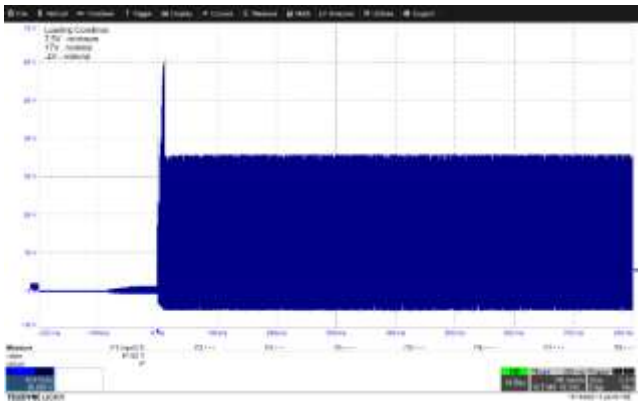


Figure 65 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 10 V / div., 100 ms / div.
V_{DS} (Maximum): 61.62 V.
Derating: 15.41 %.

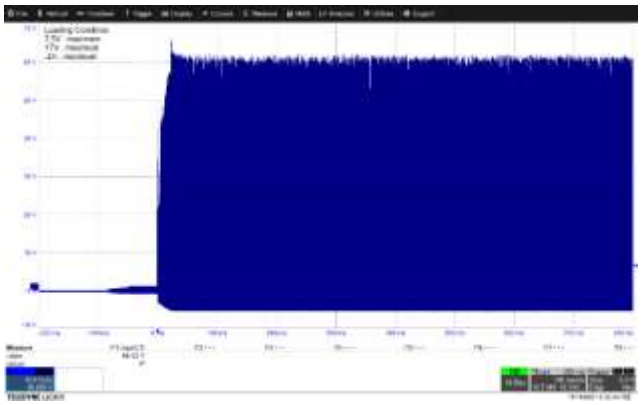


Figure 66 – Input: 40 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 10 V / div., 100 ms / div.
V_{DS} (Maximum): 66.52 V.
Derating: 16.63 %.

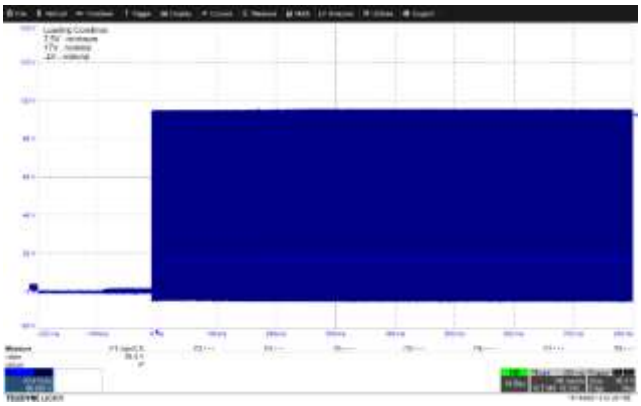


Figure 67 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 20 V / div., 100 ms / div.
V_{DS} (Maximum): 95.4 V.
Derating: 23.85 %.

Figure 68 – Input: 530 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 2s0 V / div., 100 ms / div.
V_{DS} (Maximum): 95.4 V.
Derating: 23.85 %.

12.5.2 Steady-State Waveforms

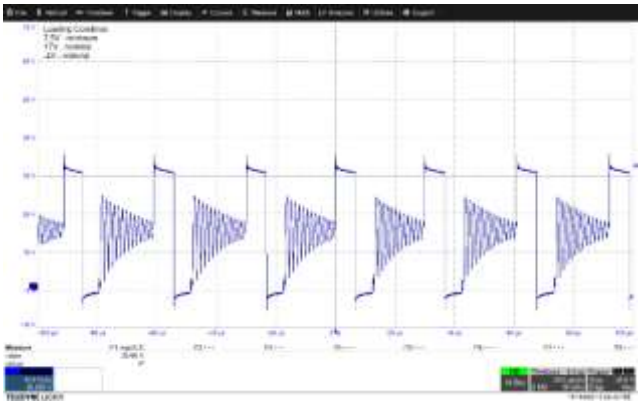


Figure 69 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 10 V / div., 20 µs / div.
V_{DS} (Maximum): 35.66 V.
Derating: 8.92 %.

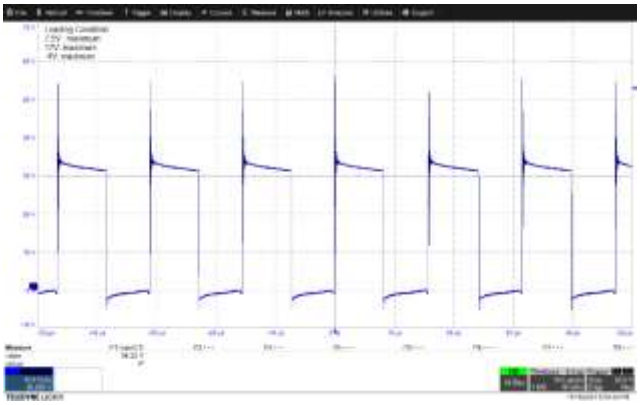


Figure 70 – Input: 40 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 10 V / div., 10 µs / div.
V_{DS} (Maximum): 56.22 V.
Derating: 14.01 %.

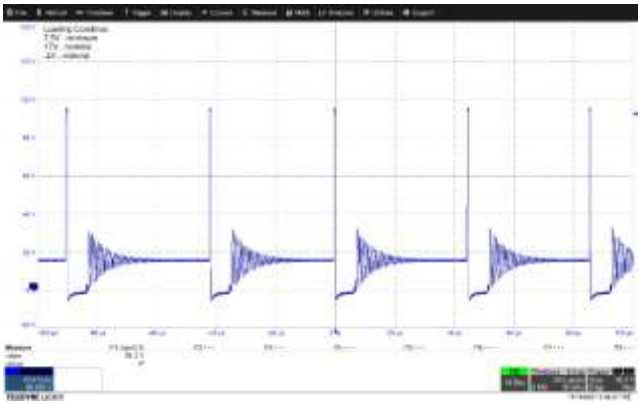


Figure 71 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 20 V / div., 20 µs / div.
V_{DS} (Maximum): 95.3 V.
Derating: 23.82 %.

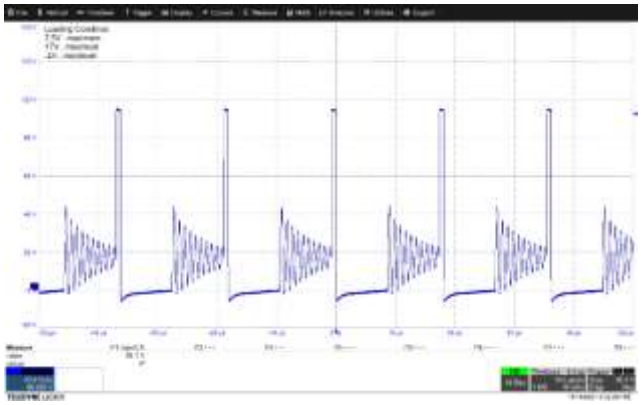


Figure 72 – Input: 530 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 20 V / div., 10 µs / div.
V_{DS} (Maximum): 95.1 V.
Derating: 23.78 %.

12.6 *-4 V Diode Waveforms*

12.6.1 Start-Up Waveforms

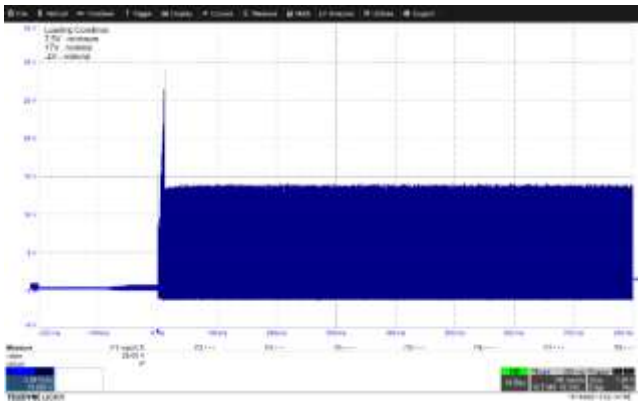


Figure 73 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 5 V / div., 100 ms / div.
V_{DS} (Maximum): 29.09 V.
Derating: 14.55 %.

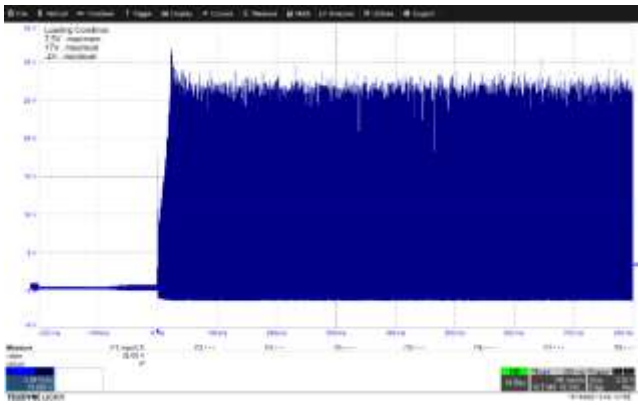


Figure 74 – Input: 40 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 5 V / div., 100 ms / div.
V_{DS} (Maximum): 32.08 V.
Derating: 16.04 %.

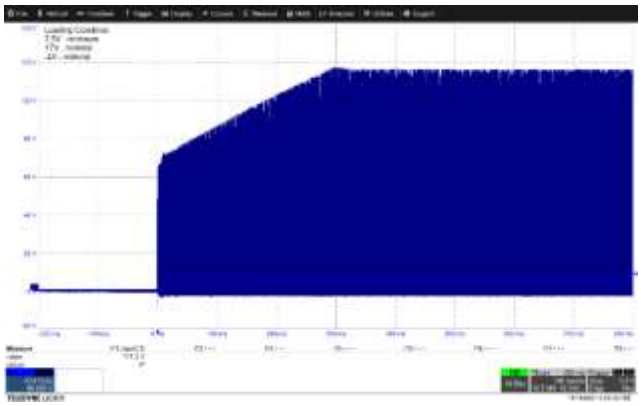


Figure 75 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 20 V / div., 100 ms / div.
V_{DS} (Maximum): 117.3 V.
Derating: 58.65 %.

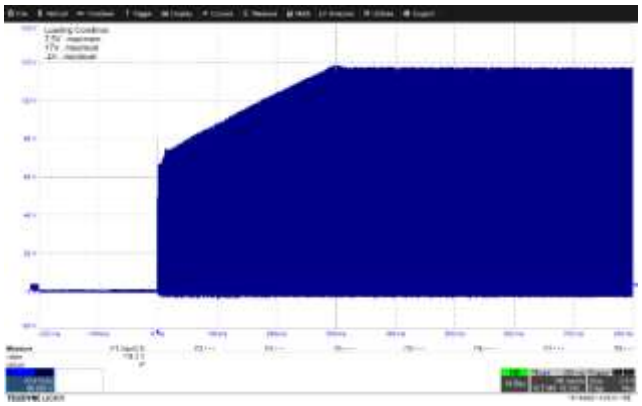


Figure 76 – Input: 530 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 20 V / div., 100 ms / div.
V_{DS} (Maximum): 118.3 V.
Derating: 59.15 %.

12.6.2 Steady-State Waveforms

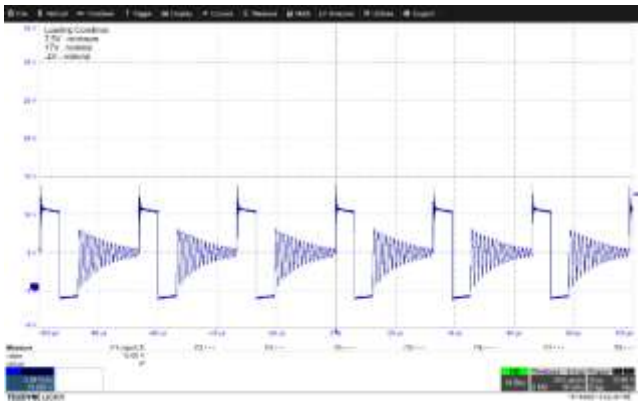


Figure 77 – Input: 40 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 10 V / div., 20 µs / div.
V_{DS} (Maximum): 14 V.
Derating: 7 %.

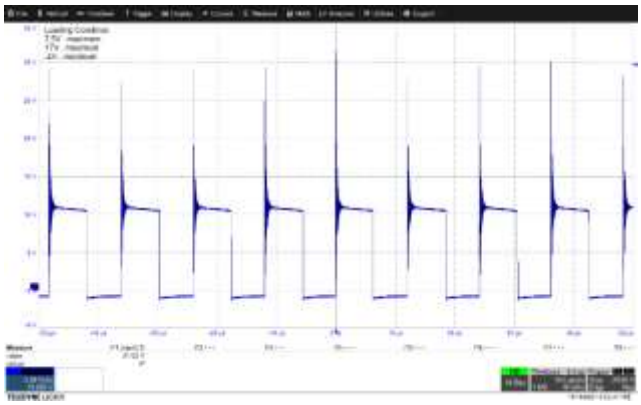


Figure 78 – Input: 40 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 5 V / div., 10 µs / div.
V_{DS} (Maximum): 31.52 V.
Derating: 15.76 %.

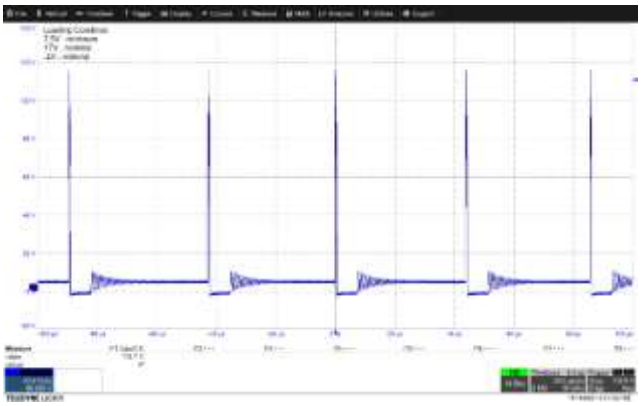


Figure 79 – Input: 530 VDC; 7.5 V Load: 65 mA; 17 V and -4 V Load: 120 mA.

CH1, V_{DS}, 20 V / div., 20 µs / div.
V_{DS} (Maximum): 115.7 V.
Derating: 57.85 %.

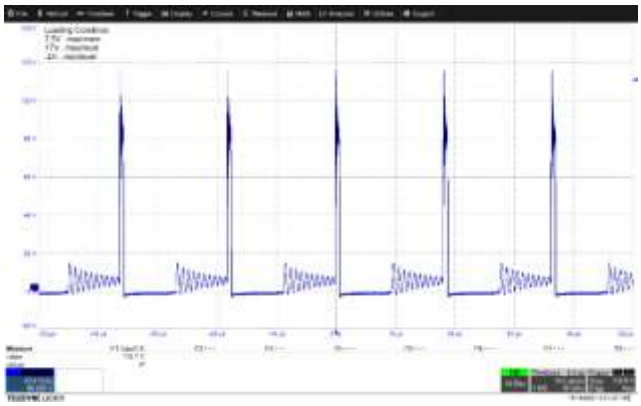
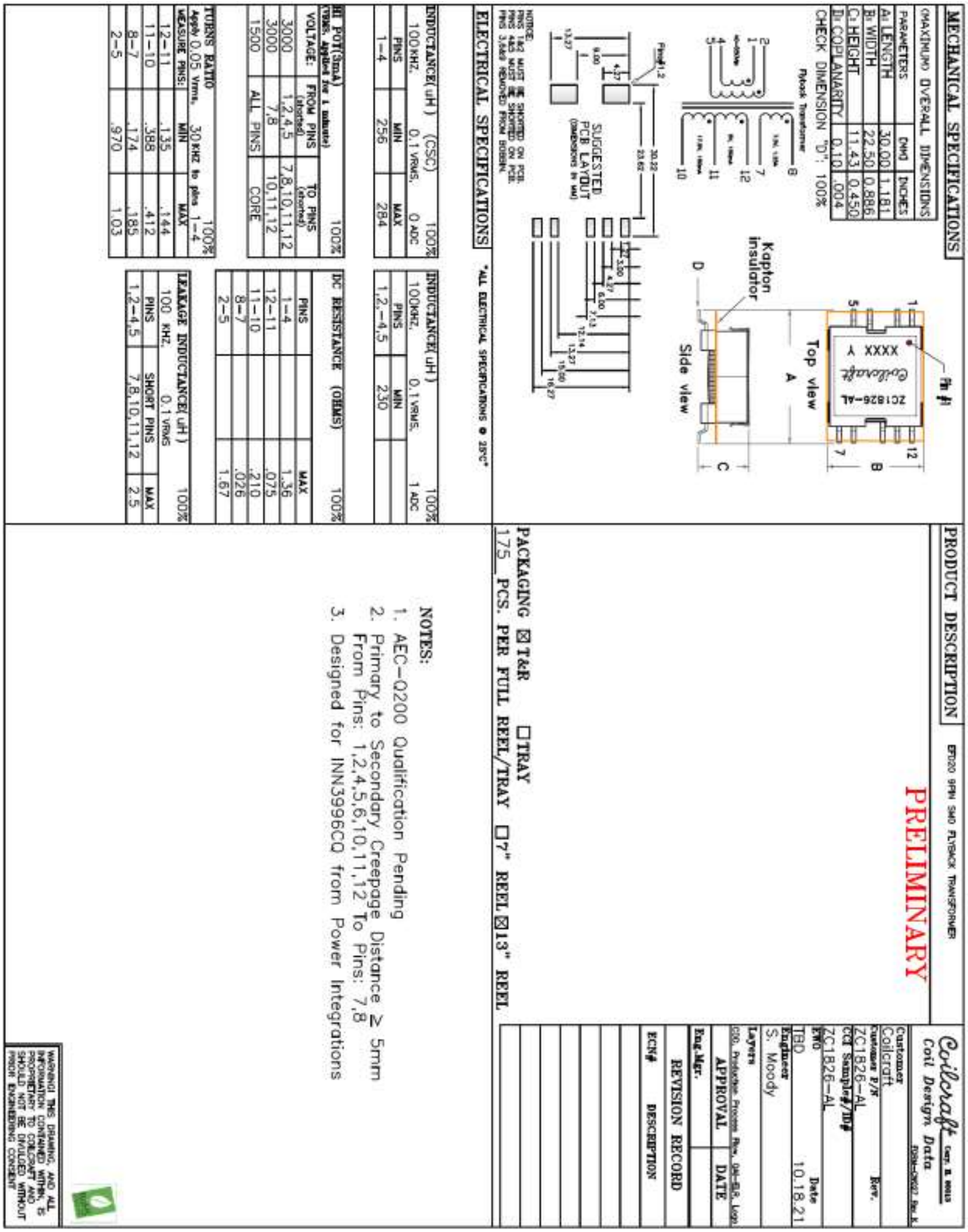


Figure 80 – Input: 530 VDC; 7.5 V Load: 1.3 A; 17 V and -4 V Load: 140 mA.

CH1, V_{DS}, 20 V / div., 10 µs / div.
V_{DS} (Maximum): 115.7 V.
Derating: 57.85 %.

13 Appendix A – CoilCraft Transformer Datasheet



MECHANICAL SPECIFICATIONS

(MAXIMUM) OVERALL DIMENSIONS

PARAMETERS	(MM)	INCHES
A: LENGTH	30.00	1.181
B: WIDTH	22.50	0.886
C: HEIGHT	11.43	0.450
D: COPLANARITY	0.10	.004

CHECK DIMENSION "D": 100%

NOTICE:
PINS 1&2 MUST BE SHORTED ON PCB.
PINS 4&5 MUST BE SHORTED ON PCB.
PINS 3,6&9 REMOVED FROM BOBBIN.

ELECTRICAL SPECIFICATIONS "ALL ELECTRICAL SPECIFICATIONS @ 25°C"

INDUCTANCE(uH) (CSC) 100% — 100KHZ, 0.1 VRMS, 0 ADC

PINS	MIN	MAX
1–4	256	284

INDUCTANCE(uH) 100% — 100KHZ, 0.1 VRMS, 1 ADC

PINS	MIN
1,2,–4,5	230

HI POT(3mA) 100% (VRMS, Applied for 1 minute)

VOLTAGE:	FROM PINS (shorted)	TO PINS (shorted)
3000	1,2,4,5	7,8,10,11,12
3000	7,8	10,11,12
1500	ALL PINS	CORE

DC RESISTANCE (OHMS) 100%

PINS		MAX
1–4		1.36
12–11		.075
11–10		.210
8–7		.026
2–5		1.67

TURNS RATIO 100% — Apply 0.05 Vrms, 30 KHZ to pins 1–4

MEASURE PINS:	MIN	MAX
12–11	.135	.144
11–10	.388	.412
8–7	.174	.185
2–5	.970	1.03

LEAKAGE INDUCTANCE(uH) 100% — 100 KHZ, 0.1 VRMS

PINS	SHORT PINS	MAX
1,2–4,5	7,8,10,11,12	2.5

PRODUCT DESCRIPTION EFD20 9PIN SMD FLYBACK TRANSFORMER

PRELIMINARY

PACKAGING ☒ T&R ☐ TRAY
175 PCS. PER FULL REEL/TRAY ☐ 7" REEL ☒ 13" REEL

Coilcraft Coil Design Data

Customer	Coilcraft
Customer P/N	ZC1826–AL
Rev.	
CCI Sample#/ID#	ZC1826–AL
EWO	TBD
Date	10.18.21
Engineer	S. Moody
Layers	COO, Production Process Flow, QAI–ELR, Logo

APPROVAL	DATE
Eng.Mgr.	

REVISION RECORD

ECN#	DESCRIPTION

NOTES:

1. AEC–Q200 Qualification Pending
2. Primary to Secondary Creepage Distance ≥ 5mm From Pins: 1,2,4,5,6,10,11,12 To Pins: 7,8
3. Designed for INN3996CQ from Power Integrations

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
07-Jan-22	JMR	1.0	Initial Release.	Apps & Mktg
10-Mar-22	PV	1.1	Corrected T1 Part Number.	Apps

For the latest updates, visit our website: www.power.com

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