Design Example Report

Title	***10 W CV/CC Charger Using LinkSwitch™-3 LNK6448K***
Specification	90-265 VAC Input; 5 V, 2 A Output
Application	Low-cost Charger or Adapter
Author	Applications Engineering Department
Document Number	DER-403
Date	April 21, 2015
Revision	1.2

Summary and Features

- Revolutionary control concept provides very low cost, low part-count solution
- Primary-side control eliminates secondary-side control and optocoupler
- Provides ±5% constant voltage (CV) and ±10% constant current (CC) accuracy
- Over-temperature protection – accurate tolerance (±5%) with hysteretic recovery for safe PCB temperatures under all conditions
- Auto-restart output short circuit and open-loop protection
- Extended pin creepage distance for reliable operation in humid environments, >3.05 mm at package
- No-load consumption <30 mW at 230 VAC
- Ultra-low leakage current: <5 µA at 265 VAC input (no Y capacitor required)
- Design easily passes EN550022 and CISPR-22 Class B EMI testing with >6 dB margin
- Meets IEC 61000-4-5 Class 3 AC line surge
- Meets IEC 61000-4-2 ESD withstand (contact discharge to ±8 kV and air discharge to ±15 kV)

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a 10 W constant voltage/constant current (CV/CC) universal-input power supply for cell phone or similar charger applications. This reference design is based on the LinkSwitch-3 family product LNK6448K.

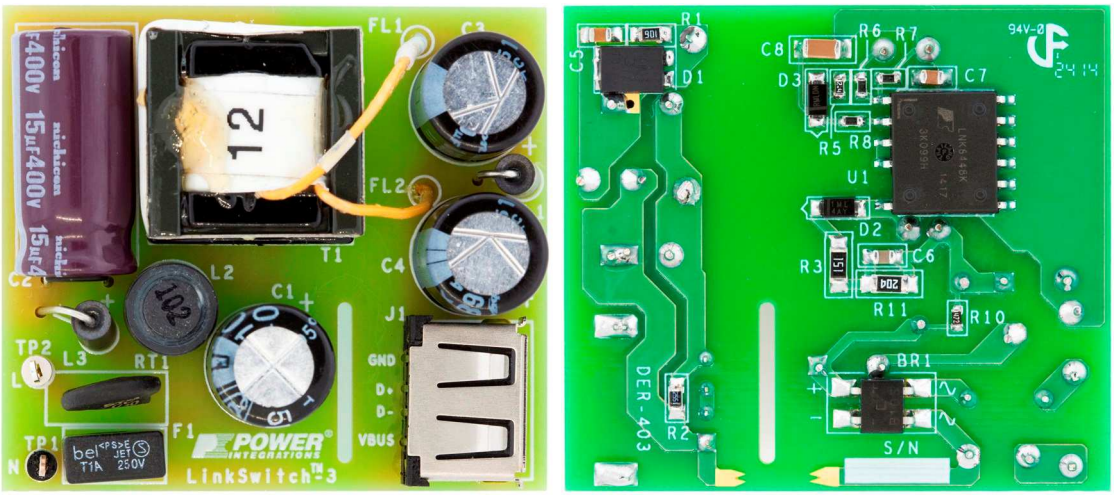

Figure 1 – DER-403 Board Photograph (Top and Bottom).

The LNK6448K was developed to cost effectively replace all existing solutions in low-power charger and adapter applications. Its core controller is optimized for CV/CC charging applications with minimal external parts count and very accurate control of both the output voltage and current, without the use of an optocoupler. The LNK6448K has an integrated 725 V switching MOSFET and ON/OFF control function which together deliver high efficiency under all load conditions and low no-load energy consumption. Both the operating efficiency and no-load performance exceed all current international energy efficiency standards.

The LNK6448K monolithically integrates the 725 V power MOSFET switch and controller. A unique ON/OFF control scheme provides CV regulation. The IC also incorporates accurate regulation over a wide temperature range for enhanced CV control. The switching frequency is modulated to regulate the output current for a linear CC characteristic.

The LNK6448K controller consists of an oscillator, a feedback (sense and logic) circuit, a 5.9 V regulator, BYPASS pin programming functions, over-temperature protection, frequency jittering, a current-limit circuit, leading-edge blanking, a frequency controller for CC regulation, and an ON/OFF state machine for CV control.

The LNK6448K also provides a sophisticated range of protection features including auto-restart for control loop component open/short circuit faults and output short circuit

conditions. Accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions.

The IC package provides extended creepage distance between high and low voltage pins (both at the package and PCB), which is required in highly humid environments to prevent arcing and to further improve reliability.

A external bias winding is required for LNK6448K to supply the current for the controller during switching. When fed from an optional bias supply (as in this design), the no-load power consumption reduces to <30 mW.

The EPC17 transformer bobbin in this design provides extended creepage to meet safety spacing requirements.

This document contains the power supply specifications, schematic, bill of materials, transformer specifications, and typical performance characteristics for this reference design.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power	P_{NL}			30	mW	Measured at V_{IN} = 230 VAC
Output						All measured at end of cable
Output Voltage	V_{OUT}	4.75	5.00	5.25	V	±5%
Output Ripple Voltage	V_{RIPPLE}		150		mV	20 MHz bandwidth
Output Current	I_{OUT}	2			A	±10%
Output Power	P_{OUT}		10		W	
Efficiency						
Average Active Mode	η	76.0			%	115 VAC / 230 VAC, 25 °C
Environmental						
Conducted EMI	Meets CISPR22B / EN55022B					>6 dB margin
Safety	Designed to meet IEC950, UL1950 Class II					
Line Surge						1.2/50 µs surge, IEC 1000-4-5, Series Impedance:
Differential		1			kV	Differential Mode: 2 Ω
Common Mode		2			kV	Common Mode: 12 Ω
ESD	**Air**	-15		15	kV	Air discharge to IEC 61000-4-2
	Contact	-8		8	kV	Contact discharge to IEC 61000-4-2
Ambient Temperature	T_{AMB}	0		40	°C	Case external, free convection, sea level

3 Schematic

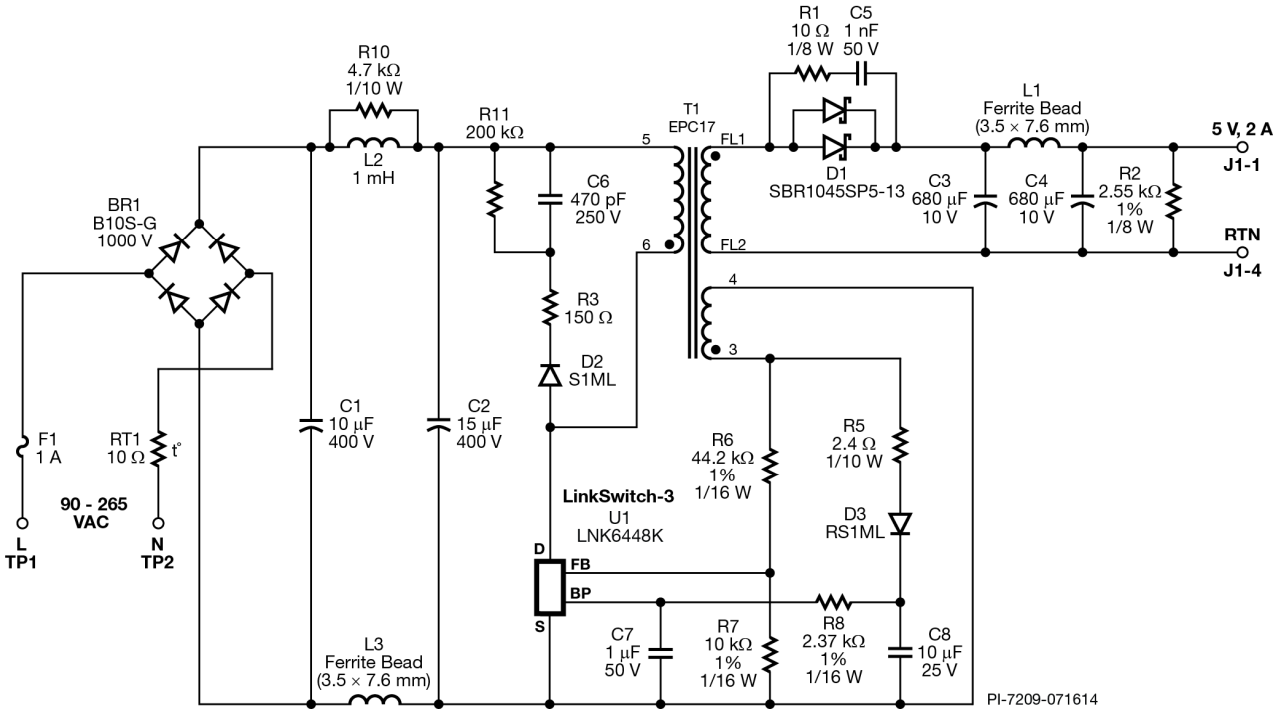

Figure 2 – Schematic.

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4 Circuit Description

This circuit uses the LNK6448K in a primary-side regulated flyback power-supply configuration.

4.1 Input Filter

The AC input power is rectified by BR1. The rectified DC is filtered by the bulk storage capacitors C1 and C2. Inductor L2 and ferrite bead L3, with capacitors C1 and C2, form pi (π) filters to attenuate conducted differential-mode EMI noise. This configuration, along with Power Integrations' transformer E-shield™ technology, allows this design to meet EMI standard EN55022 class B with good margin and without a Y capacitor. The transformer construction also gives very good EMI repeatability. Fuse F1 provides protection against catastrophic failure. It should be rated to withstand the instantaneous dissipation when the supply is first connected to the AC input (while the input capacitors charge) at VAC_{MAX}. The thermistor RT1 limits the peak current when first powering up the power supply and when the initial voltage on the bulk capacitor is 0 V.

4.2 LNK6448K Primary

The LNK6448K device (U1) incorporates the power switching device, oscillator, CV/CC control engine, and start-up and protection functions all on one IC. Its integrated 725 V power MOSFET allows sufficient voltage margins in universal input AC applications, including extended line swells. The device is self-powered from the BYPASS pin via the decoupling capacitor C7. The optional bias circuit consisting of D3, C8, R5, and R8, increases efficiency and reduces no-load input power. The resistor R5 helps to damp the ringing on the bias winding voltage.

The rectified and filtered input voltage is applied to one end of the transformer (T1) primary winding. The other side of the transformer's primary winding is driven by the internal MOSFET of U1. A RCD-R consisting of D2, R3, C6 and R11 limits drain-voltage spikes caused by leakage inductance in the transformer. Resistor R3 has a relatively large value to prevent any excessive ringing on the drain voltage waveform caused by the leakage inductance. Excessive ringing on the bias winding, which reflected from the drain voltage, can increase output ripple by introducing an error in the sampled output voltage. IC U1 samples the feedback winding each cycle, 2.55 μs after turn-off of its internal power MOSFET at full load condition.

4.3 Output Rectification and Filtering

Transformer T1's secondary is rectified by D1, a Schottky barrier-type diode (chosen for higher efficiency), and filtered by C3 and C4. In this application, C3 and C4 have sufficiently low ESR characteristics to allow meeting the output voltage ripple requirement without adding an LC post filter. Resistor R1 and capacitor C5 dampen high-frequency ringing and reduce the voltage stress on D1. Ferrite bead L1 helps to eliminate the high switching noise in the output.

In designs where lower average efficiency is acceptable (by 3% to 4%) D7 may be replaced by a PN-junction to lower cost. In this case, ensure R6 and R7 are re-adjusted as necessary to keep the output voltage centered.

4.4 Output Regulation

The LNK6448K regulates output using ON/OFF control for CV regulation, and frequency control for CC regulation. The output voltage is sensed by a bias winding on the transformer. The feedback resistors (R6 and R7) were selected using standard 1% resistor values to center both the nominal output voltage and constant current regulation thresholds. Resistor R2 provides a minimum load to maintain output regulation when the output is unloaded.

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5 PCB Layout

Notable layout design points are:

1 A spark gap and associated slot in the PCB between the primary and secondary allows successful ESD testing up to ±15 kV.
   - The preferential arcing point routes the energy from ESD discharges back to the AC input, away from the transformer and primary circuitry.
   - The trace connected to the AC input side of the spark gap is spaced away from the rest of the board and its components to prevent arc discharges to other sections of the circuit.

2 The drain trace length has been minimized to reduce EMI.

3 Clamp and output diode loop areas are minimized to reduce EMI.

4 The AC input is located away from switching nodes to minimize noise coupling that may bypass input filtering.

5 Place C7 (the bypass capacitor) as close as possible to the BYPASS pin on U1.

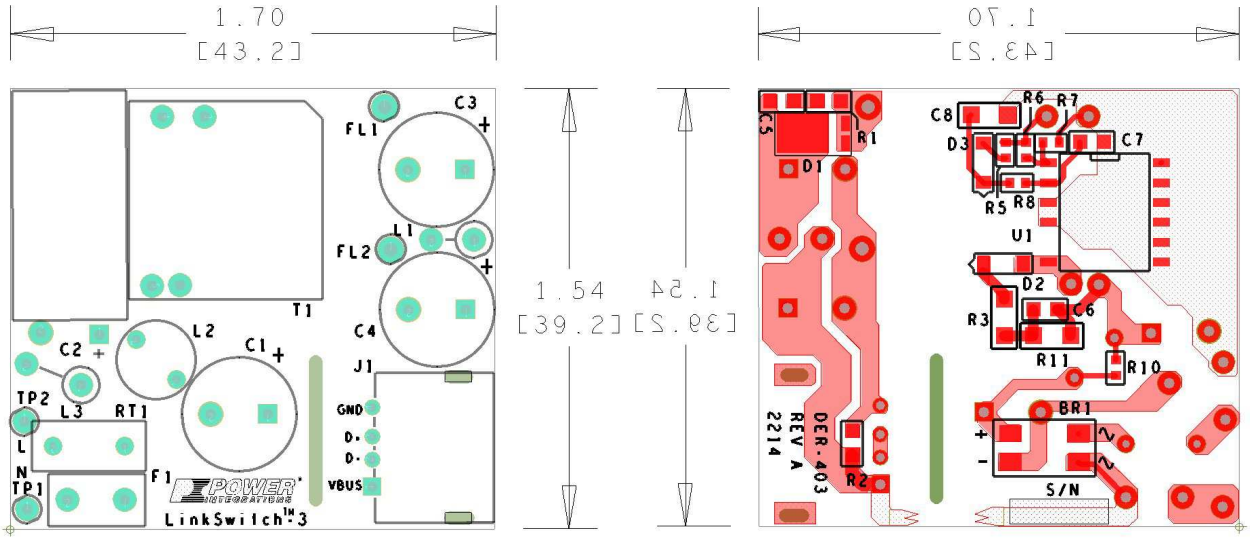

Figure 3 – Printed Circuit Layout. (Top and Bottom).

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg P/N	Manufacturer
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip Tech
2	1	C1	10 µF, 400 V, Electrolytic, Low ESR, 79 mA, (10 x 12.5)	TYD2GM100G13O	Ltec
3	1	C2	15 µF, 400 V, Electrolytic, (10 x 20),	UCY2G150MPD	Nichicon
4	2	C3 C4	680 µF, 10 V, Electrolytic, 20%, (8 x 10.8 mm) 680 µF, 10 V, Electrolytic, 20%, (10 x 12.5 mm)	10AX680M8X10.8 10AX680MEFC10X12.5	Rubycon Rubycon
5	1	C5	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX
6	1	C6	470 pF, 250 V, Ceramic,GCM, 0805	GCM21A7U2E471JX01D	Murata
7	1	C7	1 µF, 50 V, Ceramic, X7R, 0805	C2012X7R1H105M	TDK
8	1	C8	10 µF, 25 V, Ceramic, X7R, 1206	C3216X7R1E106M	TDK
9	1	D1	45 V, 10 A, Schottky, SMD, POWERD15	SBR1045SP5-13	Diodes, Inc.
10	1	D2	1 kV, 1 A, Standard Recovery, SMA	S1ML	Taiwan Semi
11	1	D3	1000 V, 800 mA, Fast Recovery SMF, 5000 ns,	RS1ML	Taiwan Semi
12	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
13	2	FL1 FL2	PCB Terminal Hole, 22 AWG	N/A	N/A
14	1	J1	CONN USB FEMALE TYPE A	USB-AF-DIP-094-H	GOLDCONN
15	2	L1 L3	3.5 mm x 7.6 mm, 75 Ω at 25 MHz, #22 AWG hole, Ferrite Bead	2743004112	Fair-Rite
16	1	L2	1 mH, 0.23 A, Ferrite Core	CTSCH875DF-102K	CT Parts
17	1	R1	10 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
18	1	R2	2.55 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2551V	Panasonic
19	1	R3	150 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ151V	Panasonic
20	1	R5	2.4 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ2R4V	Panasonic
21	1	R6	44.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4422V	Panasonic
22	1	R7	10 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
23	1	R8	2.37 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2371V	Panasonic
24	1	R10	4.7 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ472V	Panasonic
25	1	R11	200 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2003V	Panasonic
26	1	RT1	NTC Thermistor, 10 W, 1.7 A	CL-120	Thermometrics
27	1	T1	Bobbin, EPC17, Horizontal, 10 pins	BEPC-17-1110CPHFR	TDK
28	1	TP1	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
29	1	TP2	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
30	1	U1	LinkSwitch-3, 0%, eSOP	LNK6448K	Power Integrations

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7 Transformer Specification

7.1 Electrical Diagram

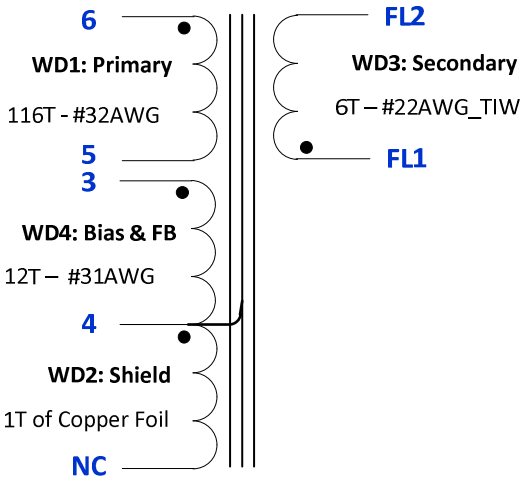

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 3-6 and leads FL1-FL2.	3000 VAC
Primary Inductance	Pins 5-6, all other windings open, measured at 70 kHz, 0.4 V_{RMS}.	1.16 mH ±7%
Resonant Frequency	Pins 5-6, all other windings open.	600 kHz (Min.)
Primary Leakage Inductance	Pins 5-6, with leads FL1-FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	60 µH (Max.)

7.3 Materials

Item	Description
[1]	Core: EPC17, TDK-PC44, or equivalent, and gapped ALG 109.24 nH/T^2
[2]	Bobbin: EPC17-Horizontal, 10 pins (4/6) (1-4: primary, 5-10: secondary); TDK-BEPC17-1110CPHFR.
[3]	Magnet wire: #32 AWG, double coated.
[4]	Magnet wire: #31 AWG, double coated.
[5]	Magnet wire: #22 AWG, Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 9.5 mm wide, 2.0 mils thick.
[7]	Copper foil tape: 2 mils thick.
[8]	Glue: Loctite 409, Industrial Grade Gel, 40904; or equivalent.
[9]	Epoxy: Devcon, 5 min epoxy, No 14210; or equivalent.
[10]	Varnish: Dolph BC-359; or equivalent.

7.4 Transformer Build Diagram

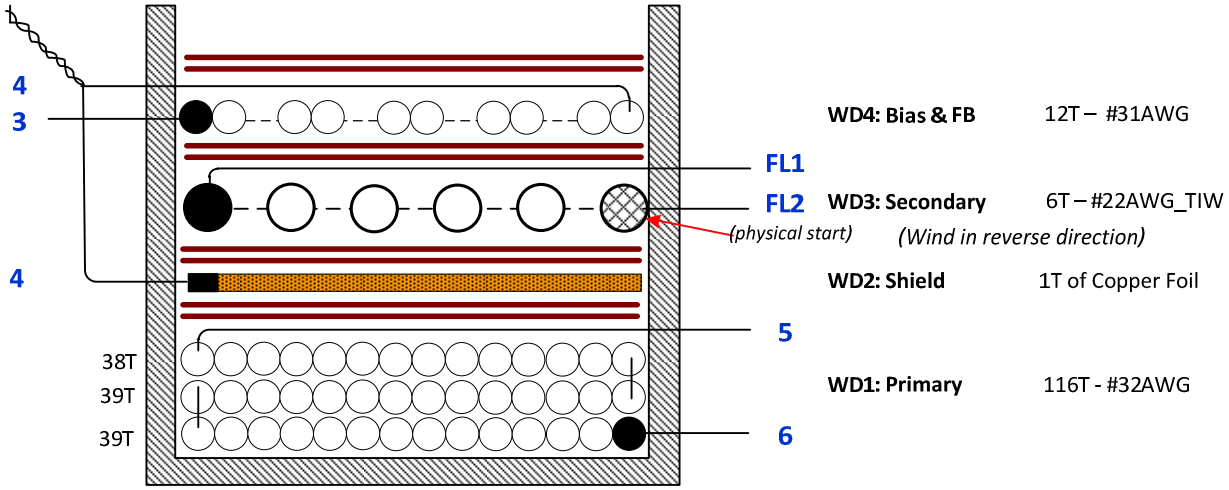

Figure 5 – Transformer Build Diagram.

7.5 Transformer Construction

Winding Preparation	Place the bobbin on the mandrel with the primary side (pins 1-4) is on the left side. Winding direction is clockwise direction.
WD1 Primary	Start pin 6, wind 116 turns of wire item [3] in 3 layers (39T+39T+38T), at the last turn bring the wire back to the right and finish at pin 5.
Insulation	Place 2 layers of tape item [6].
WD2 Shield	Use copper foil item [7] to make copper shield showed as in illustration below. Start pin 4, leave ~30 mm extra of wire, wind 1 full turn of Copper Foil (should be overlapped but no shortage) and leave no-connect at the end.
Insulation	Place 2 layers of tape item [6].
WD3 Secondary	This winding is reverse winding, so turn the bobbin with primary side (pins 1-4) now is on the right side. Start on the top of bobbin, leave ~30 mm floating with wire item [5] and designate as FL2, wind 6 turns from left to right, spread the wire evenly. At the last tum bring the wire back to the left, also leave ~30 mm floating and designate as FL1.
Insulation	Place 2 layers of tape item [6].
WD3 Bias & FB	Now turn the bobbin back to previous position. Start at pin 3, wind 12 turns of wire item [4] from left to right, spread wire evenly. At the last turn bring the wire back to the right to finish at pin 4, and leave ~30 mm floating.
Insulation	Place 2 layers of tape item [6] to secure windings.
Final Assembly	Twist 2 floating wires and tint to remove insulation of wires Gap core halves to get 1.16 mH. Place glue item [8] on both center legs of core halves. Wrap core halves and floating wires above with tape, see illustration below. Place epoxy item [9] at core gaps, to secure core halves with transformer body, sees illustration below. Remove non-using pins: 1, 2, 7, 8, 9, and 10. Vanish item [10].

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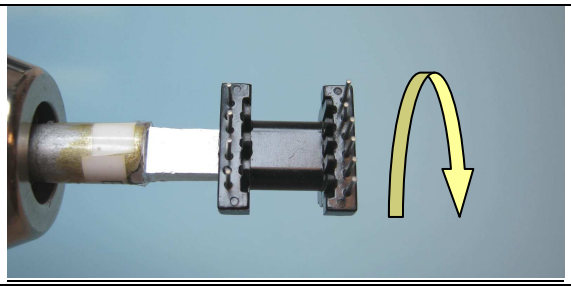
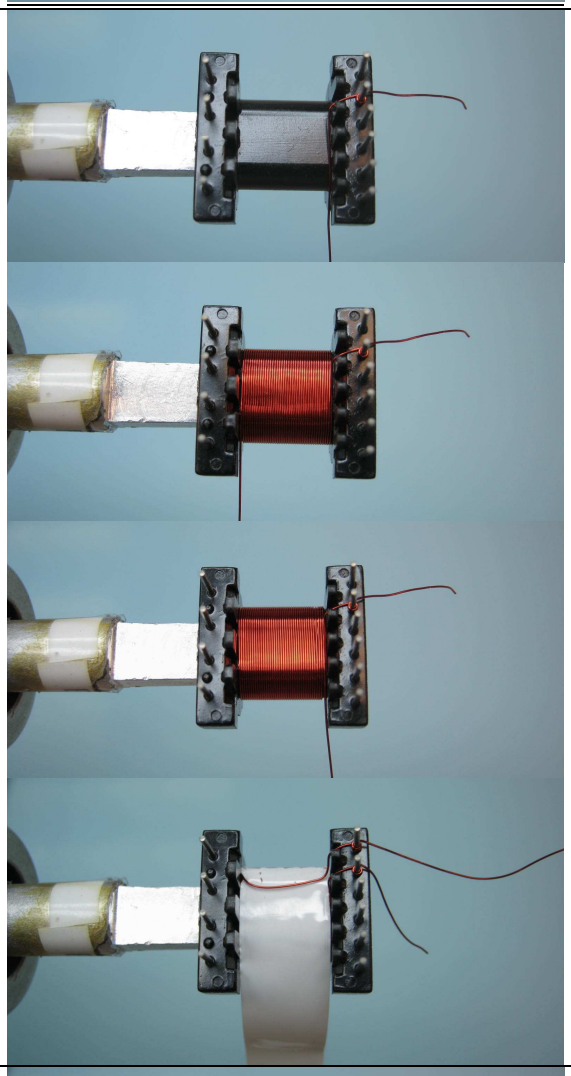
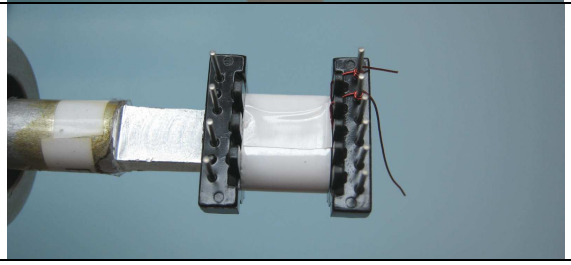
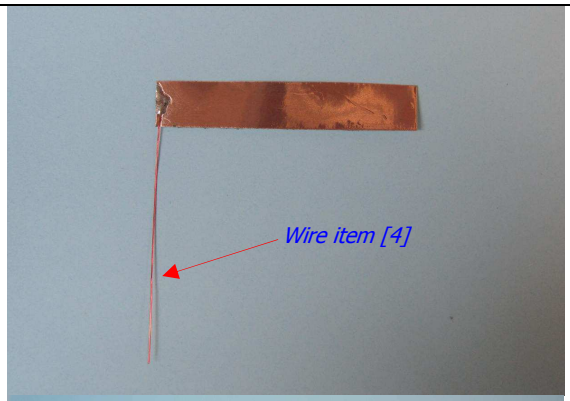
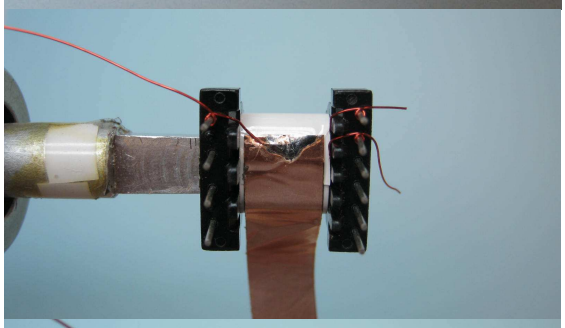
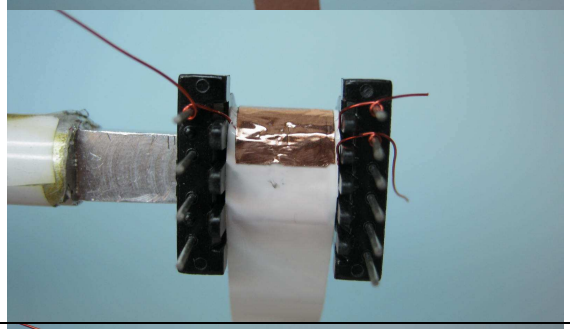
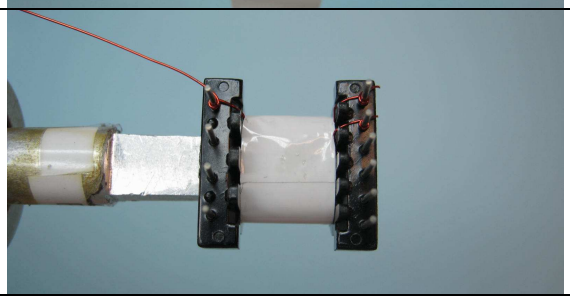
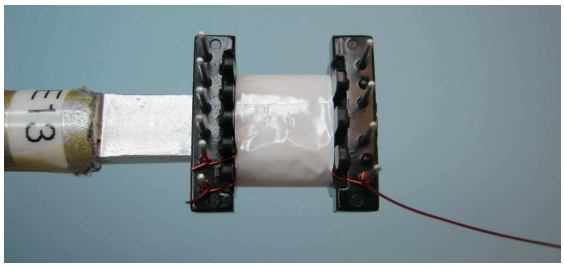
7.6 Transformer Illustrations

Winding Preparation		Place the bobbin on the mandrel with the primary side (pins 1-4) is on the left side. Winding direction is clockwise direction.
WD1 **Primary**		Start pin 6, wind 116 turns of wire item [3] in 3 layers (39T+39T+38T), at the last turn bring the wire back to the right and finish at pin 5.
Insulation		Place 2 layers of tape item [6].

WD2 **Shield**	  	Use copper foil item [7] to make copper shield showed as in illustration below. Start at pin 4, leave ~30 mm extra of wire, wind 1 full turn of copper foil (should be overlapped but no shortage) and leave no-connect at the end.
Insulation		Place 2 layers of tape item [6].
WD3 **Secondary**		This winding is reverse winding, so turn the bobbin with primary side (pins 1-4) now is on the right side. Start on the top of bobbin, leave ~30 mm floating with wire item [5] and designate as FL2, wind 6 turns from left to right, spread the wire evenly. At the last tum bring the wire

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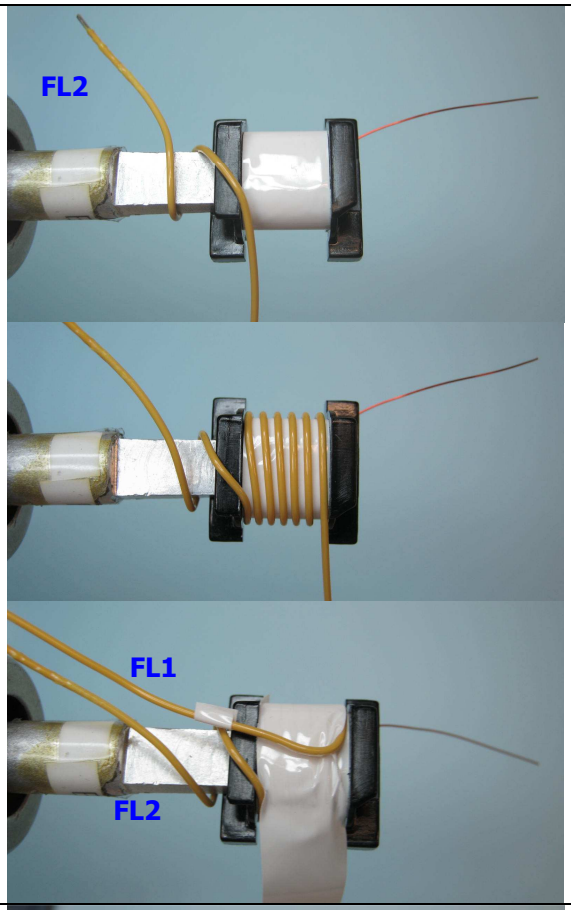
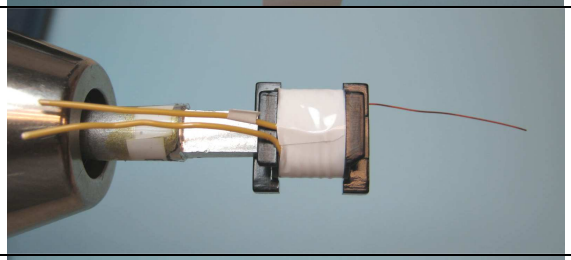
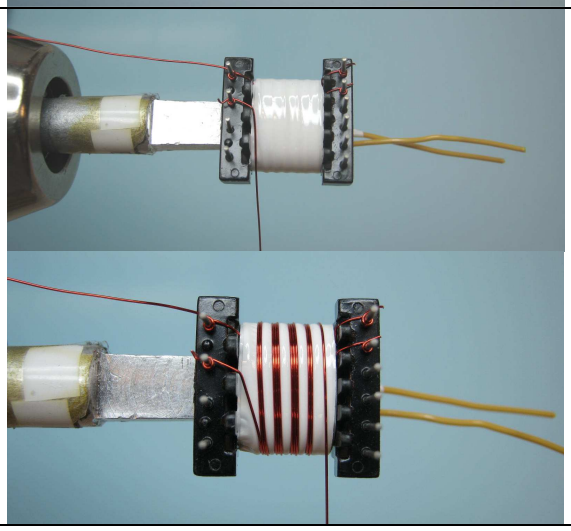
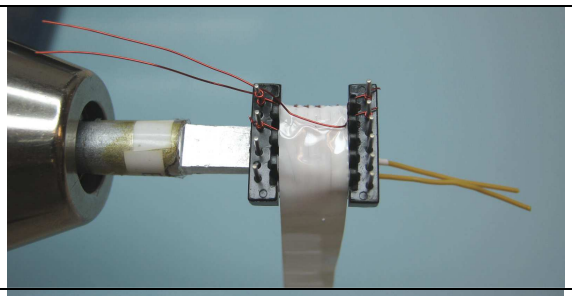
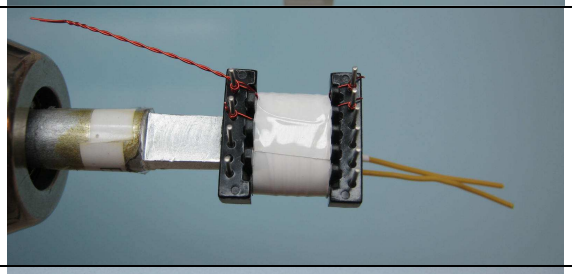
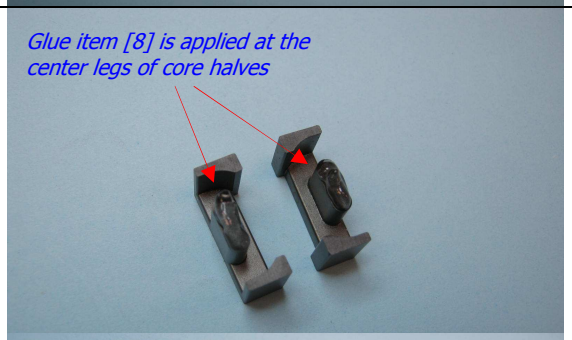
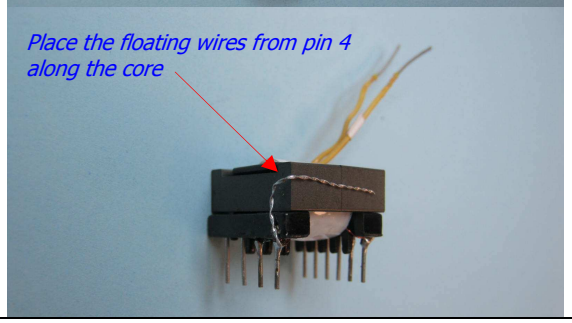
		back to the left, also leave ~30 mm floating and designate as FL1.
Insulation		Place 2 layers of tape item [6].
WD3 **Bias & FB**		Now turn the bobbin back to previous position. Start at pin 3, wind 12 turns of wire item [4] from left to right, spread wire evenly. At the last turn bring the wire back to the right to finish at pin 4, and leave ~30 mm floating.

		
Insulation		Place 2 layers of tape item [6] to secure windings.
Final Assembly	 	Twist 2 floating wires and tint to remove insulation of wires, Gap core halves to get 1.16 mH. Place glue item [8] on both center legs of core halves. Wrap core halves and floating wires above with tape, see illustration beside.

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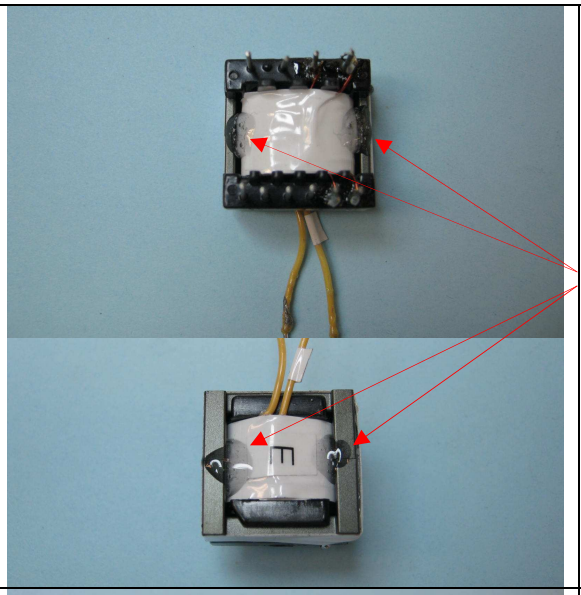
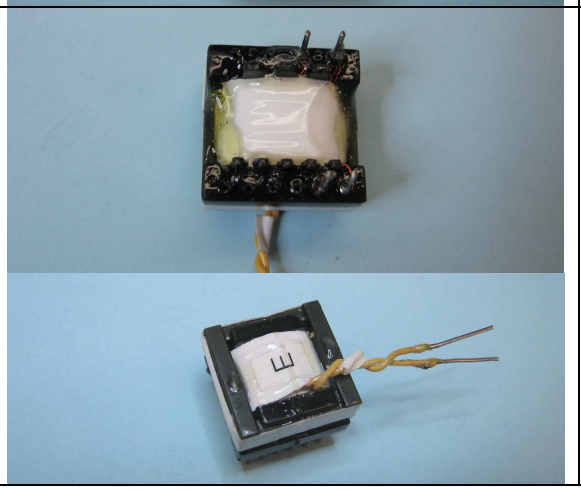
		Place epoxy item [9] at core gaps, to secure core halves with transformer body, see illustration beside.
		Remove non-using pins: 1, 2, 7, 8, 9, and 10. Vanish item [10].

8 Transformer Design Spreadsheet

ACDC_LinkSwitch-3_060914; Rev.2.1; Copyright Power Integrations 2014	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-3_060914_Rev2-1; LinkSwitch-3 Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN			90	V	Minimum AC Input Voltage
VACMAX			265	V	Maximum AC Input Voltage
fL			50	Hz	AC Mains Frequency
Application Type	**Adapter**				Choose application type
VO			5.00	V	Output Voltage (at continuous power)
IO	2.00		2.00	A	Minimum required output current
Power			10.00	W	Continuous Output Power
n			0.78		Efficiency Estimate at output terminals.
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
CIN	25.00		25.00	uF	Input Capacitance
ENTER LinkSwitch-3 VARIABLES					
Chosen Device	**LNK64x8K**		LNK64x8K		Chosen LinkSwitch-3 device and package. E.g. - LNK64x4D or LNK64x8K
Cable drop compensation option	**No comp**		No comp		Select level of cable drop compensation
Complete Part Number			LNK6448K		Full Part Number
ILIMITMIN			0.47	A	Minimum Current Limit
ILIMITTYP			0.51	A	Typical Current Limit
ILIMITMAX			0.55	A	Maximum Current Limit
FS	80.00		80.00	kHz	Typical Device Switching Frequency at maximum power
VOR			106.33	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10.00	V	LinkSwitch-3 on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP		*Info*	1.05		Power Supply may be operating in continuous conduction mode under certain conditions. Increase Cin, decrease DCON or use larger LYTSwitch-2 device
FEEDBACK WINDING PARAMETERS					
NFB	12.00		12.00		Feedback winding turns
VFLY			11.00	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
VFOR			9.83	V	Forward voltage - Voltage on Feedback Winding during switch on time
BIAS WINDING PARAMETERS					
BIAS	**Ext. Bias**		Ext. Bias		Select between self bias or external bias to supply the IC. Note that this will affect ILIMIT
VB			N/A	V	Feedback Winding Voltage (VFLY) is greater than 10 V. The feedback winding itself can be used to provide external bias to the LinkSwitch. Additional Bias winding is not required.
NB			N/A		Bias Winding number of turns
REXT			6.20	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
DESIGN PARAMETERS					
DCON	5.00		5.00	us	Desired output diode conduction time
DCON_FINAL			4.72	us	Final output conduction diode, assuming integer values for NP and NS, and VMIN
TON			5.29	us	LinkSwitch-3 On-time (calculated at LPMIN, VMIN and ILIMITMIN)

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RUPPER			44.69	k-ohm	Upper resistor in Feedback resistor divider
RLOWER			9.57	k-ohm	Lower resistor in resistor divider
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	**EPC17**		EPC17		Enter Transformer Core.
Custom_Core					Enter Core name if selection on drop down menu is "Custom"
Bobbin			EPC17_BOBBIN		Generic EPC17_BOBBIN
AE			22.80	mm^2	Core Effective Cross Sectional Area
LE			40.20	mm	Core Effective Path Length
AL			1150.00	nH/turn^2	Ungapped Core Effective Inductance
BW			9.55	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00		3.00		Number of Primary Layers
NS			6.00	turns	Number of Secondary Turns. To adjust Secondary number of turns change DCON
DC INPUT VOLTAGE PARAMETERS					
VMIN			94.98	V	Minimum DC bus voltage
VMAX			374.77	V	Maximum DC bus voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.52		Maximum duty cycle measured at VMIN
IAVG			0.15	A	Input Average current, at VMIN
IP			0.47	A	Peak primary current
IR			0.47	A	Primary ripple current
IRMS			0.23	A	Primary RMS current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			1077.58	uH	Minimum Primary Inductance
LPTYP			1158.69	uH	Typical Primary inductance
LP_TOLERANCE	7.00		7.00	%	Tolerance in primary inductance
NP			116.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG			86.11	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET	2220.00		2220.00	Gauss	Target Flux Density
BM			2216.79	Gauss	Maximum Operating Flux Density (calculated with LPTYP, ILIMITTYP), BM < 2600 is recommended
BP			2559.48	Gauss	Peak Operating Flux Density (calculated with LPMAX, ILIMITMAX), BP < 3100 is recommended
BAC			1108.40	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			161.35		Relative Permeability of Ungapped Core
LG			0.33	mm	Gap Length (LG > 0.1 mm)
BWE			28.65	mm	Effective Bobbin Width
OD			0.25	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.20	mm	Bare conductor diameter
AWG			33	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			50.80	Cmils	Bare conductor effective area in circular mils
CMA			224.41	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
ISP			9.01	A	Peak Secondary Current assuming Ilimitmin
ISRMS			4.14	A	Secondary RMS Current assuming Ilimitmax and Dmax
IRIPPLE			3.62	A	Output Capacitor RMS Ripple Current
CMS			827.19	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			20.00		Secondary Wire Gauge (Rounded up to next larger

					standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			618.07	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)
PIVS			24.38	V	Output Rectifier Maximum Peak Inverse Voltage
FINE TUNING					
RUPPER_ACTUAL			44.69	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL			9.57	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measued) Output Voltage (VDC)			5.00	V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)			2.00	Amps	Measured Output current from first prototype
RUPPER_FINE			44.69	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 44.2 k-ohms
RLOWER_FINE			9.57	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 9.53 k-ohms

Note: Different spreadsheet revisions may give slightly different spreadsheet values.

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9 Performance Data

All measurements were taken at room temperature unless otherwise specified, with 60 Hz input frequency. Measurements were taken on the PCB board.

9.1 Active Mode Efficiency

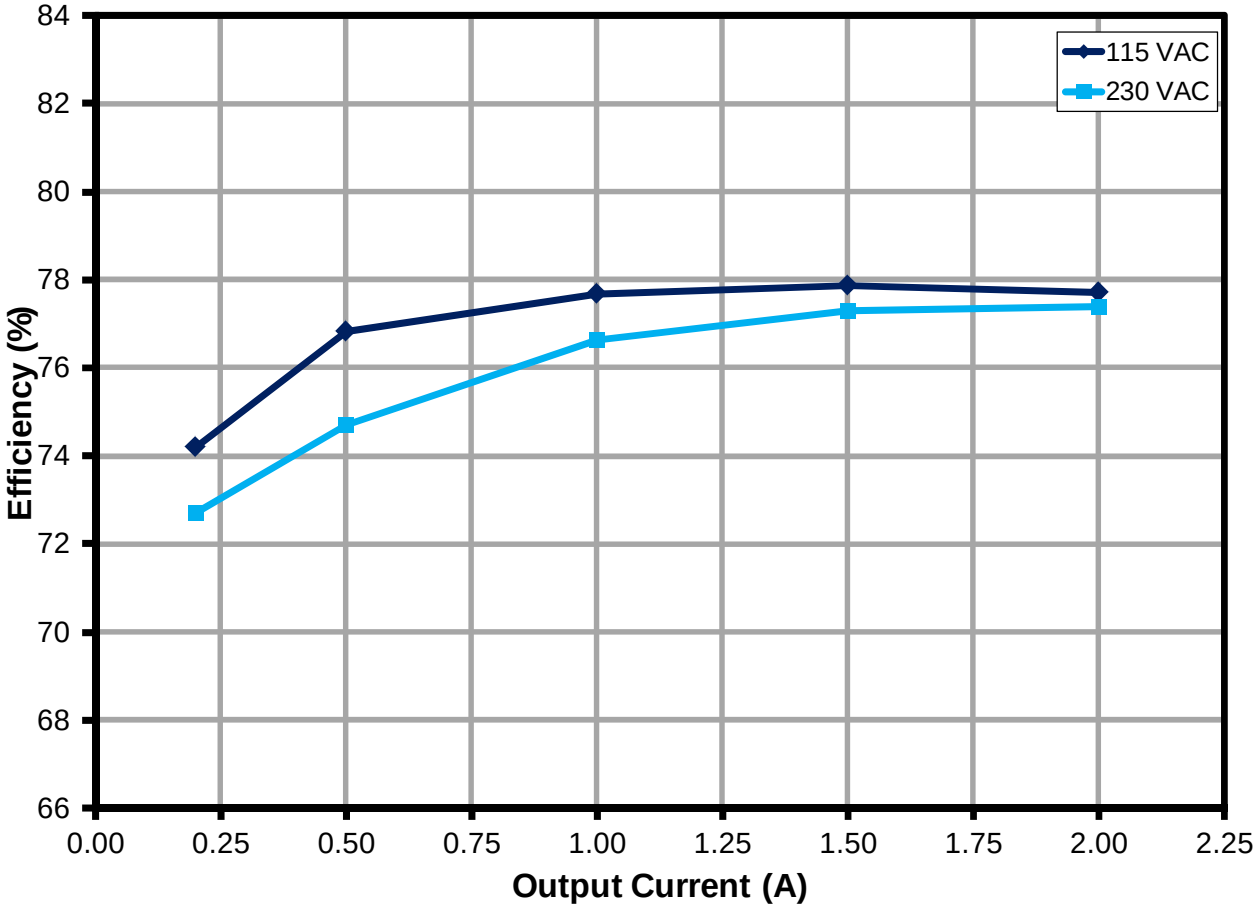

Figure 6 – Efficiency vs. Output Current.

9.2 Active Mode Measurement Data

For the latest, up-to-date information on energy efficiency regulations, please visit the PI Green Room, at:
http://www.powerint.com/greenroom/regulations.htm

Measured Performance			
		V_{IN} (VAC)	
		115	230
		Efficiency (%)	
Percent of Full Load	10	74.2	72.71
	25	76.82	74.71
	50	77.66	76.63
	75	77.86	77.28
	100	77.72	77.38
	Ave	**77.52**	**76.5**
No-Load Input Power† (mW)		26.09	26.65

Table 1 – Average Active Mode Efficiency.

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9.3 No-Load Input Power

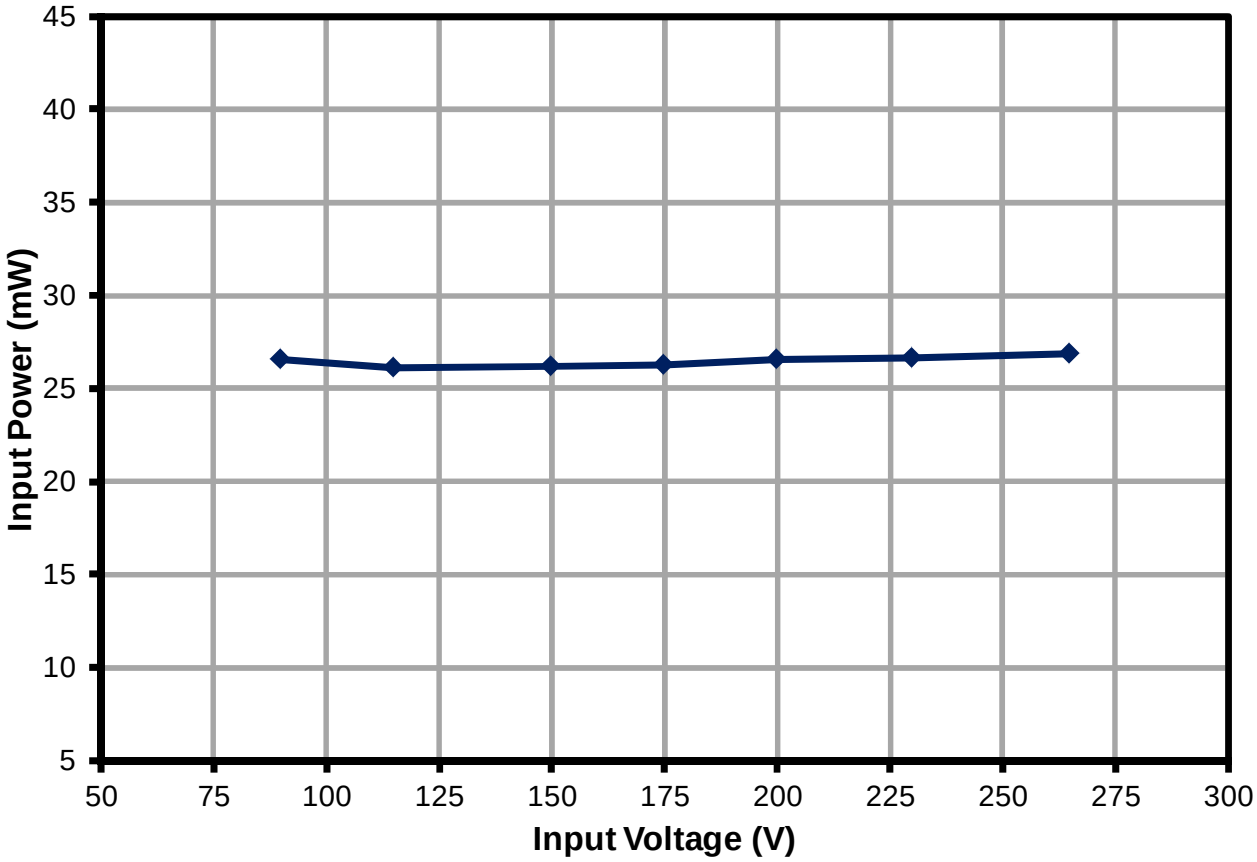

Figure 7 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 50 Hz.

9.4 Regulation

9.4.1 Load, Line and Temperature

The output characteristic was tested on the board. The measurements were made with the supply inside a sealed cardboard box. The cardboard box ensures air flow from the thermal chamber does not affect the test. The ambient temperature of the thermal chamber was monitored and adjusted to maintain the desired temperature. The unit was allowed to thermally stabilize for 30 minutes, unloaded, at each measurement temperature prior to data being recorded.

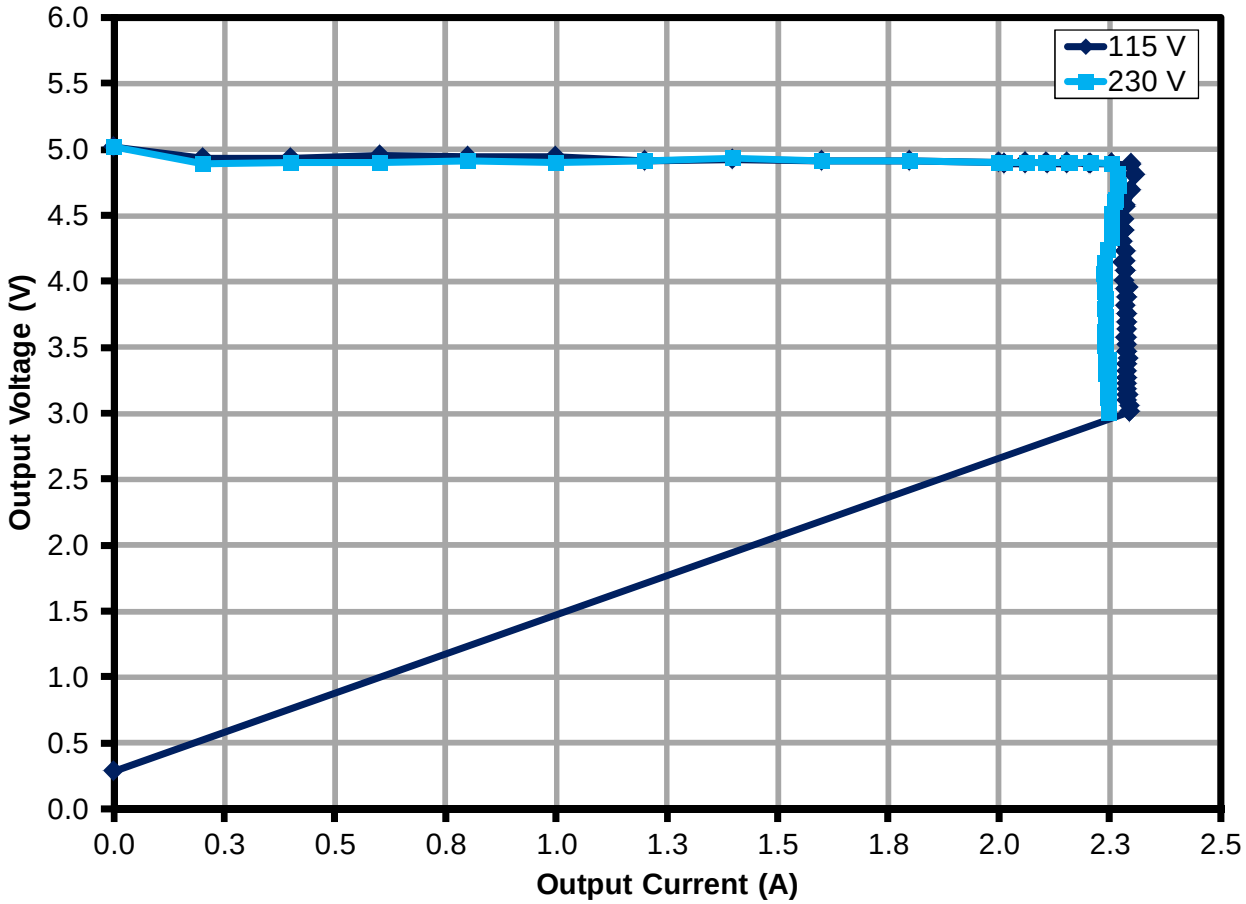

Figure 8 – CV/CC, 25 ºC.

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10 Thermal Performance

10.1 Operating Temperature Survey

Thermal performance was measured inside a sealed plastic enclosure at full load with no airflow; the sealed plastic enclosure was then put in a sealed cardboard box. The cardboard box ensures aif flow from the thermal chamber does not affect the test. The ambient temperature inside the cardboard box was monitored, and the temperature of the thermal chamber was adjusted to maintain the desired temperature. A thermocouple was attached to U1's source pin to measure the temperature of the device. The ambient temperature inside the sealed plastic enclosure also recorded.

Item	90 VAC	115 VAC	175 VAC	230 VAC	265 VAC
Ambient	40 ºC	40 ºC	40 ºC	40 ºC	40 ºC
Ambient in Enclosure	51.9 ºC	50.9 ºC	51.7 ºC	51.3 ºC	50.5 ºC
U1 SOURCE Pin	95.3 ºC	91.7 ºC	91.4 ºC	97.9 ºC	101.1 ºC

Table 2 – Temperature of the Device.

11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

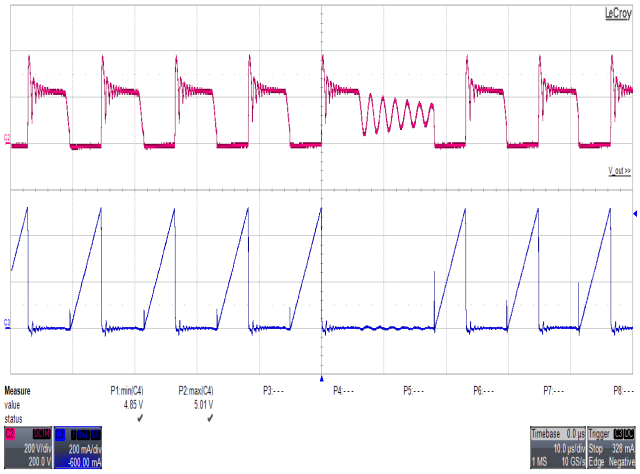

Figure 9 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 200 mA / div., 10 µs / div.

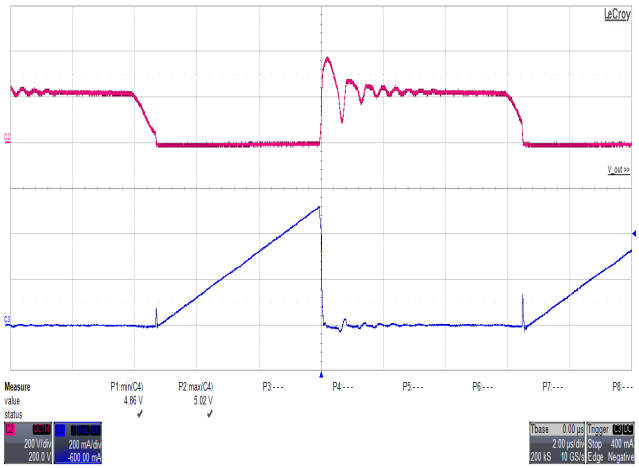

Figure 10 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 200 mA / div., 2 µs / div.

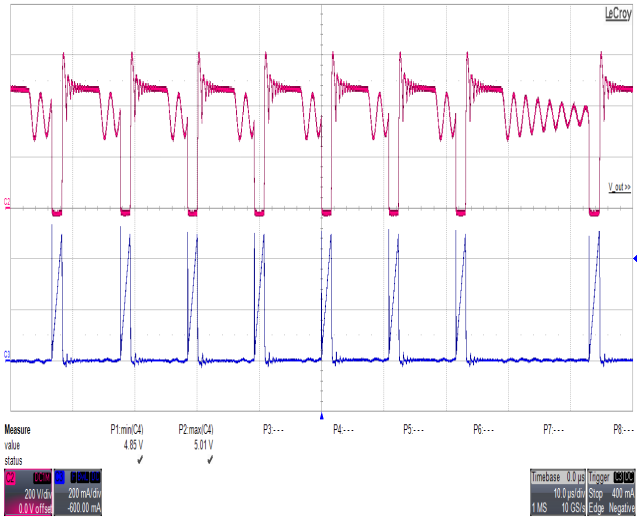

Figure 11 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 200 mA / div., 10 µs / div.

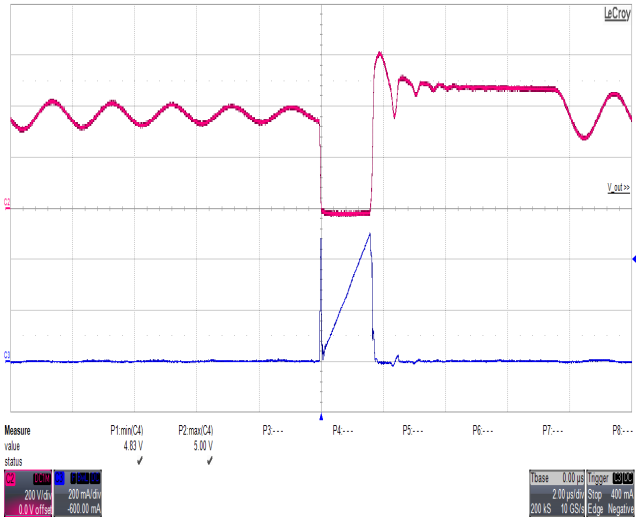

Figure 12 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 200 mA / div., 10 µs / div.

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11.2 Drain Voltage Current Start-up Profile

11.2.1 No-Load Output Voltage Start-up Characteristic

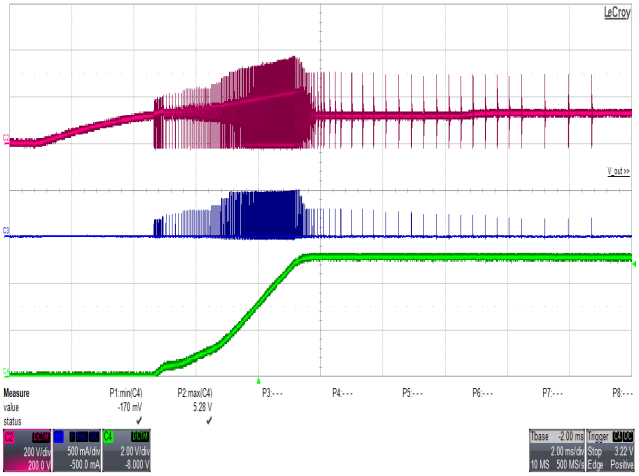

Figure 13 – 90 VAC Start-up Profile (No-Load).
Upper: V_{DRAIN}, 200 V / div.
Middle: I_{DRAIN}, 500 mA / div.
Lower: V_{OUT}, 2 V / div., 2 ms / div.

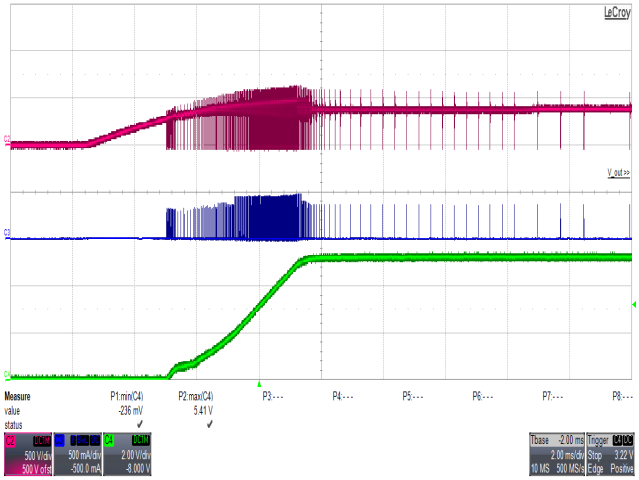

Figure 17 – 265 VAC Start-up Profile (No-Load).
Upper: V_{DRAIN}, 500 V / div.
Middle: I_{DRAIN}, 500 mA / div.
Lower: V_{OUT}, 2 V / div., 2 ms / div.

11.2.2 Full Load Start-up Characteristic

The output voltage was measured at the end of the USB cable.

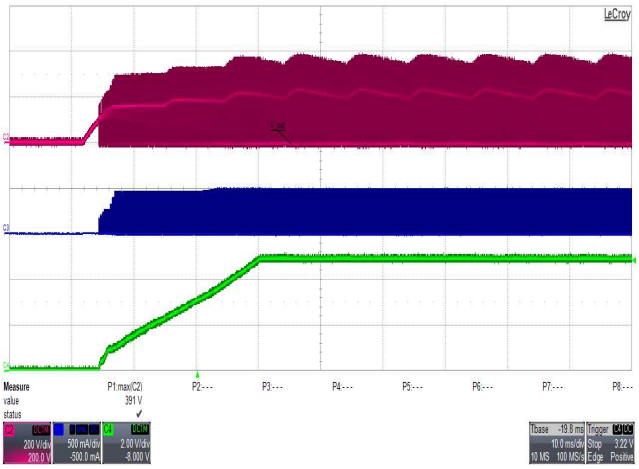

Figure 14 – 90 VAC Start-up Profile (Full Load).
Upper: V_{DRAIN}, 200 V / div.
Middle: I_{DRAIN}, 500 mA / div.
Lower: V_{OUT}, 2 V / div., 2 ms / div.

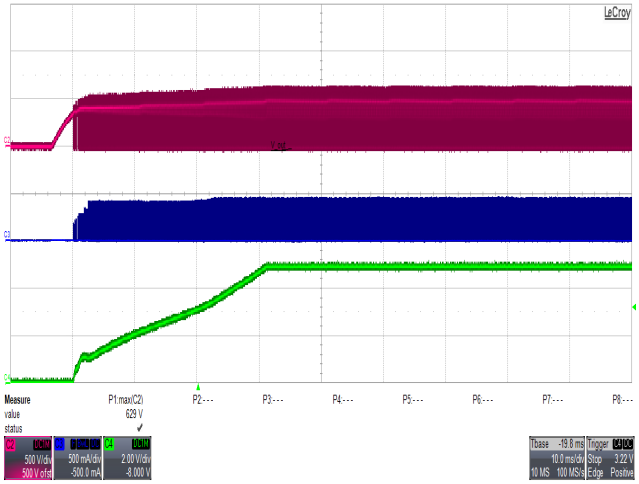

Figure 15 – 265 VAC Start-up Profile (Full Load), 629 V Maximum.
Upper: V_{DRAIN}, 500 V / div.
Middle: I_{DRAIN}, 500 mA / div.
Lower: V_{OUT}, 2 V / div., 2 ms / div.

11.3 Load Transient Response

11.3.1 (10% to 90% Load Step, 100 Hz)

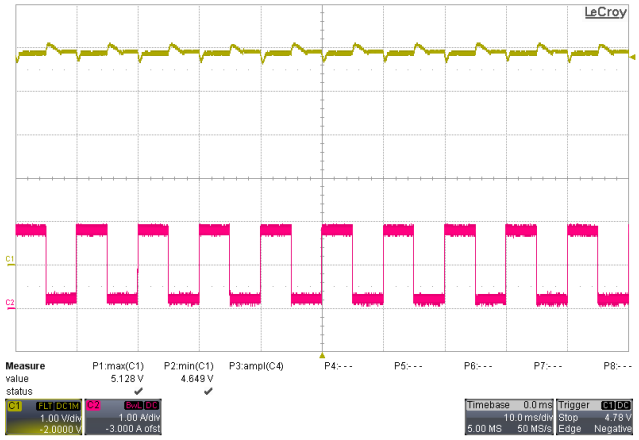

Figure 16 – Transient Response, 115 VAC, 90-10-90% Load Step.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 1 A / div., 250 mA / µs
5 ms / div.

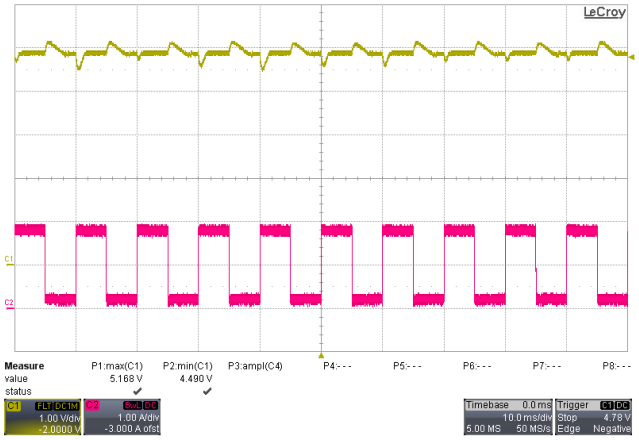

Figure 17 – Transient Response, 230 VAC, 90-10-90% Load Step.
Upper: V_{OUT} 1 V / div.
Lower: I_{OUT}, 1 A / div., 250 mA / µs
5 ms / div.

11.3.2 (0% to 500 mA Load Step, 100 Hz)

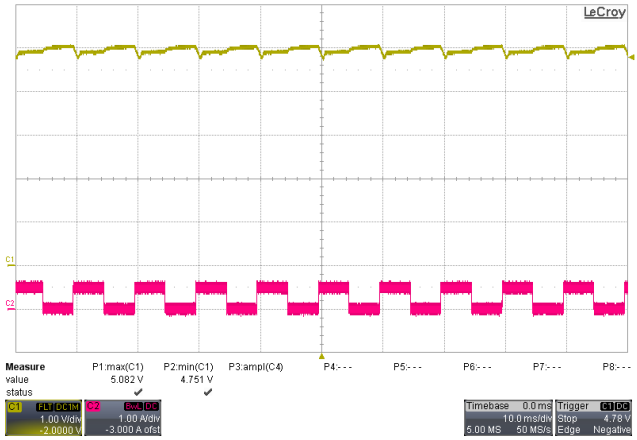

Figure 18 – Transient Response, 115 VAC, 25-0-25% Load Step.
Upper: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 1 A / div., 250 mA / µs,
5 ms / div.

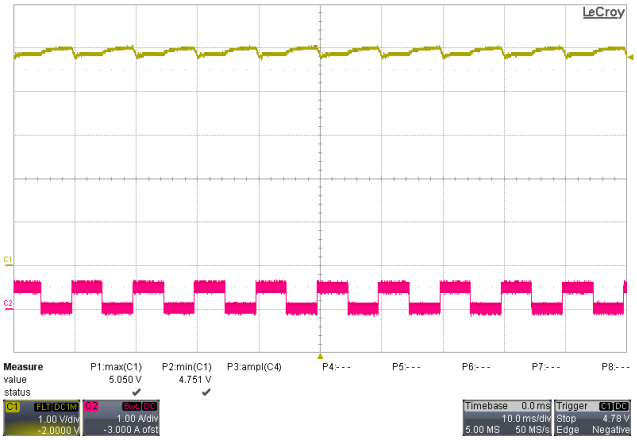

Figure 19 – Transient Response, 230 VAC, 25-0-25% Load Step.
Upper: V_{OUT} 1 V / div.
Lower: I_{OUT}, 1 A / div, 250 mA / µs,
5 ms / div.

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11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 μF / 50 V ceramic capacitor and 1 μF / 50 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

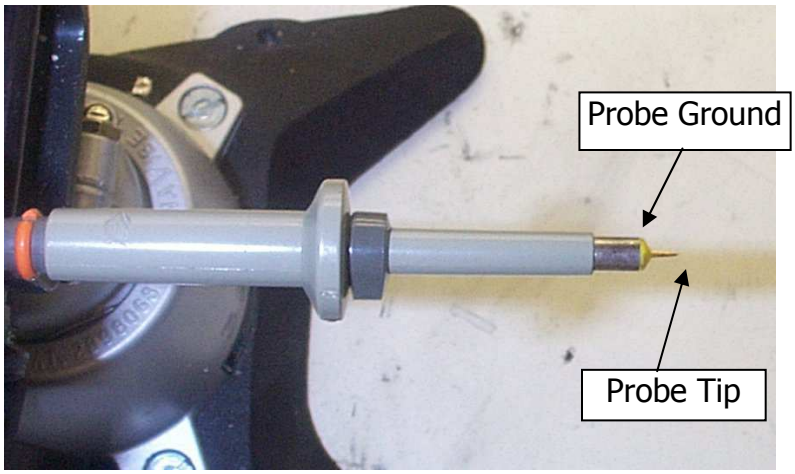

Figure 20 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

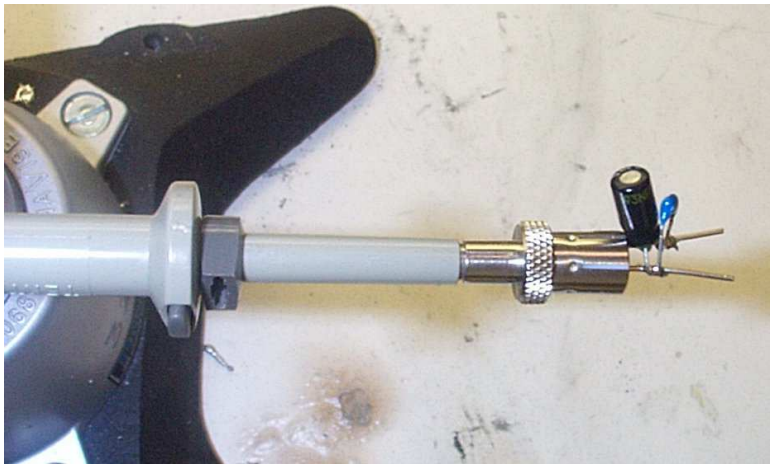

Figure 21 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

11.4.2 Ripple Measurement Results

The output ripple voltage is measured at the end of the USB cable.

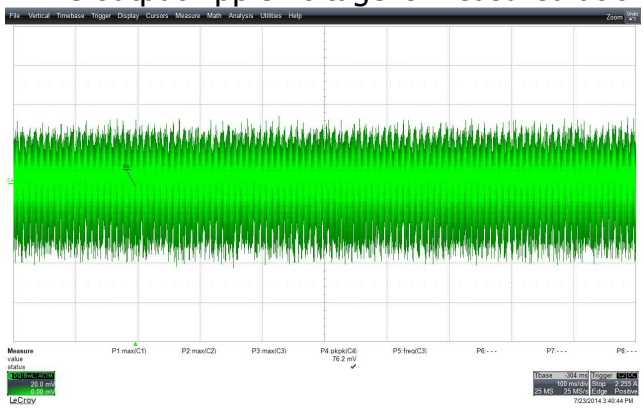

Figure 22 – V_{OUT} Ripple (76.2 mV), 90 VAC, 2 A
20 mV / div., 100 ms / div.

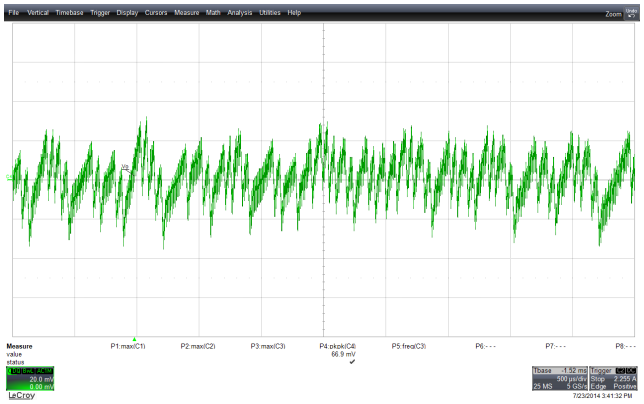

Figure 23 – V_{OUT} Ripple (66.9 mV), 90 VAC, 2 A
20 mV / div., 500 µs / div.

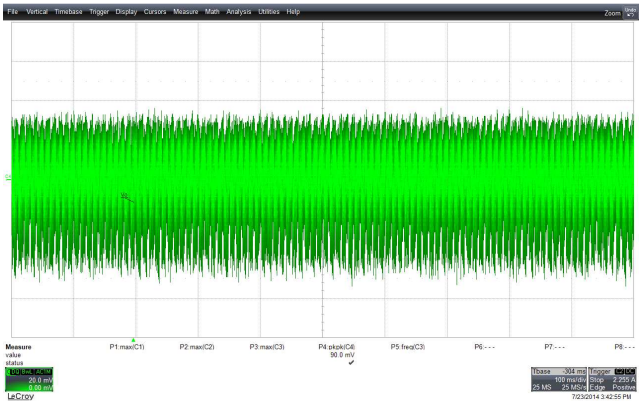

Figure 24 – V_{OUT} Ripple (90.0 mV), 115 VAC, 2 A
20 mV / div., 100 ms / div.

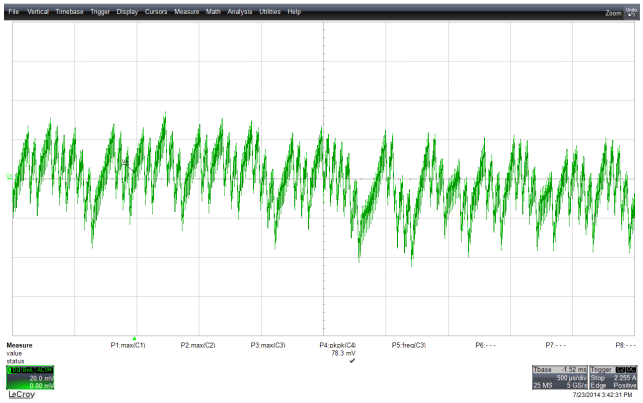

Figure 25 – V_{OUT} Ripple (78.3 mV), 115 VAC, 2 A
20 mV / div., 500 µs / div.

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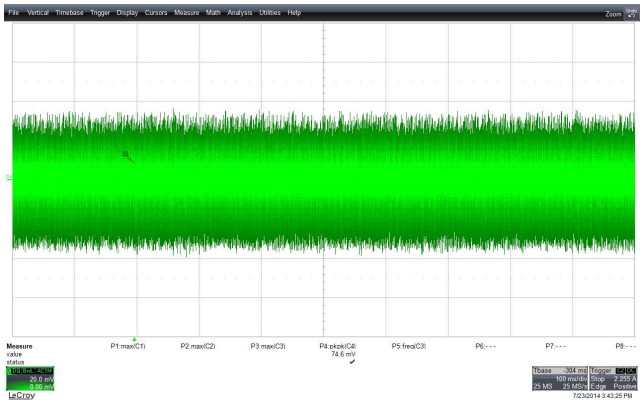

Figure 26 – V_{OUT} Ripple (74.6 mV), 230 VAC, 2 A
20 mV / div., 100 ms / div.

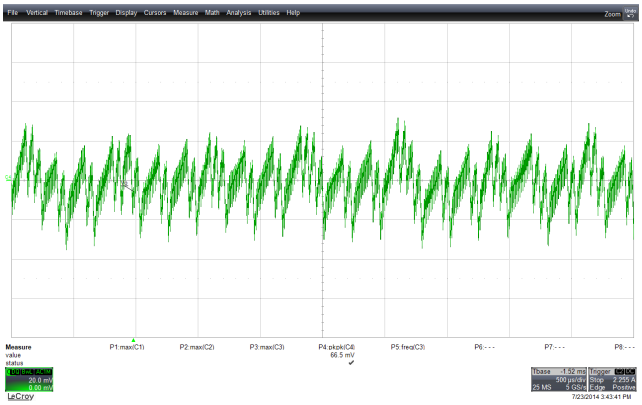

Figure 27 – V_{OUT} Ripple (66.5 mV), 230 VAC, 2 A
20 mV / div, 500 µs / div.

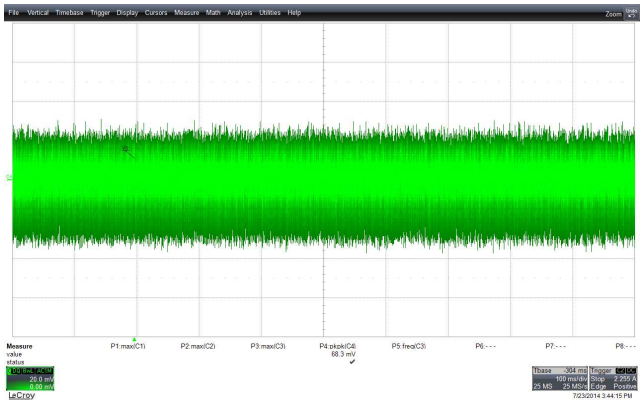

Figure 28 – V_{OUT} Ripple (68.3 mV), 265 VAC, 2 A
20 mV / div., 100 ms / div.

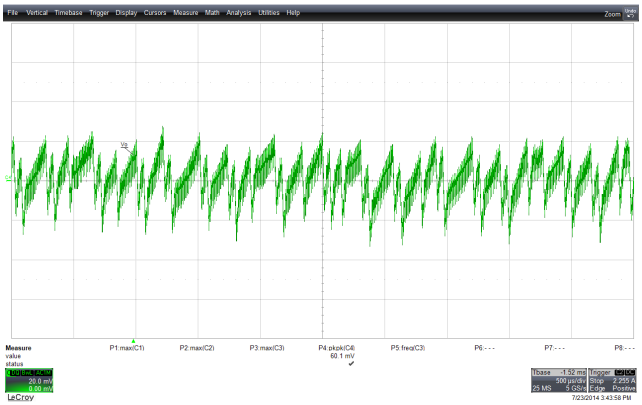

Figure 29 – V_{OUT} Ripple (60.1 mV), 265 VAC, 2 A
20 mV / div., 500 µs / div.

12 Line Surge

Differential input line 1.2 µs / 50 µs surge testing to IEC61000-4-5 standards was completed on a single test unit. The input voltage was set at 230 VAC / 60 Hz.

	Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)	Inject strike
DM (2 Ω)	+1 kV	230	L to N	0	Pass	10 Times
DM (2 Ω)	-1 kV	230	L to N	0	Pass	10 Times
DM (2 Ω)	+1 kV	230	L to N	90	Pass	10 Times
DM (2 Ω)	-1 kV	230	L to N	90	Pass	10 Times
DM (2 Ω)	+1 kV	230	L to N	270	Pass	10 Times
DM (2 Ω)	-1 kV	230	L to N	270	Pass	10 Times
CM (12 Ω)	+2 kV	230	L, N to PE	0	Pass	10 Times
CM (12 Ω)	-2 kV	230	L, N to PE	0	Pass	10 Times
CM (12 Ω)	+2 kV	230	L, N to PE	90	Pass	10 Times
CM (12 Ω)	-2 kV	230	L, N to PE	90	Pass	10 Times
CM (12 Ω)	+2 kV	230	L, N to PE	270	Pass	10 Times
CM (12 Ω)	-2 kV	230	L, N to PE	270	Pass	10 Times

13 ESD (Resistive Full Load at the Output)

Device	Discharge Type	Discharge Location	Voltage	# of Events (1/sec)	Remarks
LNK6448K	Contact	+ Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
		- Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
	Air	+ Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS
		- Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS

PASS = No output glitch or latch-off.

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14 Conducted EMI

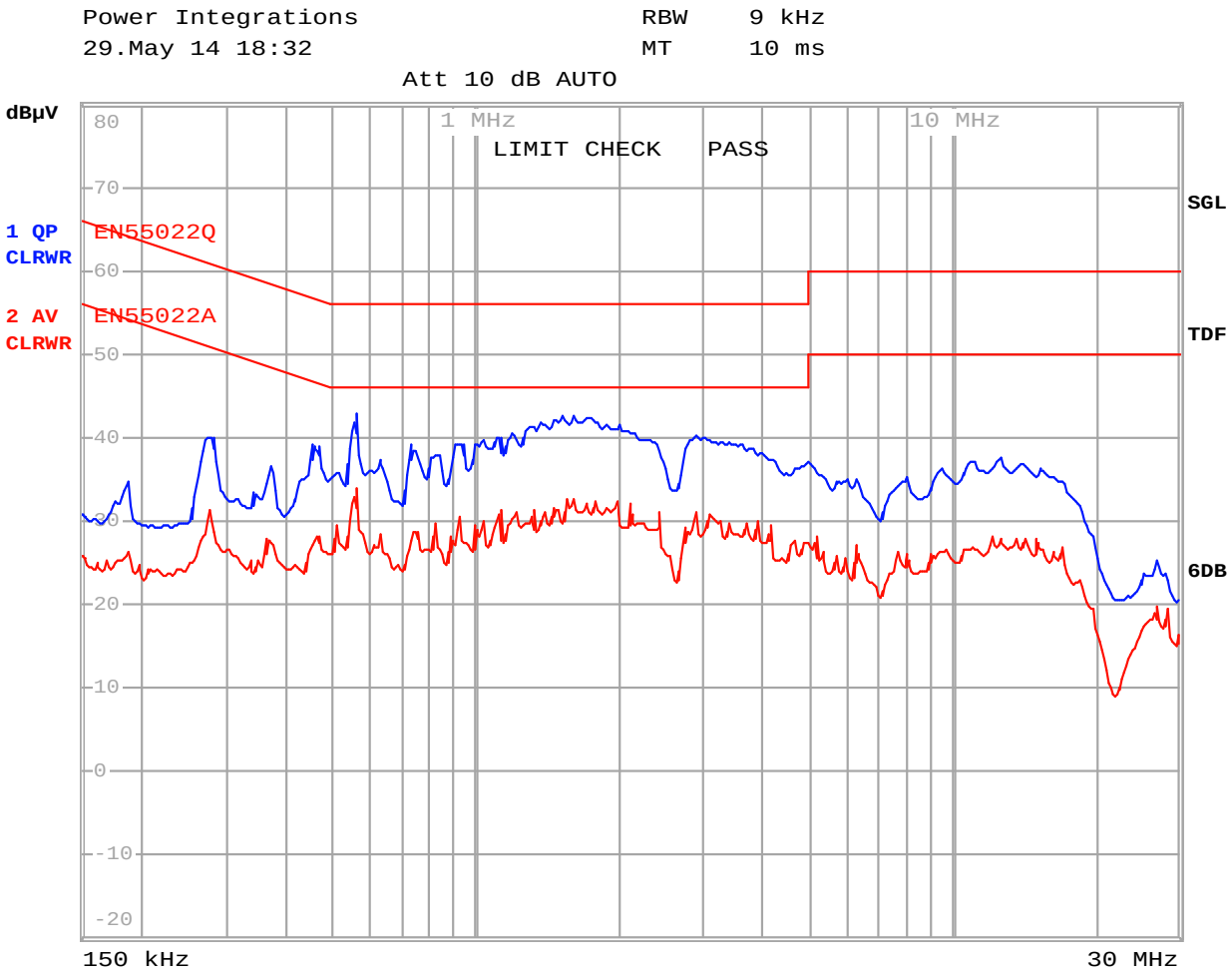

Figure 30 – 115 VAC Line, 2.5 Ω Resistor Load, Artificial Ground**.**

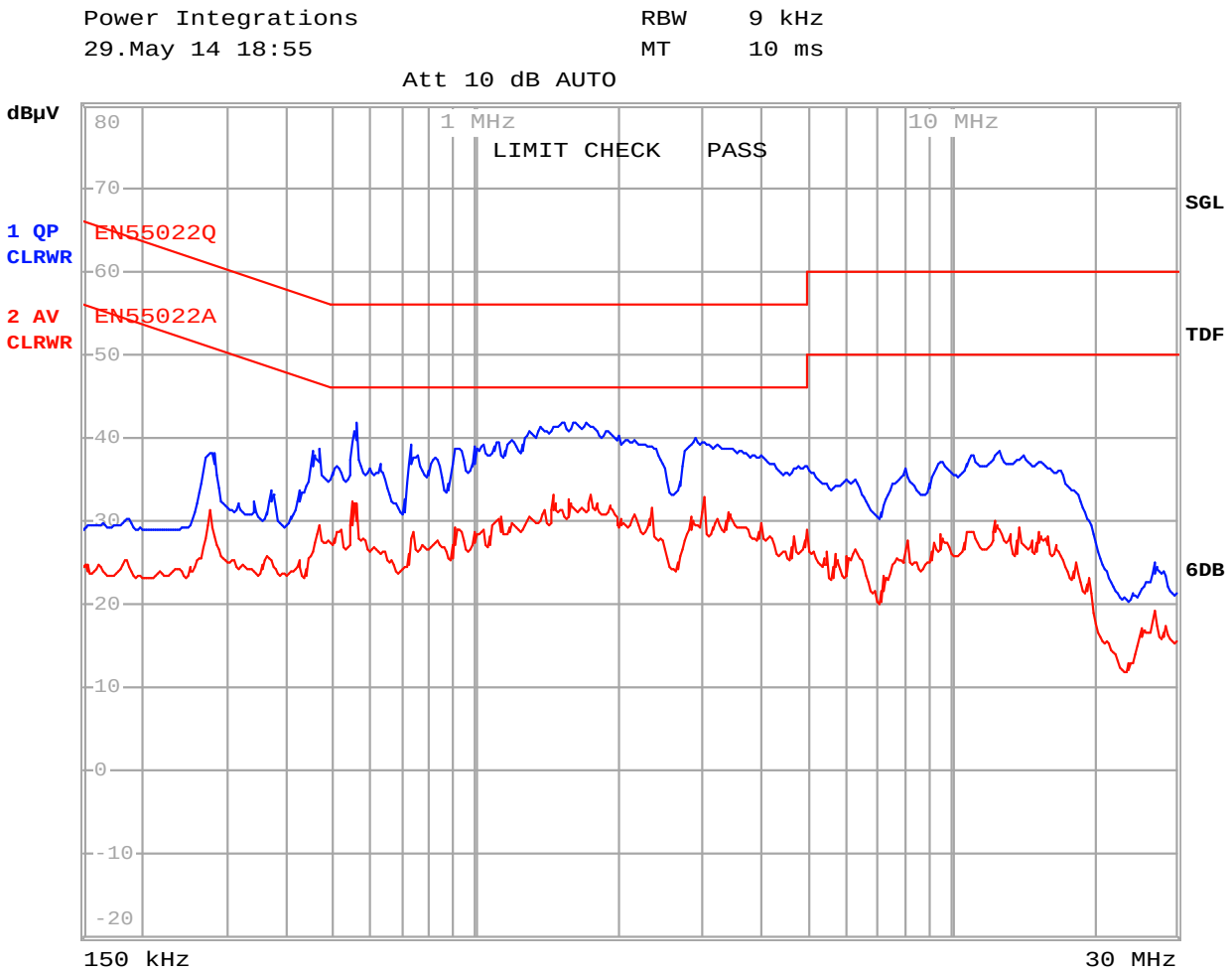

Figure 31 – 115 VAC Neutral, 2.5 Ω Resistor Load, Artificial Ground.

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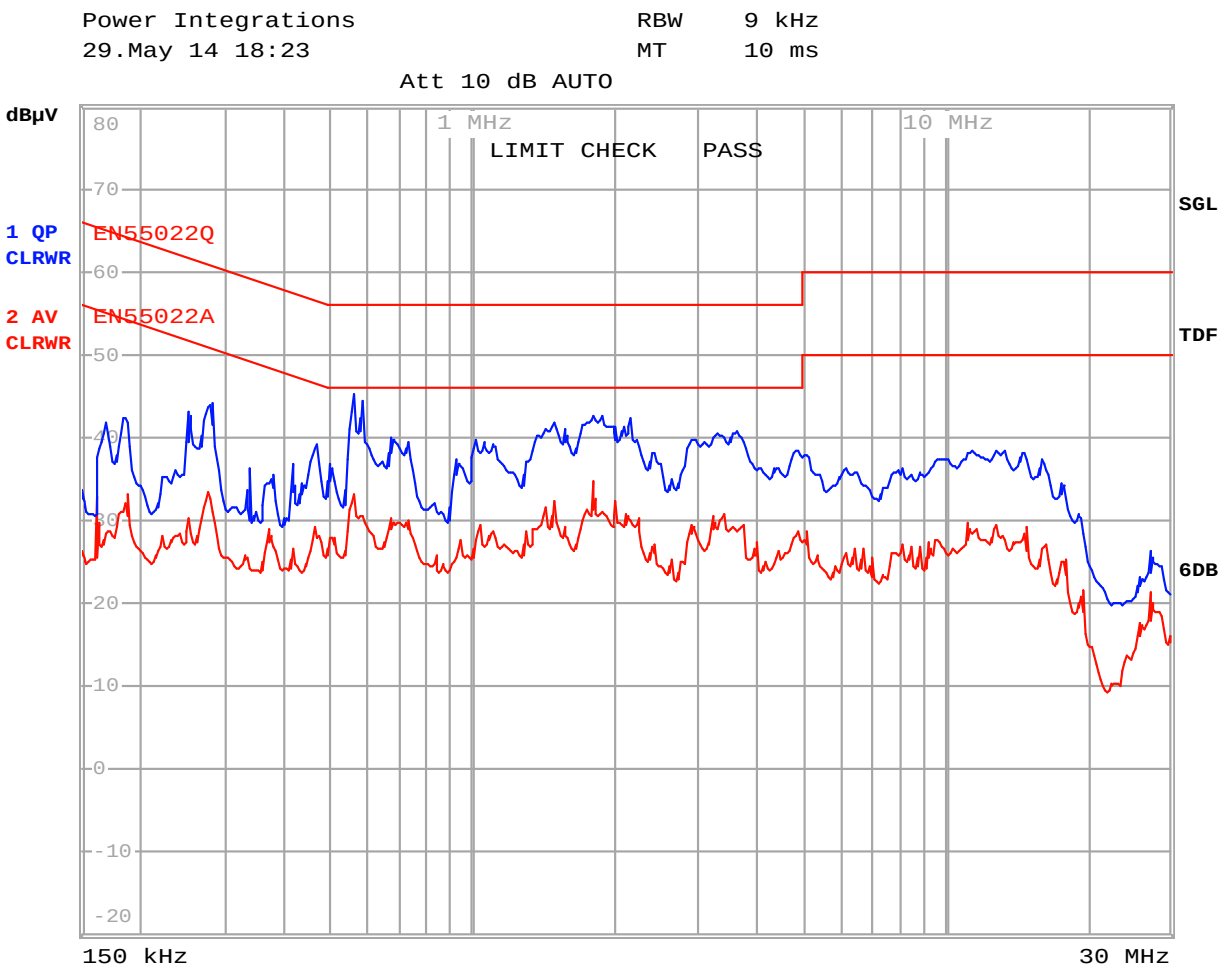

Figure 32 – 230 VAC Line, 2.5 Ω Resistor Load, Artificial Ground.

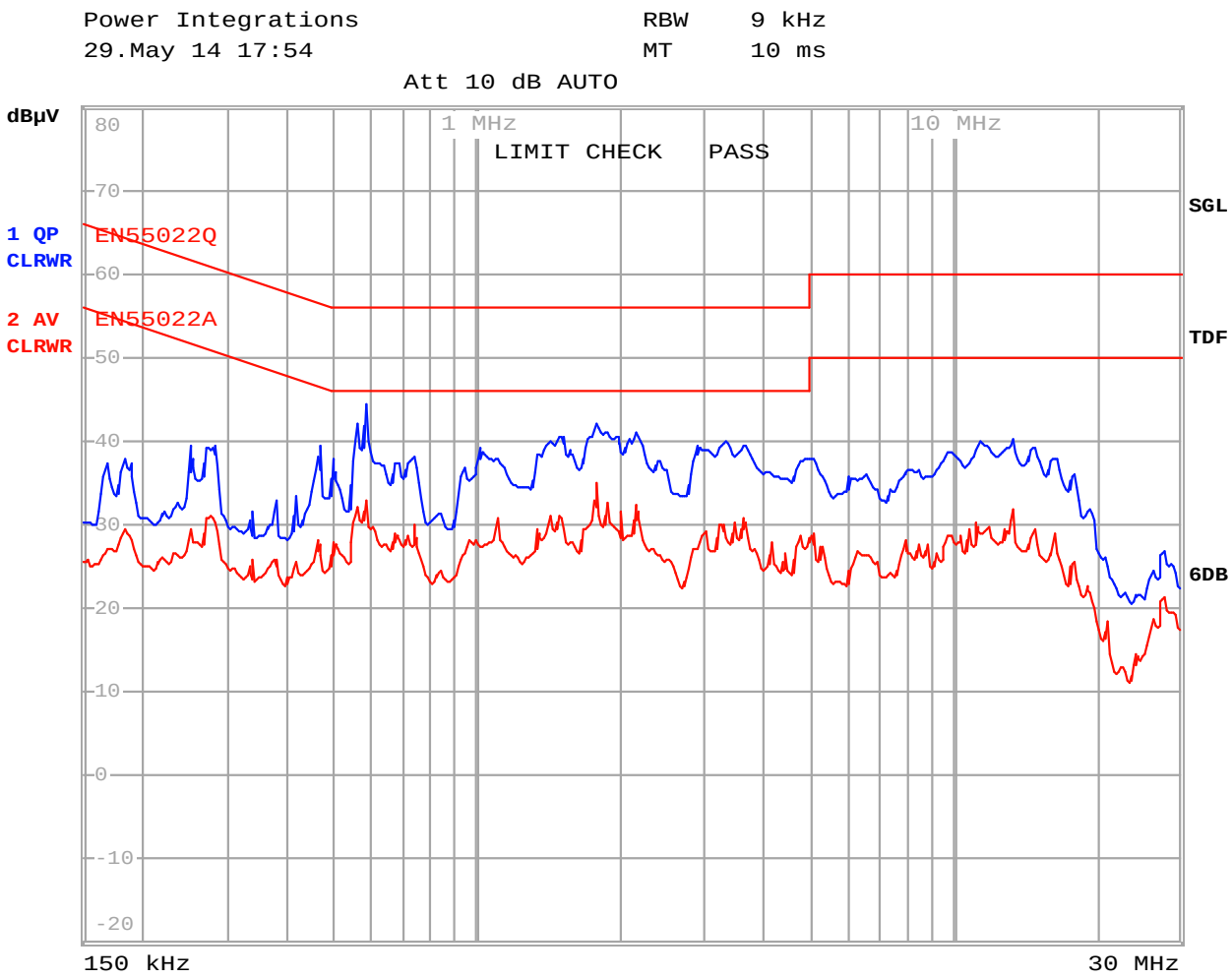

Figure 33 – 230 VAC Neutral, 2.5 Ω Resistor Load, Artificial Ground.

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15 Revision History

Date	Author	Revision	Description and changes	Reviewed
21-Apr-15	XL	1.2	Initial Release	Apps & Mktg

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