### Design Example Report

<table>
<thead>
<tr>
<th><strong>Title</strong></th>
<th>4 W Power Factor Corrected (Valley Fill) Non-Dimmable Isolated Flyback, Constant Voltage LED Driver Using LYTSwitch™-2 LYT2003D</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Specification</strong></td>
<td>Input: 190 VAC – 265 VAC (47 – 63 Hz); Output: 24 V, 167 mA</td>
</tr>
<tr>
<td><strong>Application</strong></td>
<td>Ballast LED Driver</td>
</tr>
<tr>
<td><strong>Author</strong></td>
<td>Applications Engineering Department</td>
</tr>
<tr>
<td><strong>Document Number</strong></td>
<td>DER-421</td>
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<tr>
<td><strong>Date</strong></td>
<td>August 20, 2014</td>
</tr>
<tr>
<td><strong>Revision</strong></td>
<td>1.2</td>
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</table>

#### Summary and Features
- Accurate primary side control constant voltage eliminates optocoupler and secondary control circuit.
- Combined CV/CC output characteristic
- Eliminates current sense resistors for better efficiency.
  - >80% active-mode efficiency.
- Easily meets CEC and ENERGY STAR 2.0 regulations
- No-load consumption <100 mW at 265 VAC
- Ultra-low leakage current: <5 μA at 265 VAC input.
- Easily meets EN550022, EN55015 and CISPR-22 Class B conducted EMI
- Auto-restart protection feature reduces power delivered to output by 95% during output short-circuit or open-loop fault conditions.

#### PATENT INFORMATION
The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations’ patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

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**Power Integrations**
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200  Fax: +1 408 414 9201
www.powerint.com
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.


1 Introduction

This engineering report describes a 4 W power supply that uses a LYTSwitch-2 IC, LYT2003D from the LYTSwitch-2 family, configured as a flyback. The power supply is specifically designed as an LED driver; however, it may also be used as a general evaluation platform for other applications that require constant voltage and constant current output.

This document contains the power supply specification, schematics, bill of materials, transformer documentation, printed circuit layout, and performance data.
## 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Comment</th>
</tr>
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<tr>
<td>Input</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>( V_{\text{IN}} )</td>
<td>190</td>
<td>265</td>
<td>2 Wire – no P.E.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>( f_{\text{LINE}} )</td>
<td>47</td>
<td>63</td>
<td>0.05</td>
<td>Hz</td>
<td>269 V; 50 Hz – No damage will occur to the PSU nor should the fuse open</td>
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<tr>
<td>No-load Input Power (230 VAC)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>In-rush Current (Cold start)</td>
<td>( I_{\text{RUSH}} )</td>
<td></td>
<td></td>
<td>0.67</td>
<td></td>
<td></td>
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<tr>
<td>Power Factor</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CV Output Voltage</td>
<td>( V_{\text{OUT}} )</td>
<td>23</td>
<td>24</td>
<td>25</td>
<td>V ± 5%</td>
<td></td>
</tr>
<tr>
<td>CC Output Voltage Range</td>
<td></td>
<td>10</td>
<td>23</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Ripple Voltage</td>
<td>( V_{\text{RIPPLE}} )</td>
<td>1</td>
<td></td>
<td>V</td>
<td>Peak to peak, 20 MHz bandwidth-measured with 1 ( \mu )F and 0.1 ( \mu )F ceramic capacitor</td>
<td></td>
</tr>
<tr>
<td>Total Output Power</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous Output Power</td>
<td>( P_{\text{OUT}} )</td>
<td>4</td>
<td></td>
<td>W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Required Average Efficiency at 25, 50, 75 and 100 % of ( P_{\text{OUT}} )</td>
<td>( \eta_{\text{AVE}} )</td>
<td>75</td>
<td></td>
<td>%</td>
<td>Per Energy Star test method</td>
<td></td>
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<td>Environmental</td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>Conducted EMI</td>
<td></td>
<td></td>
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<tr>
<td>Safety</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Meets CISPR22B / EN55022B/FCC Part 15</td>
</tr>
<tr>
<td>Leaked Current</td>
<td>( I_{\text{LEAK}} )</td>
<td>0.25 mA</td>
<td></td>
<td></td>
<td>Measured at 265 V(_{\text{AB}}), 50/60 Hz</td>
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<tr>
<td>Line Surge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Mode (L1-L2)</td>
<td></td>
<td>1</td>
<td></td>
<td>kV</td>
<td>IEC 61000-4-5/EN5504,</td>
<td></td>
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<tr>
<td>Common mode (L1/L2-PE)</td>
<td></td>
<td>2.5</td>
<td></td>
<td>kV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ring Wave (100 kHz)</td>
<td></td>
<td>2.5</td>
<td></td>
<td>kV</td>
<td>500 A short-circuit</td>
<td></td>
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<tr>
<td>Differential Mode (L1-L2)</td>
<td></td>
<td>2.5</td>
<td></td>
<td>kV</td>
<td>Series Impedance:</td>
<td></td>
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<tr>
<td>Common Mode (L1/L2-PE)</td>
<td></td>
<td></td>
<td></td>
<td>kV</td>
<td>Differential Mode: 2 ( \Omega )</td>
<td></td>
</tr>
<tr>
<td>Ambient Temperature</td>
<td>( T_{\text{AMB}} )</td>
<td>0</td>
<td>45</td>
<td>°C</td>
<td>Free convection, sea level</td>
<td></td>
</tr>
</tbody>
</table>
3 Schematic

![Schematic Diagram]

Figure 2 – Schematic.
4 Circuit Description
This LYTSwitch-2 based driver uses a flyback configuration to provide isolation between the primary and secondary. This converter provides 167 mA at 24 V over an input voltage range of 190 VAC to 265 VAC and is designed to drive LEDs in constant voltage or constant current operation. The LYTSwitch-2 IC controls the output using primary side regulation (PSR), reducing component count.

Being isolated, the user can dim by connecting a PWM converter, linear regulator or a DC-DC converter to the output.

This converter can also be used as an auxiliary supply for other types of lighting application.

4.1 Input Stage
Fusible resistor RF1 protects the power supply in the event that excessive input current is drawn. This fusible resistor aids in limiting the stress voltage during line transient and line surge as well as limiting the inrush current during a hot-plug.

The AC input is full wave rectified by diodes D1- D4 in full bridge configuration. The rectified DC is filtered by the bulk storage capacitors C8 and C10. Differential choke L1, C8 and C10 form the EMI filter which ensures compliance with Class B emission limits for conducted EMI. Resistor R1 damps the Q of L1, attenuating high frequency noise.

A passive (valley-fill) power factor correction circuit is employed to increase power factor to 0.74 at 230 VAC. This is composed of capacitors C1 and C2 and diodes D5, D6, D7 plus resistor R2. The valley-fill circuit also absorbs energy during differential line surges (IEC 61000-4-5/EN5504). At the point that the DC rectified voltage $V_{IN}$ falls lower than the voltage across C1 and C2, they are effectively connected in parallel and supply power to the bulk capacitor (C10). Capacitors C1 and C2, which appear in series, are charged through D6 and R2 when $V_{IN}$ DC is higher than the voltage across these capacitors. This forces input current to follow the input voltage, as shown in Figures 22 to 25, thus increasing PF.

4.2 LYTSwitch-2 - LYT2003D
The LYT2003D IC (U1) combines a power switching MOSFET, an oscillator, CV/CC control engine, as wells as start-up and protection circuits into one IC.

The control input regulates both the output voltage in CV mode and the output current in CC mode. Control is achieved by measuring forward and flyback voltages developed across the bias winding which is fed to the FB pin. Resistors R5 and R6 are 1% resistors to center the nominal (CV) $V_{OUT}$ and to ensure accurate constant current regulation. The device uses an ON/OFF control technique with multiple states to minimize audible noise and to optimize efficiency in CV mode operation. Variable frequency control is used in CC mode.
IC U1 is supplied from the BP (BYPASS) pin and the decoupling capacitor C4. IC U1 uses the energy stored in C4 when the MOSFET is on, and an internal 6 V regulator draws current from the MOSFET DRAIN pin when the MOSFET is off.

To minimize power consumption during no-load, especially at highest input voltage, the design employs the external supply voltage from the feedback/bias winding, through diode D10 and resistor R7 plus capacitor C5. Note that the bias winding return is directly connected to the bulk capacitor C10 ground point in the layout, which helps increase surge immunity.

This design used of a RCD-R clamp comprising of diode D9, capacitor C3 and resistors R3 and R4 to limit the MOSFET’s drain voltage due to the leakage inductance of the transformer. The loop formed by this clamp and the primary winding of the transformer T1 is made small to reduce radiation EMI.

4.3 Output Rectification

Schottky diode D11 rectifies the transformer secondary output and the rectified voltage is filtered by the output capacitor C11. Capacitor C11 has low ESR to reduce output voltage ripple. The output does not need an LC post filter.

Secondary RC-snubber (R8 and C6) is used across D11 to reduce radiated EMI.

4.4 Overvoltage Protection

In the event of a fault condition, the LYTSwitch-2 IC enters a protection mode. If the FEEDBACK pin voltage falls below 0.7 V during the flyback period (tAR(ON)) the converter enters auto-restart. Subsequently, if the FEEDBACK pin current during the forward period of the conduction cycle falls below 120 μA, the converter infers an open-loop condition and inhibits switching. Refer to the data sheet for details of the auto-restart and open-loop protection features of the LYTSwitch-2 family of ICs.
4.5 PCB Layout

Figure 3 – Printed Circuit Layout, Top. (2.5 in [63.5 mm] L x 1.15 in [29.2 mm] W)

Figure 4 – Printed Circuit Layout, Bottom.
5 PCB Assembly

Figure 5 – PCB Assembly Top.

Figure 6 – PCB Assembly Bottom, Showing the LYTSwitch-IC.
# 6 Bill of Materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Qty</th>
<th>Ref Des</th>
<th>Description</th>
<th>Mfg Part Number</th>
<th>Mfg</th>
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<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>C1 C2</td>
<td>4.7 (\mu)F, 400 V, Electrolytic, (8 x 11.5)</td>
<td>SHD400WV 4.7uF</td>
<td>Sam Young</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>C3</td>
<td>1 (\mu)F, 1000 V, Ceramic, X7R, 0805</td>
<td>C0805C102KDRACTU</td>
<td>Kemet</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>C4</td>
<td>1 (\mu)F, 25 V, Ceramic, X7R, 1206</td>
<td>C3216X7R1E105K</td>
<td>TDK</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>C5</td>
<td>10 (\mu)F, 100 V, Electrolytic, Gen. Purpose, (6.3 x 11)</td>
<td>EKMG101ELL100MF11D</td>
<td>Nippon Chemi-Con</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>C6</td>
<td>1 (\mu)F, 200 V, Ceramic, X7R, 0805</td>
<td>08052C102KAT2A</td>
<td>AVX</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>C11 C7 (Opt)</td>
<td>470 (\mu)F, 35 V, Electrolytic, Low ESR, 52 m(\Omega), (10 x 20)</td>
<td>ELXZ350ELL471MJ20S</td>
<td>Nippon Chemi-Con</td>
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<tr>
<td>7</td>
<td>2</td>
<td>C8 C10</td>
<td>100 nF, 400 V, Film</td>
<td>ECQ-E4104KF</td>
<td>Panasonic</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>C9</td>
<td>2.2 (\mu)F, Ceramic, Y1</td>
<td>440LD22-R</td>
<td>Vishay</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>C12 (Opt)</td>
<td>47 nF, 630 V, Film</td>
<td>ME2PD24704J</td>
<td>Duratech</td>
</tr>
<tr>
<td>10</td>
<td>5</td>
<td>D1 D2 D5  D6 D7</td>
<td>1000 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)</td>
<td>DL4007-13-F</td>
<td>Diodes, Inc.</td>
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<tr>
<td>11</td>
<td>2</td>
<td>D3 D4</td>
<td>1000 V, 1 A, Rectifier, DO-41</td>
<td>1N4007-E3/54</td>
<td>Vishay</td>
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<tr>
<td>12</td>
<td>1</td>
<td>D9</td>
<td>1000 V, 1 A, Rectifier, Glass Passivated, 2 us, DO-41</td>
<td>1N4007GP</td>
<td>Vishay</td>
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<tr>
<td>13</td>
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<td>D10</td>
<td>250 V, 0.2 A, Fast Switching, 50 ns, SOD-123</td>
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<td>14</td>
<td>1</td>
<td>D11</td>
<td>200 V, 1 A, DIODE SCHOTTKY 1 A 200 V PWRDI 123</td>
<td>DFSL1200-7</td>
<td>Diodes, Inc.</td>
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<tr>
<td>15</td>
<td>1</td>
<td>L1</td>
<td>10 mH, 0.076 A, 20%</td>
<td>RL-5480-3-10000</td>
<td>Renco</td>
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<tr>
<td>16</td>
<td>1</td>
<td>R1</td>
<td>10 k(\Omega), 5%, 1/8 W, Thick Film, 0805</td>
<td>ERJ-6GEYJ103V</td>
<td>Panasonic</td>
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<tr>
<td>17</td>
<td>1</td>
<td>R2</td>
<td>1 (\Omega), 5%, 1/2 W, Carbon Film</td>
<td>CFR-50J5-1R0</td>
<td>Yageo</td>
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<tr>
<td>18</td>
<td>1</td>
<td>R3</td>
<td>330 k(\Omega), 5%, 1/4 W, Thick Film, 1206</td>
<td>ERJ-8GEYJ334V</td>
<td>Panasonic</td>
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<tr>
<td>19</td>
<td>1</td>
<td>R4</td>
<td>300 (\Omega), 5%, 1/8 W, Thick Film, 0805</td>
<td>ERJ-6GEYJ301V</td>
<td>Panasonic</td>
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<tr>
<td>20</td>
<td>1</td>
<td>R5</td>
<td>54.9 (k\Omega), 1%, 1/8 W, Thick Film, 0805</td>
<td>ERJ-6ENF5492V</td>
<td>Panasonic</td>
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<tr>
<td>21</td>
<td>1</td>
<td>R6</td>
<td>4.99 (k\Omega), 1%, 1/8 W, Thick Film, 0805</td>
<td>ERJ-6ENF4991V</td>
<td>Panasonic</td>
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<tr>
<td>22</td>
<td>1</td>
<td>R7</td>
<td>12 (k\Omega), 5%, 1/4 W, Thick Film, 1206</td>
<td>ERJ-8GEYJ123V</td>
<td>Panasonic</td>
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<tr>
<td>23</td>
<td>1</td>
<td>R8</td>
<td>100 (\Omega), 5%, 1/8 W, Thick Film, 0805</td>
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<td>Panasonic</td>
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<td>24</td>
<td>1</td>
<td>R9</td>
<td>510 (\Omega), 5%, 1/8 W, Thick Film, 0805</td>
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<tr>
<td>25</td>
<td>1</td>
<td>RF1</td>
<td>10 O, 2 W, Wire Wound Fusible</td>
<td>FW20A10R0JA</td>
<td>Bourns</td>
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<td>26</td>
<td>1</td>
<td>T1</td>
<td>Bobbin, EE13, Horizontal, 8 pins Transformer</td>
<td>Custom SNX-R1748</td>
<td>Custom Santronics</td>
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<td>27</td>
<td>1</td>
<td>U1</td>
<td>LYTSwitch-2, CV/CC, SO-8D</td>
<td>LYT2003D</td>
<td>Power Integrations</td>
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**Mechanical BOM**

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<td>J3</td>
<td>Wire, UL1007, #22 AWG, Red, PVC, 4 inches</td>
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<tr>
<td>2</td>
<td>1</td>
<td>J4</td>
<td>Wire, UL1007, #22 AWG, Blk, PVC, 4 inches</td>
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<tr>
<td>3</td>
<td>1</td>
<td>J1</td>
<td>Wire, UL1007, #22 AWG, Wht, PVC, 4 inches</td>
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<td>4</td>
<td>1</td>
<td>J2</td>
<td>Wire, UL1007, #22 AWG, Blu, PVC, 4 inches</td>
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7 Transformer Specification

7.1 Electrical Diagram

![Transformer Electrical Diagram](image)

Figure 7 – Transformer Electrical Diagram.

7.2 Electrical Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Description</th>
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<tbody>
<tr>
<td>Electrical Strength</td>
<td>1 second, 60 Hz, from pins 1-3 to pins 8-9.</td>
</tr>
<tr>
<td>Primary Inductance</td>
<td>Pins 3-4, all other windings open, measured at 100 kHz, 0.4 $V_{RMS}$.</td>
</tr>
<tr>
<td>Resonant Frequency</td>
<td>Pins 3-4 all other windings open.</td>
</tr>
<tr>
<td>Primary Leakage Inductance</td>
<td>Pins 1-2, and pins 5-7 shorted, measured at 100 kHz, 0.4 $V_{RMS}$.</td>
</tr>
</tbody>
</table>

7.3 Materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>Core: EE13, PC34, $AL = 94nH/A^2 \pm 10%$.</td>
</tr>
<tr>
<td>[2]</td>
<td>Bobbin: EE13;4/4 pin; Extended horizontal; Hical magnetics-548 or equivalent (PI part number 25-00002-00)</td>
</tr>
<tr>
<td>[5]</td>
<td>Magnet Wire: #34 AWG.</td>
</tr>
</tbody>
</table>
7.4 **Transformer Build Diagram**

![Transformer Build Diagram](image)

**Figure 8 – Transformer Build Diagram.**

7.5 **Transformer Construction**

<table>
<thead>
<tr>
<th>Bobbin Preparation</th>
<th>For the purpose of these instructions, bobbin is oriented on winder such that pin 1 side is on the left. Winding direction is counter-clockwise. Follow the pin number assignment in the specification. Construction description starts with the wire closest to the bobbin. Construction description starts with the wire closest to the bobbin. Cut pin number 6.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>WDG1; Cancellation Winding</strong></td>
<td>Wound 20 turns (x 2 filar) of Item [5] and solder the start of this winding at pin 4. Spread the winding evenly across the entire bobbin. Finish this winding by temporarily (do not solder) winding it on pin 8. Leave this end of primary shield winding not connected. Bend the end 90 degrees with respect to the wound wire and cut this wire in the middle of the bobbin.</td>
</tr>
<tr>
<td>Insulation</td>
<td>Add 2 layer of tape, item [7], for insulation.</td>
</tr>
<tr>
<td><strong>WDG2; Primary Winding</strong></td>
<td>Wound 108 turns (x 1 filar) of Item [4], terminating this start at pin 3 (soldered). Spread the winding evenly across the entire bobbin in four layers, placing two layers of tape, Item [7], in between layers. Finish this winding on pin 4 (soldered).</td>
</tr>
<tr>
<td>Insulation</td>
<td>Add 2 layers of tape, item [7], for insulation.</td>
</tr>
<tr>
<td><strong>WDG3; Bias Winding</strong></td>
<td>Wound 29 turns (x 2 filar) of Item [6], soldering this start on pin 2. Spread the winding evenly across the entire bobbin. Terminate the end of this winding on pin 1 (soldered).</td>
</tr>
<tr>
<td>Insulation</td>
<td>Add 2 layers of tape, item [7], for insulation.</td>
</tr>
<tr>
<td><strong>WDG4; Secondary Winding</strong></td>
<td>Wound 30 turns (x 1 filar) of Item [3], terminating this start on pin 5 (soldered). Evenly spread the winding across the bobbin. Terminate this end on pin 7 (soldered).</td>
</tr>
<tr>
<td>Insulation</td>
<td>Add 2 layers of tape, item [7], for insulation.</td>
</tr>
<tr>
<td>Core Preparation</td>
<td>Grind one of the cores to get the desired inductance. Wrap with 2 layers of tape to secure the cores together.</td>
</tr>
<tr>
<td>Varnish</td>
<td>Dip the transformer to the varnish Item [8], then, dry.</td>
</tr>
</tbody>
</table>
## 8 Transformer Design Spreadsheet

<table>
<thead>
<tr>
<th>ACDC_LYTSwitch-2_102413; Rev.1.0; Copyright Power Integrations 2013</th>
<th>INPUT</th>
<th>INFO</th>
<th>OUTPUT</th>
<th>UNIT</th>
<th>ACDC_LYTSwitch-2_102413_Rev1-0; Discontinuous Flyback Transformer Design Spreadsheet</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ENTER APPLICATION VARIABLES</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VACMIN</td>
<td>120</td>
<td></td>
<td>120.00</td>
<td>V</td>
<td>Minimum AC Input Voltage</td>
</tr>
<tr>
<td>VACMAX</td>
<td>265</td>
<td></td>
<td>265.00</td>
<td>V</td>
<td>Maximum AC Input Voltage</td>
</tr>
<tr>
<td>fL</td>
<td>50</td>
<td></td>
<td>50.00</td>
<td>Hz</td>
<td>AC Mains Frequency</td>
</tr>
<tr>
<td>Application Type</td>
<td>Ballast</td>
<td>Ballast</td>
<td>Choose application type</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VO</td>
<td>24.00</td>
<td>24.00</td>
<td>V</td>
<td>Output Voltage (at continuous power)</td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>0.17</td>
<td>0.17</td>
<td>A</td>
<td>Power Supply Output Current (corresponding to peak power)</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>4.08</td>
<td>W</td>
<td>Continuous Output Power</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n</td>
<td>0.80</td>
<td>0.80</td>
<td>Efficiency Estimate at output terminals</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td>0.50</td>
<td></td>
<td>Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TC</td>
<td>3.00</td>
<td>ms</td>
<td>Bridge Rectifier Conduction Time Estimate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>9.40</td>
<td>9.40</td>
<td>uF</td>
<td>Input Capacitance</td>
<td></td>
</tr>
<tr>
<td><strong>ENTER LYTSwitch-2 VARIABLES</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chosen Device</td>
<td>LYT2003D</td>
<td>LYT2003D</td>
<td>Chosen LYTSwitch-2 device</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILIMITMIN</td>
<td>0.36</td>
<td>A</td>
<td>Minimum Current Limit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILIMITTPY</td>
<td>0.39</td>
<td>A</td>
<td>Typical Current Limit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILIMITMAX</td>
<td>0.42</td>
<td>A</td>
<td>Maximum Current Limit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FS</td>
<td>60.00</td>
<td></td>
<td>60.00</td>
<td>kHz</td>
<td>Typical Device Switching Frequency at maximum power</td>
</tr>
<tr>
<td>VOR</td>
<td>73.66</td>
<td>V</td>
<td>Reflected Output Voltage (VOR &lt; 135 V Recommended)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDS</td>
<td>10.00</td>
<td>V</td>
<td>LYTSwitch-2 on-state Drain to Source Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VD</td>
<td>0.50</td>
<td>V</td>
<td>Output Winding Diode Forward Voltage Drop</td>
<td></td>
<td></td>
</tr>
<tr>
<td>KP_WORST_CASE</td>
<td>2.41</td>
<td></td>
<td>KP assuming minimum LP, VMIN, and Maximum Switching Frequency. Ensure that this value is above 1.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FEEDBACK WINDING PARAMETERS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NFB</td>
<td>29.00</td>
<td></td>
<td>29.00</td>
<td>Feedback winding turns</td>
<td></td>
</tr>
<tr>
<td>VFLY</td>
<td>19.74</td>
<td>V</td>
<td>Flyback Voltage - Voltage on Feedback Winding during switch off time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VFOR</td>
<td>39.10</td>
<td>V</td>
<td>Forward voltage - Voltage on Feedback Winding during switch on time</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>BIAS WINDING PARAMETERS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VB</td>
<td>N/A</td>
<td>V</td>
<td>Feedback Winding Voltage (VFLY) is greater than 10 V. The feedback winding itself can be used to provide external bias to the LinkSwitch. Additional Bias winding is not required.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NB</td>
<td>N/A</td>
<td></td>
<td>Bias Winding number of turns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>REXT</td>
<td>29.00</td>
<td>k-ohm</td>
<td>Suggested value of BYPASS pin resistor (use standard 5% resistor)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DESIGN PARAMETERS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DCON</td>
<td>4.60</td>
<td>us</td>
<td>Output diode conduction time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TON</td>
<td>2.33</td>
<td>us</td>
<td>LYTSwitch-2 On-time (calculated at minimum inductance)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RUPPER</td>
<td>Info</td>
<td>46.41</td>
<td>k-ohm</td>
<td>Upper resistor in Feedback resistor divider. Once the initial prototype is running, it is necessary to use the fine tuning section of this spreadsheet to adjust to the correct output current</td>
<td></td>
</tr>
<tr>
<td>RLOWER</td>
<td>5.06</td>
<td>k-ohm</td>
<td>Lower resistor in resistor divider</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core Type</td>
<td>Bobbin</td>
<td>Core Effective Cross Sectional Area</td>
<td>Bobbin part number</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>-----------------------------------</td>
<td>-------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AE</td>
<td>17.10</td>
<td>mm²</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LE</td>
<td>30.20</td>
<td>mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AL</td>
<td>1130.00</td>
<td>nH/turn²</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>7.40</td>
<td>mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>0.00</td>
<td>mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>3.00</td>
<td>Number of Primary Layers</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NS</td>
<td>36.00</td>
<td>Number of Secondary Turns. To adjust Secondary number of turns change DCON</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DC INPUT VOLTAGE PARAMETERS**

| VMIN     | 145.62 V | Minimum DC bus voltage          |
| VMAX     | 374.77 V | Maximum DC bus voltage          |

**CURRENT WAVEFORM SHAPE PARAMETERS**

| DMAX     | 0.17     | Maximum duty cycle measured at VMIN |
| IAVG     | 0.04 A   | Input Average current            |
| IP       | 0.36 A   | Peak primary current             |
| IR       | 0.36 A   | Primary ripple current           |
| IRMS     | 0.10 A   | Primary RMS current              |

**TRANSFORMER PRIMARY DESIGN PARAMETERS**

| LPMIN    | 933.39 uH | Minimum Primary Inductance        |
| LPTYP    | 1037.10 uH| Typical Primary inductance        |
| LP_TOLERANCE | 10.00 % | Tolerance in primary inductance   |
| NP       | 108.00    | Primary number of turns. To adjust Primary number of turns change BM_TARGET |
| ALG      | 88.91 nH/turn² | Gapped Core Effective Inductance |
| BM_TARGET | 2190.06 Gauss | Target Flux Density |
| BM       | 2190.06 Gauss | Maximum Operating Flux Density (calculated at nominal inductance), BM < 2500 is recommended |
| BP       | 2575.85 Gauss | Peak Operating Flux Density (calculated at maximum inductance and max current limit), BP < 3000 is recommended |
| BAC      | 1095.03 Gauss | AC Flux Density for Core Loss Curves (0.5 X Peak to Peak) |
| ur       | 158.81 Cmils | Relative Permeability of Ungapped Core |
| LG       | 0.25 mm   | Gap Length (LG > 0.1 mm)          |
| BWE      | 22.20 mm  | Effective Bobbin Width            |
| OD       | 0.21 mm   | Maximum Primary Wire Diameter including insulation |
| INS      | 0.04 mm   | Estimated Total Insulation Thickness (= 2 * film thickness) |
| DIA      | 0.16 mm   | Bare conductor diameter           |
| AWG      | 34 AWG    | Primary Wire Gauge (Rounded to next smaller standard AWG value) |
| CM       | 40.32 Cmils | Bare conductor effective area in circular mils |
| CMA      | 401.84 Cmils/A | Primary Winding Current Capacity (200 < CMA < 500) |

**TRANSFORMER SECONDARY DESIGN PARAMETERS**

| ISP      | 1.09 A   | Peak Secondary Current           |
| ISRMS    | 0.42 A   | Secondary RMS Current            |
| Iripple  | 0.39 A   | Output Capacitor RMS Ripple Current |
| CMS      | 84.64 Cmils | Secondary Bare Conductor minimum circular mils |
| AWGS     | 30.00 Cmils | Secondary Wire Gauge (Rounded up to next larger standard AWG value) |

**VOLTAGE STRESS PARAMETERS**

| VDRAIN   | 549.45 V | Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance) |
### PIVS
- **Output Rectifier Maximum Peak Inverse Voltage**: 148.92 V

### FINE TUNING

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUPPER_ACTUAL</td>
<td>52.30</td>
<td>k-ohm</td>
<td>Actual Value of upper resistor (RUPPER) used on PCB</td>
</tr>
<tr>
<td>RLOWER_ACTUAL</td>
<td>4.99</td>
<td>k-ohm</td>
<td>Actual Value of lower resistor (RLOWER) used on PCB</td>
</tr>
<tr>
<td>Actual (Measured) Output Voltage (VDC)</td>
<td>22.87</td>
<td>V</td>
<td>Measured Output voltage from first prototype</td>
</tr>
<tr>
<td>Actual (Measured) Output Current (ADC)</td>
<td>0.17</td>
<td>Amps</td>
<td>Measured Output current from first prototype</td>
</tr>
<tr>
<td>RUPPER_FINE</td>
<td>54.89</td>
<td>k-ohm</td>
<td>New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 54.9 k-ohms</td>
</tr>
<tr>
<td>RLOWER_FINE</td>
<td>4.97</td>
<td>k-ohm</td>
<td>New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 4.99 k-ohms</td>
</tr>
</tbody>
</table>

Note: VACMIN = 120 V to guarantee start-up at 190 V for a valley-fill circuit.
9 Performance Data
All measurements performed at room temperature unless specified.

9.1 Efficiency

![Graph showing Efficiency vs. Input Voltage, Room Temperature, 50 Hz.](Figure 9)

<table>
<thead>
<tr>
<th>V&lt;sub&gt;IN&lt;/sub&gt; (V&lt;sub&gt;RMS&lt;/sub&gt;)</th>
<th>I&lt;sub&gt;IN&lt;/sub&gt; (A&lt;sub&gt;RMS&lt;/sub&gt;)</th>
<th>P&lt;sub&gt;IN&lt;/sub&gt; (W)</th>
<th>PF</th>
<th>V&lt;sub&gt;OUT&lt;/sub&gt; (V&lt;sub&gt;DC&lt;/sub&gt;)</th>
<th>I&lt;sub&gt;OUT&lt;/sub&gt; (A&lt;sub&gt;DC&lt;/sub&gt;)</th>
<th>P&lt;sub&gt;OUT&lt;/sub&gt; (W)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>179.93</td>
<td>0.03</td>
<td>4.93</td>
<td>0.783</td>
<td>23.98</td>
<td>0.17</td>
<td>3.96</td>
<td>80.21</td>
</tr>
<tr>
<td>199.91</td>
<td>0.03</td>
<td>4.94</td>
<td>0.767</td>
<td>23.98</td>
<td>0.17</td>
<td>3.96</td>
<td>80.05</td>
</tr>
<tr>
<td>219.97</td>
<td>0.03</td>
<td>4.96</td>
<td>0.748</td>
<td>23.98</td>
<td>0.17</td>
<td>3.96</td>
<td>79.67</td>
</tr>
<tr>
<td>229.91</td>
<td>0.03</td>
<td>4.98</td>
<td>0.738</td>
<td>23.97</td>
<td>0.17</td>
<td>3.95</td>
<td>79.47</td>
</tr>
<tr>
<td>263.99</td>
<td>0.03</td>
<td>5.03</td>
<td>0.672</td>
<td>23.96</td>
<td>0.17</td>
<td>3.95</td>
<td>78.60</td>
</tr>
</tbody>
</table>

Table 1 – Data for Figure 9.
9.2 **Active Mode Efficiency**

![Graph showing efficiency vs load](image)

**Figure 10** – Efficiency vs Load, 230 V\(_{\text{RMS}}\) / 50 Hz line, Room Temperature.
Table 2 – Data for Figure 10.

For adapter applications that require compliance to ENERGY STAR, the external power supply requirements indicated in 8.2.1 and 8.2.2 describes active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined by the nameplate output power and the output voltage as shown in the tables in 8.2.1 and 8.2.2. The efficiency is the average efficiency measure at 25, 50, 75 and 100% load.

The measurements are done at a single rated input voltage for power supplies that are specified at either low line (115 VAC) or high line (230 VAC) only. For this design, 230 VAC was selected.

The approved test method can be found here:
For the latest up to date information, please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

9.2.1 USA Energy Independence and Security Act 2007
This legislation mandates all single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

<table>
<thead>
<tr>
<th>Nameplate Output (Pₒ)</th>
<th>Minimum Efficiency in Active Mode of Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 1 W</td>
<td>0.5 × Pₒ</td>
</tr>
<tr>
<td>≥ 1 W to ≤ 51 W</td>
<td>0.09 × ln (Pₒ) + 0.5</td>
</tr>
<tr>
<td>&gt; 51 W</td>
<td>0.85</td>
</tr>
</tbody>
</table>

ln = natural logarithm

No-load Energy Consumption

<table>
<thead>
<tr>
<th>Nameplate Output (Pₒ)</th>
<th>Maximum Power for No-load AC-DC EPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>≤ 0.5 W</td>
</tr>
</tbody>
</table>

This requirement supersedes the legislation from individual US States (for example CEC in California).

9.2.2 ENERGY STAR EPS Version 2.0
This specification took effect on November 1st, 2008.

Active Mode Efficiency Standard Models

<table>
<thead>
<tr>
<th>Nameplate Output (Pₒ)</th>
<th>Minimum Efficiency in Active Mode of Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>≤ 1 W</td>
<td>0.48 × Pₒ + 0.14</td>
</tr>
<tr>
<td>&gt; 1 W to ≤ 49 W</td>
<td>0.0626 × ln (Pₒ) + 0.622</td>
</tr>
<tr>
<td>&gt; 49 W</td>
<td>0.87</td>
</tr>
</tbody>
</table>

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (Vₒ≤6 V and Iₒ ≥ 550 mA)

<table>
<thead>
<tr>
<th>Nameplate Output (Pₒ)</th>
<th>Minimum Efficiency in Active Mode of Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>≤ 1 W</td>
<td>0.497 × Pₒ + 0.067</td>
</tr>
<tr>
<td>&gt; 1 W to ≤ 49 W</td>
<td>0.075 × ln (Pₒ) + 0.561</td>
</tr>
<tr>
<td>&gt; 49 W</td>
<td>0.86</td>
</tr>
</tbody>
</table>

ln = natural logarithm

No-load Energy Consumption (both models)

<table>
<thead>
<tr>
<th>Nameplate Output (Pₒ)</th>
<th>Maximum Power for No-load AC-DC EPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to &lt; 50 W</td>
<td>≤ 0.3 W</td>
</tr>
<tr>
<td>≥ 50 W to ≤ 250 W</td>
<td>≤ 0.5 W</td>
</tr>
</tbody>
</table>
9.3 No-Load Input Power

![Graph showing No-Load Input Power vs. Input Line Voltage](image)

**Figure 11** – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 50 Hz.

**Table 3** – Data for Figure 11.

<table>
<thead>
<tr>
<th>Input</th>
<th>Input Measurement</th>
<th>Output Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VAC (V&lt;sub&gt;RMS&lt;/sub&gt;)</td>
<td>Freq (Hz)</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; (V&lt;sub&gt;RMS&lt;/sub&gt;)</td>
</tr>
<tr>
<td>180</td>
<td>50</td>
<td>179.94</td>
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<td>199.92</td>
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<tr>
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<td>229.91</td>
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<tr>
<td>240</td>
<td>50</td>
<td>239.94</td>
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<tr>
<td>264</td>
<td>50</td>
<td>263.97</td>
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9.4 Regulation

9.4.1 Output Voltage vs. Load

Figure 12 – $V_{\text{OUT}}$ Regulation vs. Load, Room Temperature.
9.4.2 Output Voltage vs. Line

Figure 13 – $V_{\text{OUT}}$ Regulation vs. AC Input Voltage, Room Temperature, Full Load and 50 Hz.
9.5  **Power Factor (PF)**

![Graph showing Power Factor vs. AC Input, Full Load.](image)

**Figure 14** – Power Factor vs. AC Input, Full Load.
9.6 CV/CC Curve

Load resistance is reduced from 1,500 Ω down to the point the unit will enter auto-restart.

![CV/CC Curve Using CR Mode of Electronic Load](image)

**Figure 15** – CV/CC Curve Using CR Mode of Electronic Load.
9.7 **Power Curve**

![Power Curve in CR Mode from Electronic Load](image)

**Figure 16** – Power Curve in CR Mode from Electronic Load.
9.8 Thermal Performance

9.8.1 Thermal Images
Thermals measurements were taken without enclosure (open frame). Temperatures were allowed to stabilize for >60 minutes prior to taking the thermal images.

9.8.2 Test Conditions (190 VAC, 50 Hz, 25 °C Ambient)

9.8.2.1 Component Side

Figure 17 – Top side component guide for thermal scan.

Figure 18 – SP1 – Valley Fill PFC Capacitor (C2).
SP2 – Transformer (T1).
SP3 – Primary Snubber Diode (D9).

Figure 19 – SP1 – Bias Capacitor (C5).
SP2 – Output Capacitor (C11).
SP3 – Valley Fill PFC Capacitor (C1).
9.8.2.2 Solder Side

Figure 20 – Bottom side component guide for thermal scan.

Figure 21 – SP1 – LYT2003D (U1).
SP2 – Output Diode (D11).
SP3 – Bridge Diode (D2).
9.8.3 Test Conditions (265 VAC, 50 Hz, 25 °C Ambient)

9.8.3.1 Component Side

Figure 22 – Top side component guide for thermal scan.

Figure 23 – SP1 – Transformer (T1).  
SP2 – Valley Fill PFC Capacitor (C2).  
SP3 – Primary Snubber Diode (D9).

Figure 24 – SP1 – Bias Capacitor (C5).  
SP2 – Output Capacitor (C11).  
SP3 – Valley Fill PFC Capacitor (C1).
9.8.3.2 Solder Side

Figure 25 – Bottom side component guide for thermal scan.

Figure 26 – SP1 – LYT2003D (U1).
SP2 – Output Diode (D11).
SP3 – Bridge Diode (D2).
10 Waveforms

10.1 Input Voltage and Current, Normal Operation

Figure 27 – 190 VAC, Full Load.
Pink: $I_{IN}$, 50 mA / div.
Blue (Sinusoidal Wave): $V_{IN}$, 100 V, 5 ms / div.

Figure 28 – 220 VAC, Full Load.
Pink: $I_{IN}$, 50 mA / div.
Blue (Sinusoidal Wave): $V_{IN}$, 100 V, 5 ms / div.

Figure 29 – 240 VAC, Full Load.
Pink: $I_{IN}$, 50 mA / div.
Blue (Sinusoidal Wave): $V_{IN}$, 100 V, 5 ms / div.

Figure 30 – 265 VAC, Full Load.
Pink: $I_{IN}$, 50 mA / div.
Blue (Sinusoidal Wave): $V_{IN}$, 100 V, 5 ms / div.
10.2 Drain Voltage and Current, Normal Operation

Figure 31 – 190 VAC, Full Load.
Upper: $V_{\text{DRAIN}}$, 200 V
Lower: $I_{\text{DRAIN}}$, 0.2 A / div., 1 ms / div.

Figure 32 – 190 VAC, Full Load.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.2 A / div., 400 $\mu$s / div.
Zoom Time Scale: 4 $\mu$s / div.

Figure 33 – 230 VAC, Full Load.
Upper: $V_{\text{DRAIN}}$, 200 V.
Lower: $I_{\text{DRAIN}}$, 0.2 A / div., 1 ms / div.

Figure 34 – 230 VAC, Full Load.
Upper Frame: Normal Sample; 1 ms / div.
Lower Frame: Zoom Center; 2 $\mu$s / div.
Upper: $V_{\text{DRAIN}}$, 200 V.
Lower: $I_{\text{DRAIN}}$, 0.2 A / div., 1 ms / div.
10.3 Drain Voltage and Current Start-up Profile

No saturation or any possible cause of failure.
Figure 39 – 265 VAC Input and Full Load.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.4 A / div.
Time Scale: 2 ms / div.

Figure 40 – 265 VAC Input and Full Load.
Upper Frame: Normal Sample; 1 ms / div.
Lower Frame: Zoom Center; 2 $\mu$s / div.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.4 A / div.
### 10.4 Drain Voltage and Current Start-up Short Waveform

**Figure 41** – 190 VAC Input and Shorted Load.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.2 A / div.
Time Scale: 2 ms / div.

**Figure 42** – 190 VAC Input and Shorted Load.
Upper Frame: Normal Sample; 2 ms / div.
Lower Frame: Zoom Center; 40 $\mu$s / div.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.2 A / div.

**Figure 43** – 265 VAC Input and Shorted Load.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.2 A / div.
Time Scale: 4 ms / div.

**Figure 44** – 265 VAC Input and Shorted Load.
Upper Frame: Normal sample; 4 ms / div.
Lower Frame: Zoom Center; 88 $\mu$s / div.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.4 A / div.
10.5 Drain Voltage and Current Normal Running Short Waveform

Figure 45 – 265 VAC Input, Full Load then Short. 266 ms Continuous Switching.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.4 A / div.
Time Scale: 500 ms / div.

Figure 46 – 265 VAC Input, Full Load then Short.
850 ms Off Time between Auto-Restarts.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.4 A / div.
Time Scale: 500 ms / div.

Figure 47 – 265 VAC Input, Full Load then Short.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.2 A / div.
Time Scale: 20 ms / div.

Figure 48 – 265 VAC Input, Full Load then Short.
Upper Frame: Normal Sample; 40 $\mu$s / div.
Lower Frame: Zoom Center; 12 $\mu$s / div.
Upper: $V_{\text{DRAIN}}$, 200 V / div.
Lower: $I_{\text{DRAIN}}$, 0.2 A / div.
10.6 Output Diode Waveforms at Normal Operation

Figure 49 – 190 VAC Input, Normal Operation.
Upper: $I_{\text{DIODE}}$, 1 A / div.
Lower: $V_{\text{DIODE}}$, 40 V / div.
Time Scale: 10 $\mu$s / div.

Figure 50 – 265 VAC Input, Normal Operation.
Upper: $I_{\text{DIODE}}$, 1 A / div.
Lower: $V_{\text{DIODE}}$, 40 V / div.
Time Scale: 10 $\mu$s / div.

10.7 Output Diode Waveforms at Start-up

Figure 51 – 190 VAC Input, Start-up.
Upper Frame: Normal Sample; 520 $\mu$s / div.
Lower Frame: Zoom; 56 $\mu$s / div.
Upper: $I_{\text{DIODE}}$, 1 A / div.
Lower: $V_{\text{DIODE}}$, 50 V / div.

Figure 52 – 265 VAC Input, Normal Operation.
Upper Frame: Normal Sample; 520 $\mu$s / div.
Lower Frame: Zoom; 56 $\mu$s / div.
Upper: $I_{\text{DIODE}}$, 1 A / div.
Lower: $V_{\text{DIODE}}$, 50 V / div.
10.8 Diode Start-up Short Waveforms

Figure 53 – 190 VAC Input and Shorted Load.
Upper Frame: Normal Sample; 520 μs / div.
Lower Frame: Zoom; 56 μs / div.
Upper: $I_{DIODE}$, 1 A / div.
Lower: $V_{DIODE}$, 50 V / div.

Figure 54 – 265 VAC Input and Shorted Load.
Upper Frame: Normal Sample; 520 μs / div.
Lower Frame: Zoom; 56 μs / div.
Upper: $I_{DIODE}$, 1 A / div.
Lower: $V_{DRAIN}$, 50 V / div.

10.1 Output Diode Normal Running Short Waveforms

Figure 55 – 190 VAC Input and Shorted Load. Upper Frame: Normal Sample; 1 ms / div.
Lower Frame: Zoom Center; 56 μs / div.
Upper: $I_{DIODE}$, 1 A / div.
Lower: $V_{AK-DIODE}$, 50 V / div.

Figure 56 – 265 VAC Input and Shorted Load.
Upper: $I_{DIODE}$, 1 A / div.
Lower: $V_{AK-DIODE}$, 50 V / div.
Time Scale: 200 ms / div.
10.2 Output Voltage Start-up Profile

Figure 57 – Start-up Profile, 190 VAC.
Upper: \( V_{IN} \), 200 V / div.
Lower: \( V_{OUT} \), 10 V / div.
Time Scale: 40 ms / div.

Figure 58 – Start-up Profile, 265 VAC.
Upper: \( V_{IN} \), 200 V / div.
Lower: \( V_{OUT} \), 10 V / div.
Time Scale: 40 ms / div.

10.1 Output Voltage and Output Current at Normal Operation

Figure 59 – \( V_{OUT} \) and \( I_{OUT} \), 190 VAC.
Upper: \( V_{OUT} \), 5 V / div.
Lower: \( I_{OUT} \), 50 mA / div.
Time Scale: 2 ms / div.

Figure 60 – \( V_{OUT} \) and \( I_{OUT} \), 230 VAC.
Upper: \( V_{OUT} \), 5 V / div.
Lower: \( I_{OUT} \), 50 mA / div.
Time Scale: 2 ms / div.
10.2 Load Transient Response (0% to 100% and from 50% to 100% Load Step)
In the figures shown below, both AC coupling and DC coupling for the $V_{OUT}$ waveforms are shown.

**Figure 61** – $V_{OUT}$ and $I_{OUT}$, 265 VAC.
Upper: $V_{OUT}$, 5 V / div.
Lower: $I_{OUT}$, 50 mA / div.
Time Scale: 2 ms / div.

**Figure 62** – Transient Response, 230 VAC, 0-100-0%
Load Step for Worst Case Condition at 100 Hz.
Upper: $V_{OUT}$, 200 mV / div. AC Coupling.
Lower: $I_{OUT}$, 100 mA / div.
Time Scale: 2 ms / div.

**Figure 63** – Transient Response, 230 VAC, 0-100-0%
Load Step for Worst Case Condition at 100 Hz.
Upper Frame: Normal Sample; 40 ms / div.
Upper: $V_{OUT}$, 2 V / div. DC Coupling.
Lower: $I_{OUT}$, 100 mA / div.
Lower Frame: Zoom Center; 2 ms / div.
Center: $V_{OUT}$, 2 V / div. DC Coupling.
Figure 64 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 1 kHz.
Upper: $V_{OUT}$, 200 mV / div. AC Coupling.
Lower: $I_{OUT}$, 100 mA / div.
Time Scale: 1 ms / div.

Figure 65 – Transient Response, 230 VAC, 0-100-0% Load Step for Worst Case Condition at 1 kHz.
Upper Frame: Normal Sample; 5 ms / div.
Upper: $V_{OUT}$, 2 V / div. DC Coupling.
Lower: $I_{OUT}$, 100 mA / div.
Lower Frame: Zoom Center; 2 ms / div.
Center: $V_{OUT}$, 2 V / div. DC Coupling.

Figure 66 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 100 Hz.
Upper: $V_{OUT}$, 200 mV / div. AC Coupling.
Lower: $I_{OUT}$, 100 mA / div.
Time Scale: 5 ms / div.

Figure 67 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 100 Hz.
Upper Frame: Normal Sample; 5 ms / div.
Upper: $V_{OUT}$, 2 V / div. DC Coupling.
Lower: $I_{OUT}$, 100 mA / div.
Lower Frame: Zoom Center; 2 ms / div.
Center: $V_{OUT}$, 2 V / div. DC Coupling.
Figure 68 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 1 kHz. Upper: $V_{OUT}$, 200 mV / div. AC Coupling. Lower: $I_{OUT}$, 100 mA / div. Time Scale: 1 ms / div.

Figure 69 – Transient Response, 230 VAC, 50-100-50% Load Step for Worst Case Condition at 1 kHz. Upper Frame: Normal Sample; 5 ms / div. Upper: $V_{OUT}$, 2 V / div. DC Coupling. Lower: $I_{OUT}$, 100 mA / div. Lower Frame: Zoom Center; 2 ms / div. Center: $V_{OUT}$, 2 V / div. DC Coupling.
10.3 Brown-out Test
No component failure was observed.

Figure 70 – Brown-out, $V_{IN}$ decrements at 1 V / s.
Upper: $V_{IN}$, 200 V / div.
Lower: $V_{OUT}$, 10 V / div.
Time Scale: 20 s / div.

Figure 71 – Brown-in, $V_{IN}$ increments by 1 V / s.
Upper: $V_{IN}$, 200 V / div.
Lower: $V_{OUT}$, 10 V / div.
Time Scale: 20 s / div.

Figure 72 – Brown-out at 1 V / s.
Blue: $V_{IN}$, 200 V / div.
Yellow: $V_{OUT}$, 10 V / div.
Time Scale: 2 s / div.
Zoom Time Scale: 1.5 s / div.

Figure 73 – Brown-in at 1 V / s.
Upper: $V_{IN}$, 200 V / div.
Lower: $V_{OUT}$, 10 V / div.
Time Scale: 200 ms / div.
10.4 Output Ripple Measurements

10.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to noise pickup. Details of the probe modification are provided in the figures below.

To minimize the loop area between the probe (+) and its ground, a short probe is used as shown in the figures below. This is done by wrapping the grounding of the probe with wire and using it, instead, of the usual probe ground wire.

Two capacitors in parallel are utilized to ensure that ripple measurements will not vary from one setup to another. This reduces noise pick from the sets of equipment during testing. One (1) 0.1 μF/50 V ceramic type, preferably, a thru hole type(not shown) and one (1) 1.0 μF/50 V aluminum electrolytic are used as shown. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below). The oscilloscope is set to 20 Mhz bandwidth during measurements.

Figure 74 – Oscilloscope Probe Prepared for Ripple Measurement. (Probe Cap and Ground Lead Removed)

Figure 75 – Ripple Measurement Set-up.
10.4.2 Ripple and Noise Measurement Results

Figure 76 – Ripple, 190 VAC, Full Load. 10 ms / div., 100 mV / div.

Figure 77 – Ripple, 265 VAC, Full Load. 10 ms, 100 mV / div.

Figure 78 – Ripple, 230 VAC, Full Load. 10 ms, 100 mV / div.

Figure 79 – Ripple, 230 VAC, 75% of Full Load. 5 ms, 100 mV / div.
**Figure 80** – Ripple, 230 VAC, 50% of Full Load.  
10 ms, 100 mV / div.

**Figure 81** – Ripple, 230 VAC, 25% of Full Load.  
10 ms, 100 mV / div.

**Figure 82** – Ripple, 230 VAC, 12.5% of Full Load.  
10 ms, 100 mV / div.

**Figure 83** – Ripple, 230 VAC, No-Load.  
10 ms, 100 mV / div.
12 Line Surge

Differential Ring input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

<table>
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<tr>
<th>Surge Level (V)</th>
<th>Input Voltage (VAC)</th>
<th>Injection Location</th>
<th>Injection Phase (°)</th>
<th>Test Result (Pass/Fail)</th>
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<tbody>
<tr>
<td>+2500</td>
<td>230</td>
<td>L to N</td>
<td>90</td>
<td>Pass</td>
</tr>
<tr>
<td>-25000</td>
<td>230</td>
<td>L to N</td>
<td>90</td>
<td>Pass</td>
</tr>
<tr>
<td>+2500</td>
<td>230</td>
<td>L to N</td>
<td>0</td>
<td>Pass</td>
</tr>
<tr>
<td>-25000</td>
<td>230</td>
<td>L to N</td>
<td>0</td>
<td>Pass</td>
</tr>
</tbody>
</table>

Unit passes under all test conditions.

Differential input line 1.2/50 μs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

<table>
<thead>
<tr>
<th>Surge Level (V)</th>
<th>Input Voltage (VAC)</th>
<th>Injection Location</th>
<th>Injection Phase (°)</th>
<th>Test Result (Pass/Fail)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+250</td>
<td>230</td>
<td>L to N</td>
<td>90</td>
<td>Pass</td>
</tr>
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<td>-250</td>
<td>230</td>
<td>L to N</td>
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<td>Pass</td>
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<td>230</td>
<td>L to N</td>
<td>90</td>
<td>Pass</td>
</tr>
</tbody>
</table>

Unit passes under all test conditions.
12.1 Surge Waveforms

12.1.1 Ring Wave Surge

**Figure 84** – Ring Surge of 2.5 kV, 230 VAC at 0°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 1 ms / div.

**Figure 85** – Ring Surge of 2.5 kV, 230 VAC at 0°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 50 μs / div.

**Figure 86** – Ring Surge of 2.5 kV, 230 VAC at 90°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 1 ms / div.

**Figure 87** – Ring Surge of 2.5 kV, 230 VAC at 90°.
Yellow (Overlay): V_{BULK}, 100 V / div.
Red: V_{DS}, 100 V / div.
Time Scale: 50 μs / div.
12.1.2 Differential Surge

Figure 88 – Differential Surge of 2.5 kV, 230 VAC at 0°.
Yellow (Overlay): $V_{BULK}$, 100 V / div.
Red: $V_{DS}$, 100 V / div.
Time Scale: 1 ms / div.

Figure 89 – Differential Surge of 2.5 kV, 230 VAC at 0°.
Yellow (Overlay): $V_{BULK}$, 100 V / div.
Red: $V_{DS}$, 100 V / div.
Time Scale: 1 ms / div.

Figure 90 – Differential Surge of 2.5 kV, 230 VAC at 90°.
Yellow (Overlay): $V_{BULK}$, 100 V / div.
Red: $V_{DS}$, 100 V / div.
Time Scale: 1 ms / div.

Figure 91 – Differential Surge of 2.5 kV, 230 VAC at 90°.
Yellow (Overlay): $V_{BULK}$, 100 V / div.
Red: $V_{DS}$, 100 V / div.
Time Scale: 1 ms / div.
13 Conducted EMI

Figure 92 – Conducted EMI Set-up.

Figure 93 – Conducted EMI Set-up. Unit Under Test and Load.
**Figure 94** – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits (top solid red line is the QP limit while the bottom solid red line is the average limit.). UUT is Floating (Ungrounded and Not on the Metal Plane).

**Table 4** – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. UUT is Floating (Ungrounded and Not on the Metal Plane).
Figure 95 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits (top solid red line is the QP limit while the bottom solid red line is the average limit.). Unit is on Top of Ungrounded Copper Plane.

Table 5 – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit is on Top of Ungrounded Copper Plane.
**Figure 96** – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits (top solid red line is the QP limit while the bottom solid red line is the average limit.). Unit is on Top of Grounded Copper Plane.

**Table 6** – Conducted EMI, Maximum Steady-State Load, 230 VAC, 60 Hz, and EN55015 B Limits. Unit is on Top of Grounded Copper Plane.
## 14 Revision History

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<thead>
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<th>Date</th>
<th>Author</th>
<th>Revision</th>
<th>Description &amp; changes</th>
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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY
Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-89-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@powerint.com

JAPAN
Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caixi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@powerint.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@powerint.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

EUROPE HQ
1st Floor, St. James’s House
East Street, Farnham
Surrey GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

CHINA (SHENZHEN)
3rd Floor, Block A,
Zhongtou International Business
Center, No. 1061, Xiang Mei Rd,
FuTian District, ShenZhen,
China, 518040
Phone: +86-755-8379-3243
Fax: +86-755-8379-5628
e-mail: chinasales@powerint.com

ITALY
Via Milanese 20, 3rd Fl.
20099 Sesto San Giovanni
(MI) Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760