Design Example Report

Title	***2 W Non-Isolated Flyback Power Supply Using LinkSwitch™-3 LNK6404D***
Specification	85 VAC – 265 VAC Input; 5 V, 400 mA Output
Application	Home and Building Automation
Author	Applications Engineering Department
Document Number	DER-880
Date	November 20, 2020
Revision	1.0

Summary and Features

- Highly integrated solution with LNK6404D
- Non-isolated 5 V / 400 mA output (±5%) for home and building automation
- Low component count with integrated 725 V power MOSFET, current sensing and protection
- Compact solution 1" x 1.1" x 0.57"
- <50 mW no-load input power at 230 VAC
- 0 to 40 ºC ambient temperature operation range
- Optimized for <20 dB audible noise performance
- 1 kV differential line surge protection
- Load short-circuit protection
- Over-temperature protection with hysteretic recovery
- EN55022B conducted EMI compliant

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a non-isolated 5 V, 400 mA supply utilizing a device from the LinkSwitch-3 family of ICs, specifically using LNK6404D.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

Figure 1 – Populated Circuit Board Photograph, Top.

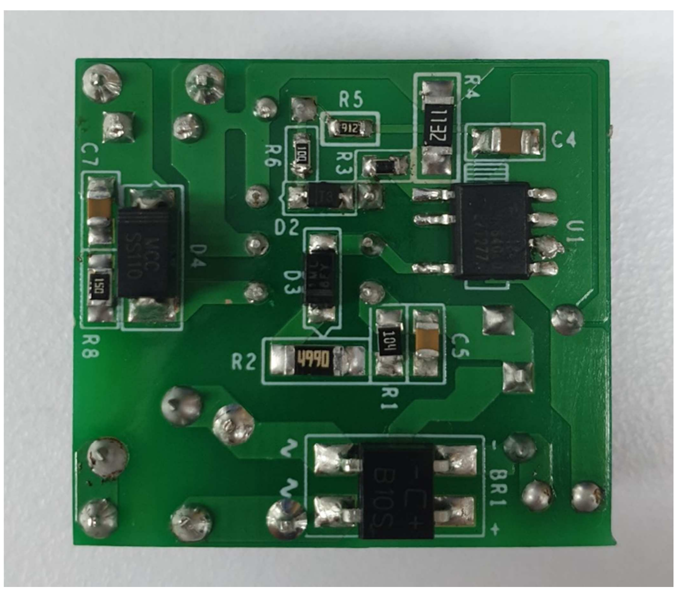

Figure 2 – Populated Circuit Board Photograph, Bottom.

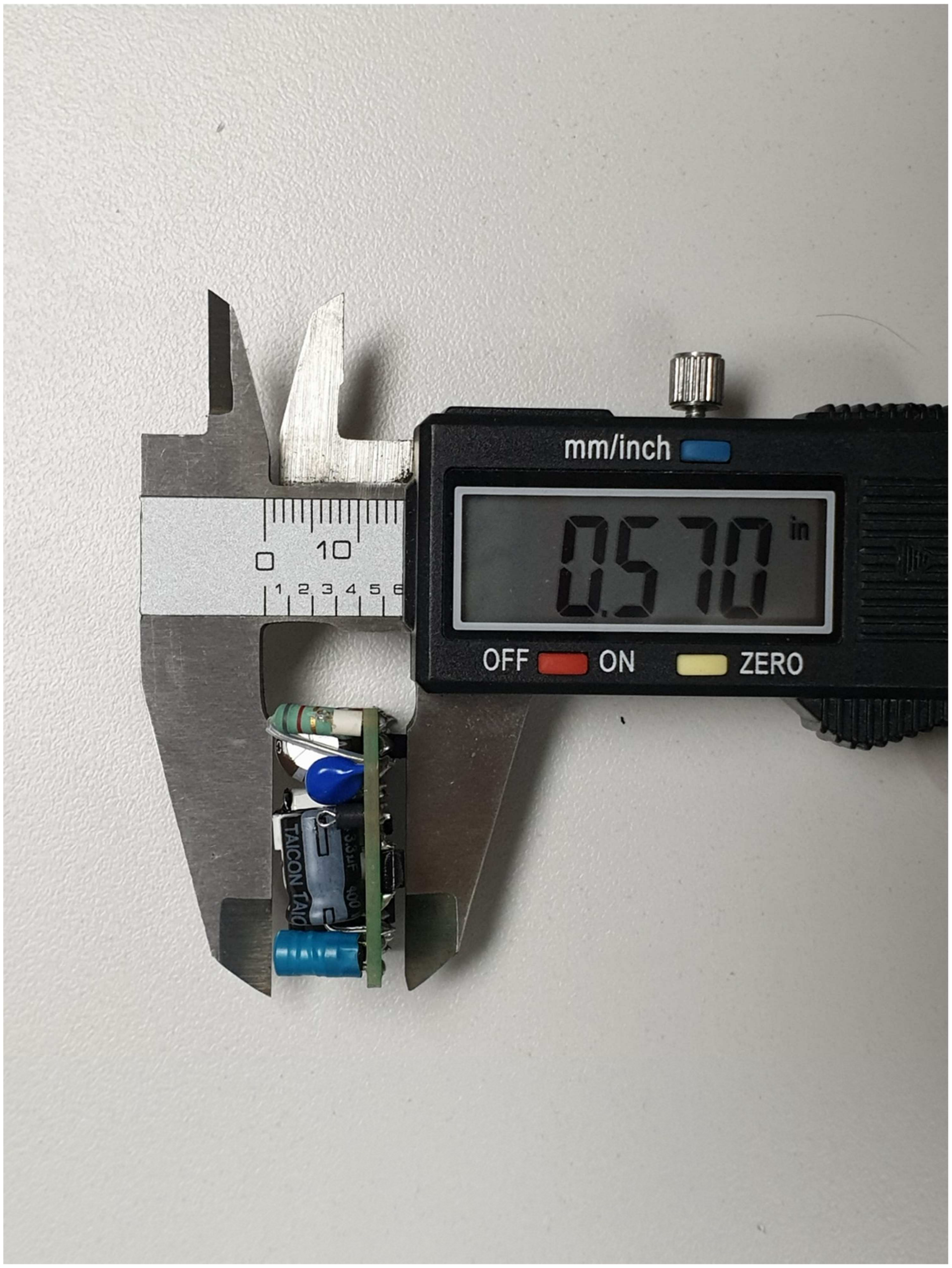

Figure 3 – Populated Circuit Board Photograph, Side.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$\mathbf{V_{IN}}$	85		265	VAC	2 Wire – no P.E.
Frequency	$\mathbf{f_{LINE}}$	47	50/60	63	Hz	
No-load Input Power				50	mW	230 VAC Input.
Output						
Output Voltage	$\mathbf{V_{OUT}}$		5.00		V	±5% PCB Connector Side.
Output Ripple Voltage	$\mathbf{V_{RIPPLE}}$			150	mVpp	Measured at the PCB End.
Output Current	$\mathbf{I_{OUT}}$	0.04		400	mA	
Continuous Output Power	$\mathbf{P_{OUT}}$			2	W	
Efficiency						
Average Efficiency 25%, 50%, 75%, and 100%	$\eta_{AVE[BRD]}$	64			%	DoE Level VI, Basic Voltage.
Full Load Efficiency	η	67			%	@ Nominal Lines and Measured at PCB End.
Environmental						
Conducted EMI		CISPR22B / EN55022B Load floating				Resistive Load, 6 dB Margin.
Differential Line Surge		1			kV	1.2/50 μs surge, IEC 61000-4-5, Series Impedance: Differential Mode: 2 Ω.
Ambient Temperature	$\mathbf{T_{AMB}}$	0		40	ºC	Free Convection, Sea Level in Sealed Enclosure.

3 Schematic Diagram

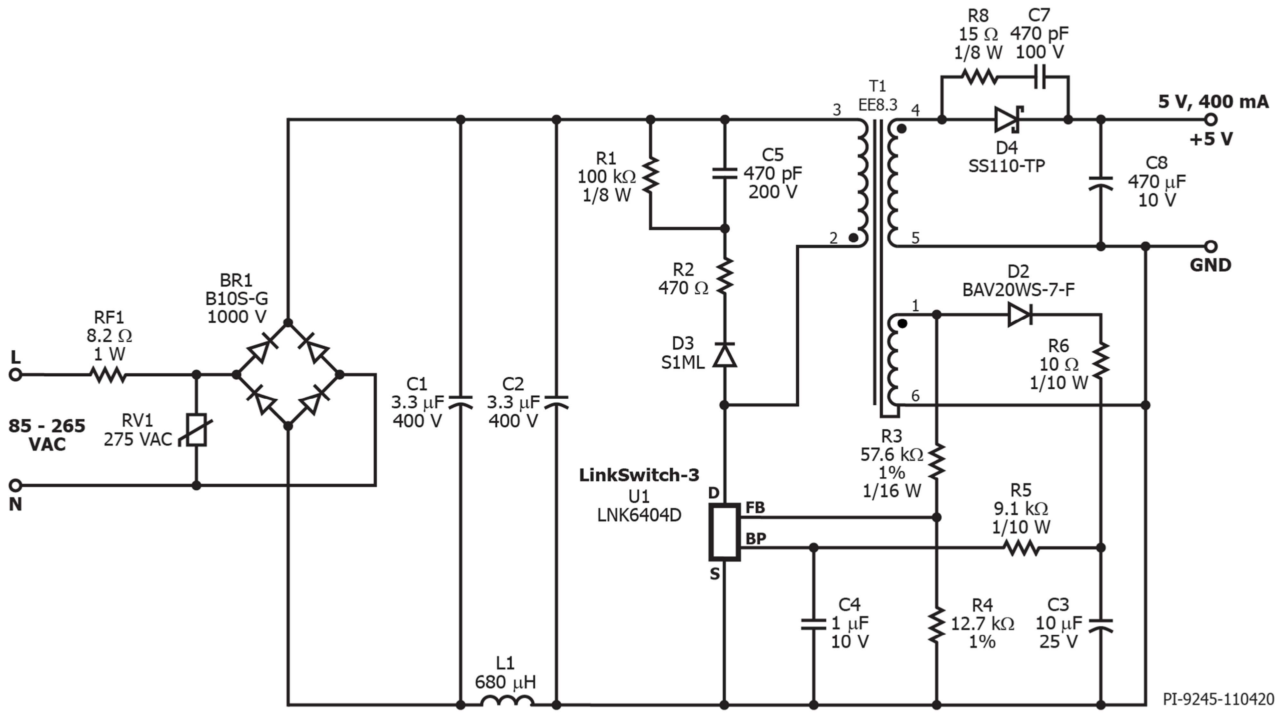

Figure 4 – Schematic.

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4 Circuit Description

4.1 *Input EMI Filtering*

Resistor RF1 is fusible, flameproof, wire-wound type and functions as a fuse and inrush current limiter which provide protection against catastrophic failure of components of the primary-side and limits the inrush current when the power supply is connected to the AC input supply due to low impedance of the input capacitors, C1 and C2, during start-up operation.

Varistor RV1 clamps the AC input voltage across the power supply against surge and voltage transients.

Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input capacitors, C1 and C2.

Capacitors C1 and C2 provide filtering of the rectified AC Input and together with L1 forming a π (pi) filter to attenuate differential mode EMI.

4.2 *LNK6404D Primary*

The LNK6404D device (U1) incorporates the power switching device, oscillator, CV/CC control engine, and start-up and protection function on a single IC. The integrated 725 V power MOSFET allows sufficient voltage margins across universal AC input applications. The device is powered from the BYPASS pin with the decoupling capacitor C4 via the bias circuit D2, R5, R6 and C3 along with the bias/feedback winding of transformer T1. The resistor R6 helps dampen the ringing on the bias winding voltage. The resistor R5 limits the BP pin current.

The rectified and filtered input voltage is applied to one end of the transformer T1 primary winding. The other side of the T1 primary winding is driven by the internal MOSFET of U1. A low cost RCD clamp formed by D3, R1, R2 and C5 limits the peak drain voltage due to the effects of transformer leakage reactance and output trace inductance.

4.3 *Output Rectification and Filtering*

Transformer T1 secondary voltage is rectified by a Schottky barrier-type diode D4 and filtered by the low ESR output capacitor C8.

4.4 *Output Regulation*

The LNK6404D regulates the output using ON/OFF control for CV regulation and frequency control for CC regulation. The output voltage is sensed by a feedback winding on transformer T1. The feedback resistors R3 and R4 were selected using standard 1% tolerance resistor values to center both the nominal output voltage and constant current regulation thresholds.

5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 µm)
PCB thickness is 1.6 mm.

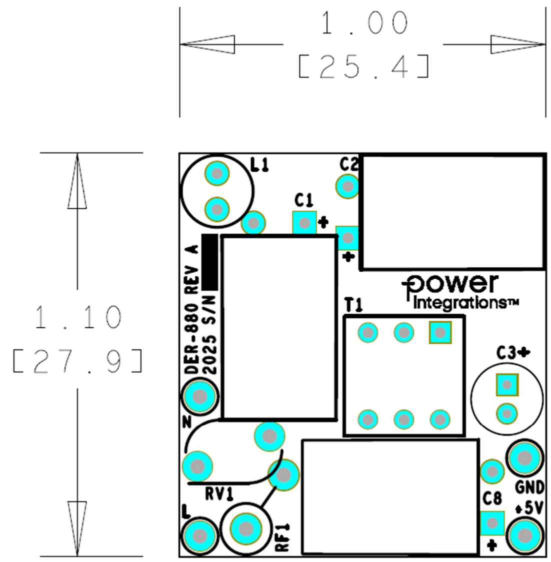

Figure 5 – Printed Circuit Layout, Top.

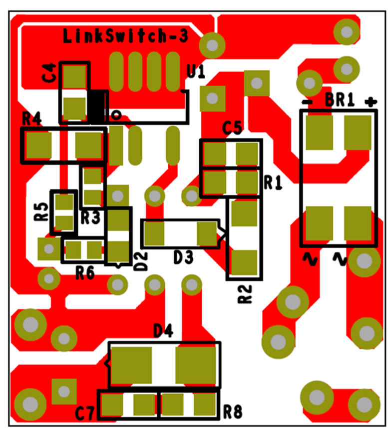

Figure 6 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	1	C1, C2	3.3 µF, 400 V, Electrolytic, (8 x 11.5)	ESMQ401ELL3R3MHB5D	Nippon Chemi-Con
3	1	C3	10 µF, 20%, 25 V, Electrolytic,-55°C ~ 105°C, 1000 Hrs @ 105°C, Gen Purpose, (5 x 6)	UMT1E100MDD1TP	Nichicon
4	1	C4	1 µF ±10% 10 V Ceramic X7R 0805	C0805C105K8RACAUTO	Kemet
5	1	C5	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
6	1	C7	470 pF, 100 V, Ceramic, X7R, 0805	08051C471KAT2A	Kemet
7	1	C8	470 µF, 10 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE100ELL471MHB5D	Nippon Chemi-Con
8	1	D2	200 V, 200 mW, Diode, SOD323	BAV20WS-7-F	ON Semi
9	1	D3	1 kV, 1 A, Standard Recovery, SMA	S1ML	Taiwan Semi
10	1	D4	100 V, 1 A, Schottky, DO-214AC (SMA)	SS110-TP	Micro commercial
11	1	L1	680 µH, 0.25 A, 5.5 x 10.5 mm	SBC1-681-251	Tokin
12	1	R1	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
13	1	R2	RES, 470 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ471V	Panasonic
14	1	R3	RES, 57.6 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF5762V	Panasonic
15	1	R4	RES, 12.7 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1272V	Panasonic
16	1	R5	RES, 9.1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ912V	Panasonic
17	1	R6	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
18	1	R8	RES, 15 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ150V	Panasonic
19	1	RF1	RES, 8.2 Ω, 1 W, 5% , Fusible/Flame Proof Wire Wound	FKN1WSJR-52-8R2	Yageo
20	1	RV1	275 VAC, 8.6 J, 5 mm, RADIAL	S05K275	Epcos
21	1	T1	Bobbin, EE8.3, Horizontal, 6 pins (8.3 mm W x 8.3 mm L x 6.2 mm H)	MCT-EE8.3-10(H3+3P)	Mycoiltech
22	1	U1	LinkSwitch-3, 1%, SO-8-D	LNK6404D	Power Integrations

Miscellaneous Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	N	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
2	2	L, GND	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
3	1	+5V	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
4	10mm	INSULATION1	Tubing 0.032" ID PTFE 100' NAT For RF1	TFT20020	Alpha Wire

7 Transformer Specification

7.1 *Electrical Diagram*

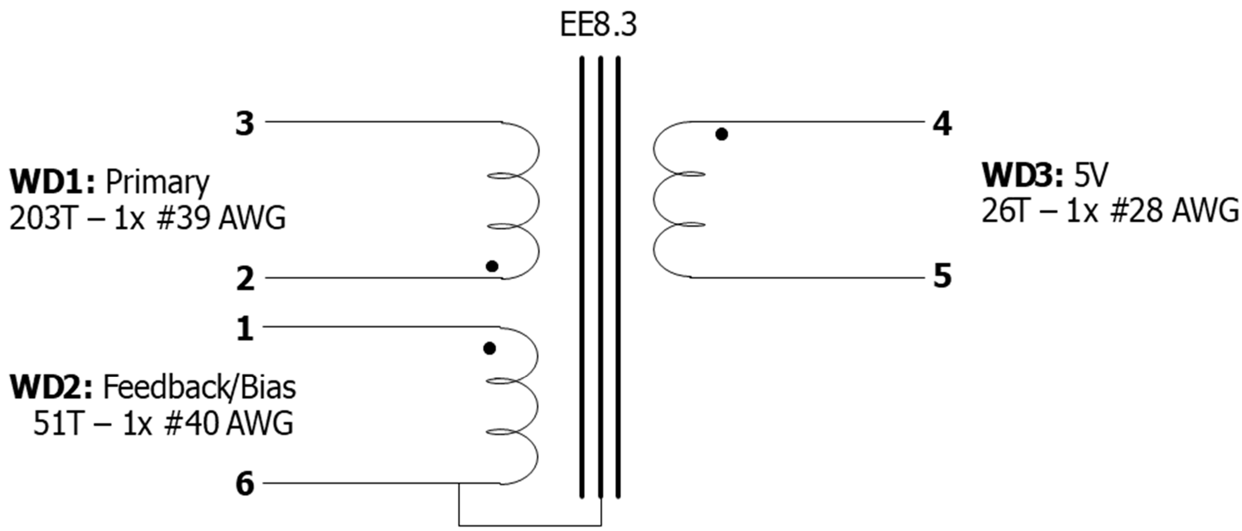

Figure 7 – Transformer Electrical Diagram.

7.2 *Electrical Specification*

Primary Inductance	Pins 2-3, all other windings open, measured at 100 kHz, 1 V_{RMS}.	970 µH ±10%
Primary Leakage Inductance	Pins 2-3, with pins 1-6 and pins 4-5 shorted, measured at 100 kHz, 0.4 V_{RMS}.	110 µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EE8.3, Ferrite Core PC40, gapped for ALG of 101nH/T².
[2]	Bobbin: EE-8.3 Vertical.
[3]	Magnet Wire: #39 AWG, Double Coated.
[4]	Magnet Wire: #40 AWG, Double Coated.
[5]	Magnet Wire: #28 AWG, Double Coated.
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 5 mm Wide.
[7]	Bus Wire: #34 AWG, Belden Electronics Div; or Equivalent.
[8]	Varnish: Dolph BC-359.
[9]	Tape: 3M 1298 Polyester Film 1 mil Thick, 3.5 mm Wide.

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7.4 *Transformer Build Diagram*

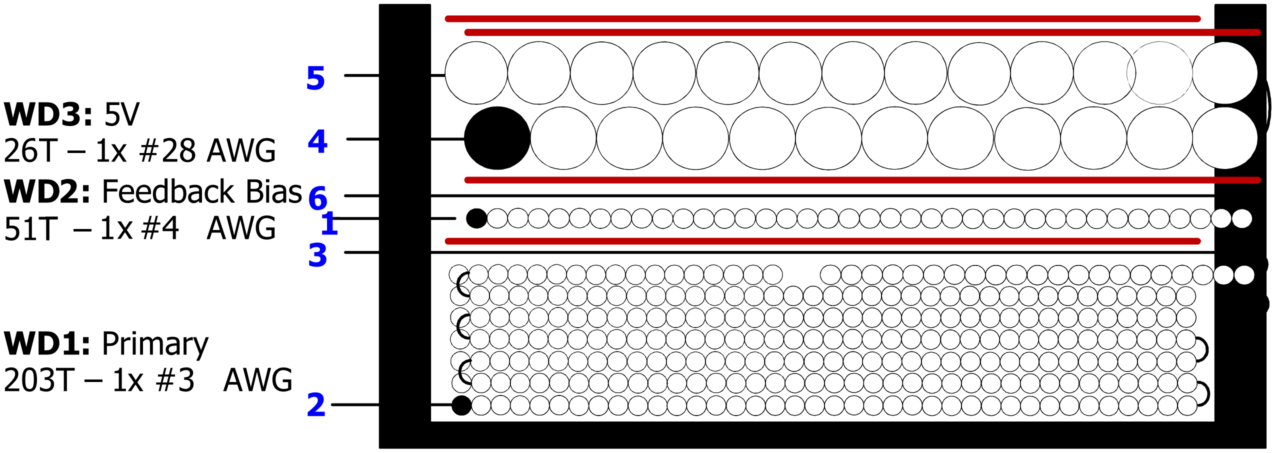
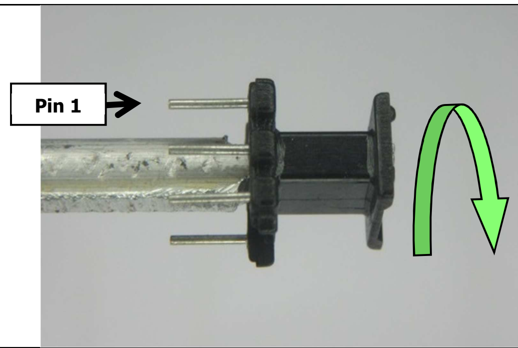
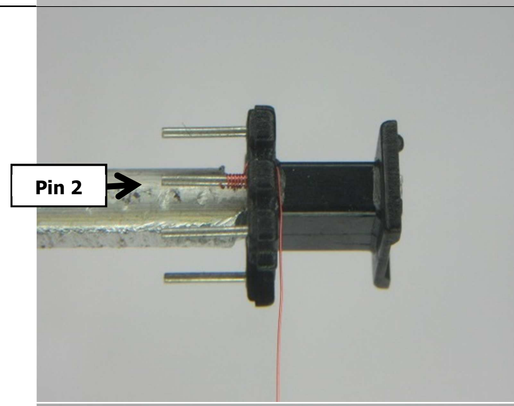
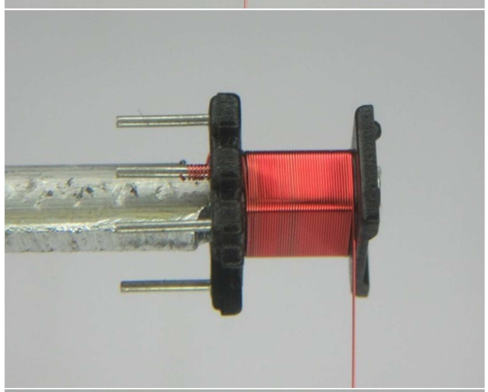
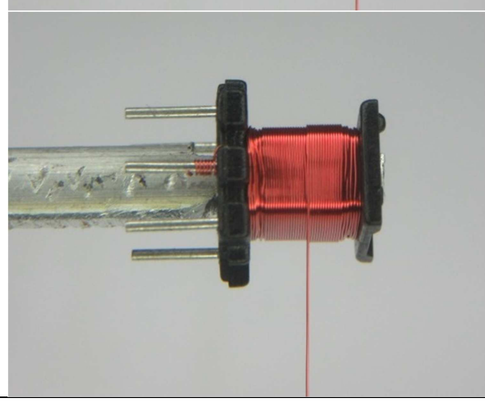


Figure 8 – Transformer Build Diagram.

7.5 *Transformer Instructions*

Winding Preparation	For the purpose of these instructions, bobbin is oriented on winder such that primary side (3-pin) is on the left side with Pin 1 at the upper side. Winding is in clockwise direction.
WD1 Primary	Start at pin 2, wind 203 turns (x1 filar) of wire Item [3] with tight tension. At the last turn, bring the wire back to the left and terminate at pin 3.
Insulation	1 layer of tape Item [6] for insulation.
WD2 Feedback/Bias	Start at pin 1, wind 51 turns (x1 filar) of wire Item [4]. Terminate winding at pin 6.
Insulation	1 layer of tape Item [6] for insulation.
WD3 Secondary	Start at pin 4, wind 26 turns (x1 filar) of wire Item [5]. Terminate winding at pin 5.
Insulation	2 layers of tape Item [6] to secure the windings.
Finish	Gap core halves for 970 μH inductance. Use 1" of bus wire Item [7] solder to pin 6. Wrap core halves and bus wire above which lean along the core with tape Item [9]. Coat with Varnish Item [8].

7.6 ***Winding Illustrations***

Winding Preparation		For the purpose of these instructions, bobbin is oriented on winder such that primary side (3-pin) is on the left side with Pin 1 at the upper side. Winding is in clockwise direction.
WD1 Primary		Start at pin 2, wind 203 turns (x1 filar) of wire Item [3] with tight tension. At the last turn, bring the wire back to the left and terminate at pin 3.

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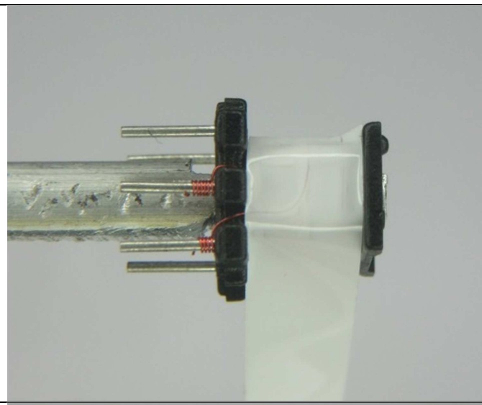
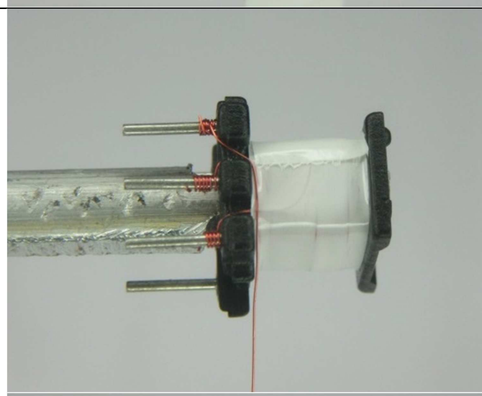
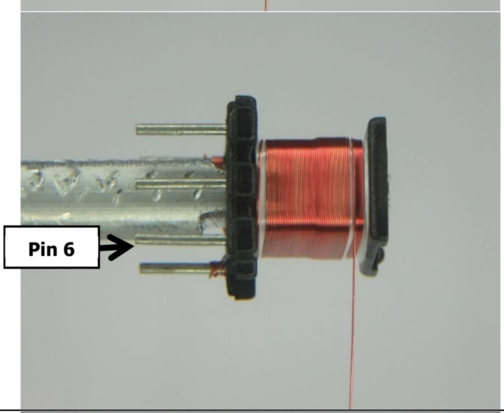
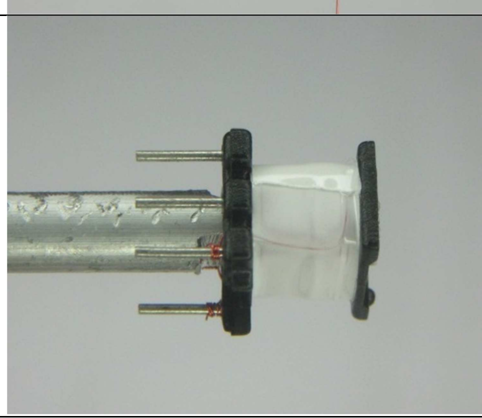
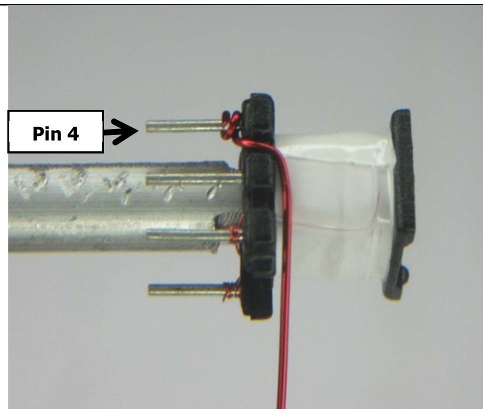
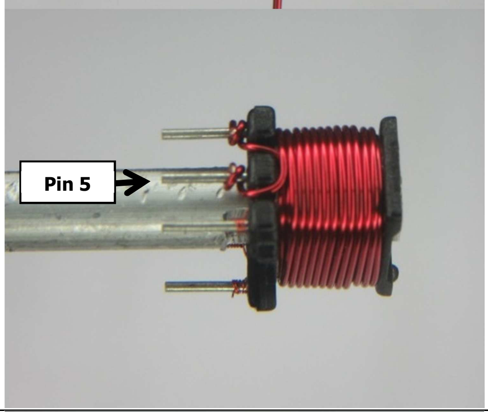
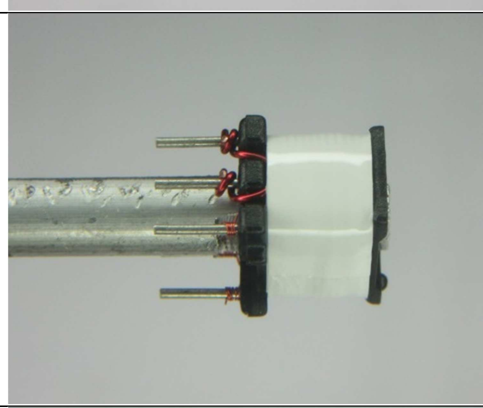
Insulation		1 layer of tape Item [6] for insulation.
WD2 Feedback/Bias	 	Start at pin 1, wind 51 turns (x1 filar) of wire Item [4]. Terminate winding at pin 6.
Insulation		1 layer of tape Item [6] for insulation.

WD5 Secondary		Start at pin 4, wind 26 turns (x1 filar) of wire Item [5]. Terminate winding at pin 5.
Insulation		2 layers of tape Item [6] to secure the windings.
Finish		Gap core halves for 970 µH inductance.

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Finish		Use 1” of bus wire Item [7] solder to pin 6.
		Wrap core halves and bus wire above which lean along the core with tape Item [9].
		Coat with varnish Item [8].

8 Design Spreadsheet

1	ACDC_LinkSwitch-3_080516; Rev.2.3; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNIT	LinkSwitch-3 Discontinuous Flyback Transformer Design Spreadsheet
2	**ENTER APPLICATION VARIABLES**					
3	VACMIN	85		85	V	Minimum AC Input Voltage
4	VACMAX	265		265	V	Maximum AC Input Voltage
5	fL			50	Hz	AC Mains Frequency
6	Application Type	Adapter		Adapter		Choose application type
7	VO	5.00		5.00	V	Output Voltage (at continuous power)
8	IO	0.40		0.40	A	Minimum required output current
9	Power	.		2.00	W	Continuous Output Power
10	n	0.63		0.63		Efficiency Estimate at output terminals.
11	Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
12	tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
13	CIN	6.60		6.60	uF	Input Capacitance
15	**ENTER LinkSwitch-3 VARIABLES**					
16	Chosen Device	LNK64x4D		LNK64x4D		Chosen LinkSwitch-3 device and package. E.g. - LNK64x4D or LNK64x8K
17	Cable drop compensation option	1%		1%		Select level of cable drop compensation
18	Complete Part Number			LNK6404D		Full Part Number
19	ILIMITMIN			0.24	A	Minimum Current Limit
20	ILIMITTYP			0.26	A	Typical Current Limit
21	ILIMITMAX			0.28	A	Maximum Current Limit
22	FS			80.00	kHz	Typical Device Switching Frequency at maximum power
23	VOR			42.94	V	Reflected Output Voltage (VOR < 135 V Recommended)
24	VDS			10.00	V	LinkSwitch-3 on-state Drain to Source Voltage
25	VD			0.50	V	Output Winding Diode Forward Voltage Drop
26	KP			1.53		KP assuming minimum LP, VMIN, and Maximum Switching Frequency, but not including frequency jitter.
29	**FEEDBACK WINDING PARAMETERS**					
30	NFB	51.00		51.00		Feedback winding turns
31	VFLY			10.79	V	Flyback Voltage - Voltage on Feedback Winding during switch off time
32	VFOR			22.07	V	Forward voltage - Voltage on Feedback Winding during switch on time
34	**BIAS WINDING PARAMETERS**					
35	BIAS	Ext. Bias		Ext. Bias		Select between self bias or external bias to supply the IC. Note that this will affect ILIMIT
36	VB			N/A	V	Feedback Winding Voltage (VFLY) is greater than 10 V. The feedback winding itself can be used to provide external bias to the LinkSwitch. Additional Bias winding is not required.
37	NB			N/A		Bias Winding number of turns
38	REXT			9.10	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
39	**DESIGN PARAMETERS**					
40	DCON	5.00		5.00	us	Desired output diode conduction time
41	DCON_FINAL			4.98	us	Final output conduction diode, assuming integer values for NP and NS, and VMIN
42	TON			2.44	us	LinkSwitch-3 On-time (calculated at LPMIN, VMIN and ILIMITMIN)
43	RUPPER			46.25	k-ohm	Upper resistor in Feedback resistor divider

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44	RLOWER			10.14	k-ohm	Lower resistor in resistor divider
46	**ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES**					
47	**Core Type**					
48	Core	EE8		EE8		Enter Transformer Core.
49	Custom_Core					Enter Core name if selection on drop down menu is "Custom"
50	Bobbin			BE-8-116-CP		Bobbin part number
51	AE			7.00	mm^2	Core Effective Cross Sectional Area
52	LE			19.20	mm	Core Effective Path Length
53	AL			610.00	nH/turn^2	Ungapped Core Effective Inductance
54	BW			4.78	mm	Bobbin Physical Winding Width
55	M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
56	L	3.00		3.00		Number of Primary Layers
57	NS			26.00	turns	Number of Secondary Turns. To adjust Secondary number of turns change DCON
59	**DC INPUT VOLTAGE PARAMETERS**					
60	VMIN			87.84	V	Minimum DC bus voltage
61	VMAX			374.77	V	Maximum DC bus voltage
63	**CURRENT WAVEFORM SHAPE PARAMETERS**					
64	DMAX			0.24		Maximum duty cycle measured at VMIN
65	IAVG			0.04	A	Input Average current, at VMIN
66	IP			0.24	A	Peak primary current
67	IR			0.24	A	Primary ripple current
68	IRMS			0.08	A	Primary RMS current
70	**TRANSFORMER PRIMARY DESIGN PARAMETERS**					
71	LPMIN			878.63	uH	Minimum Primary Inductance
72	LPTYP			976.25	uH	Typical Primary inductance
73	LP_TOLERANCE	10.00		10.00	%	Tolerance in primary inductance
74	NP			203.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
75	ALG			23.69	nH/turn^2	Gapped Core Effective Inductance
76	BM_TARGET	1800.00		1800.00	Gauss	Target Flux Density
77	BM			1803.42	Gauss	Maximum Operating Flux Density (calculated with LPTYP, ILIMITTYP), BM < 2600 is recommended
78	BP			2126.59	Gauss	Peak Operating Flux Density (calculated with LPMAX, ILIMITMAX), BP < 3100 is recommended
79	BAC			901.71	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
80	ur			133.14		Relative Permeability of Ungapped Core
81	LG			0.40	mm	Gap Length (LG > 0.1 mm)
82	BWE			14.34	mm	Effective Bobbin Width
83	OD	0.14		0.14	mm	Maximum Primary Wire Diameter including insulation
84	INS			0.03	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
85	DIA			0.11	mm	Bare conductor diameter
86	AWG			38	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
87	CM			16.00	Cmils	Bare conductor effective area in circular mils
88	CMA			200.26	Cmils/A	Primary Winding Current Capacity (200 < CMA < 500)
90	**TRANSFORMER SECONDARY DESIGN PARAMETERS**					
92	ISP			1.90	A	Peak Secondary Current assuming Ilimitmin
93	ISRMS			0.89	A	Secondary RMS Current assuming Ilimitmax and Dmax
94	IRIPPLE			0.80	A	Output Capacitor RMS Ripple Current
95	CMS			178.43	Cmils	Secondary Bare Conductor minimum circular mils
96	AWGS			27.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)

98	**VOLTAGE STRESS PARAMETERS**					
99	VDRAIN			484.95	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)
100	PIVS			72.45	V	Output Rectifier Maximum Peak Inverse Voltage
102	**FINE TUNING**					
103	RUPPER_ACTUAL	56.20		56.20	k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
104	RLOWER_ACTUAL	12.70		12.70	k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
105	Actual (Measued) Output Voltage (VDC)	4.86		4.86	V	Measured Output voltage from first prototype
106	Actual (Measured) Output Current (ADC)	0.40		0.40	Amps	Measured Output current from first prototype
107	RUPPER_FINE			57.82	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 57.6 k-ohms
108	RLOWER_FINE			12.66	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 12.7 k-ohms

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9 Performance Data

All measurements performed with room ambient temperature.

9.1 *Full Load Efficiency vs. Line*

Soak for 20 minutes and 5 minutes for each line/step.
Measured at 0.4 A Full Load

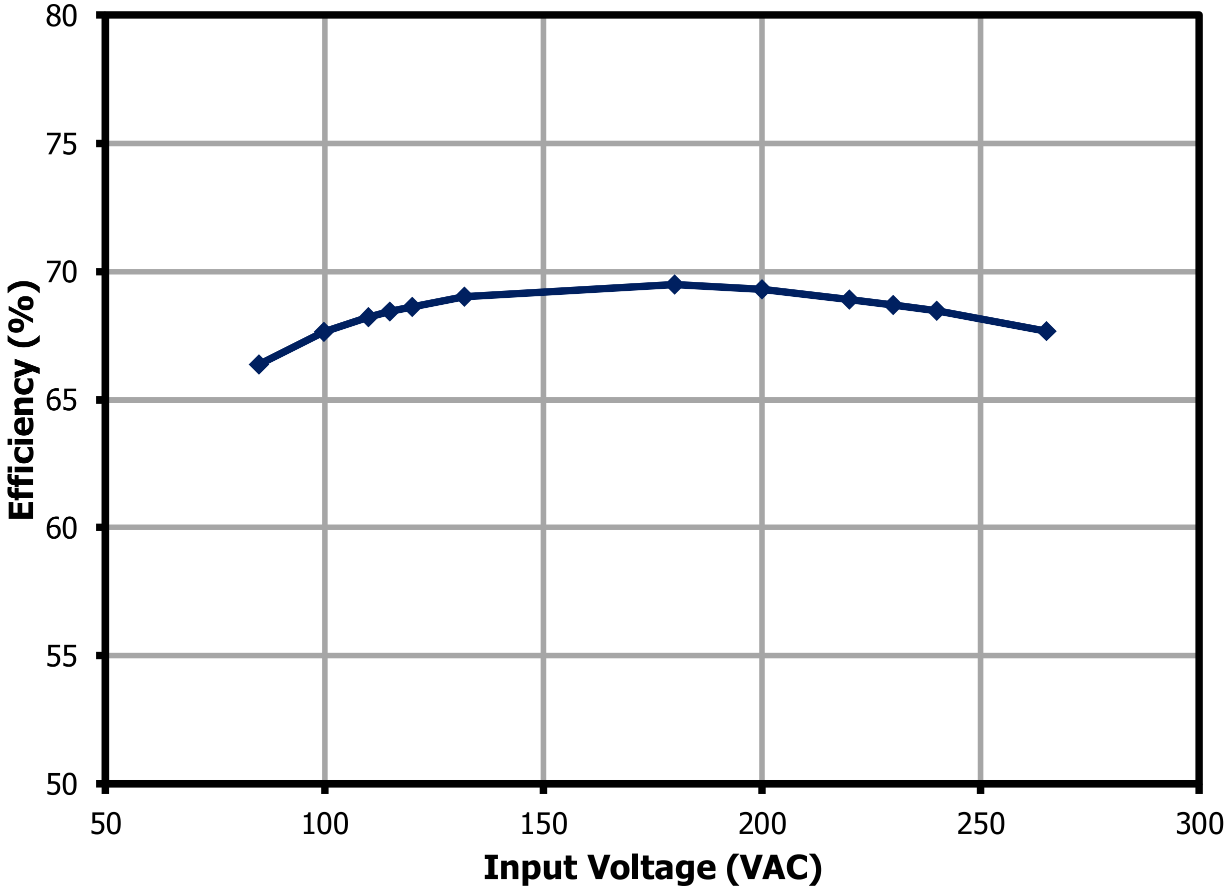

Figure 9 – Efficiency vs. Line.

9.2 ***Efficiency vs. Load***

Soak for 5 minutes and 30 seconds for each load step.

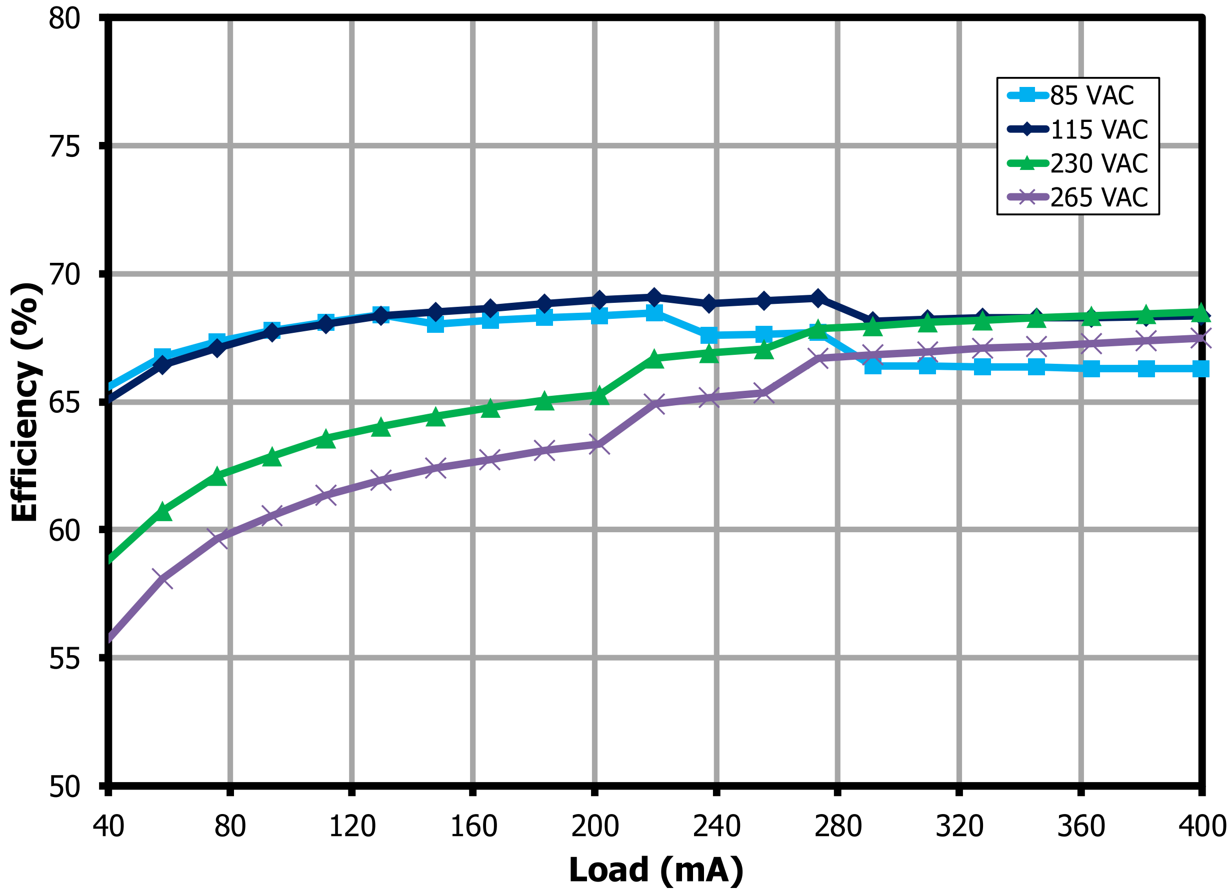

Figure 10 – Efficiency vs. Load (Measured Across PCB Connector).

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9.3 *Average Efficiency, 115 VAC (PCB End)*

Load Settings	Input Measurement			5 V / 400 mA Measurement Variable			
% Load	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency (%)
100	115.00	62.07	2.94	4.97	400.59	1.99	67.86
75	115.00	52.15	2.19	4.99	300.59	1.50	68.44
50	115.00	41.59	1.46	4.94	200.64	0.99	68.09
25	115.01	30.06	0.75	4.96	100.80	0.50	66.92
AVERAGE							67.83

9.4 *Average Efficiency, 230 VAC (PCB End)*

Load Settings	Input Measurement			5 V / 400 mA Measurement Variable			
% Load	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency (%)
100	229.93	36.32	2.93	4.99	400.57	2.00	68.17
75	229.94	30.09	2.22	4.99	300.57	1.50	67.60
50	229.94	23.57	1.52	4.92	200.61	0.99	65.06
25	229.94	16.11	0.79	4.90	100.81	0.49	62.76
AVERAGE							65.90

10 No-Load Input Power

Soak for 15 minutes and 3 minutes integration time for each line/step.

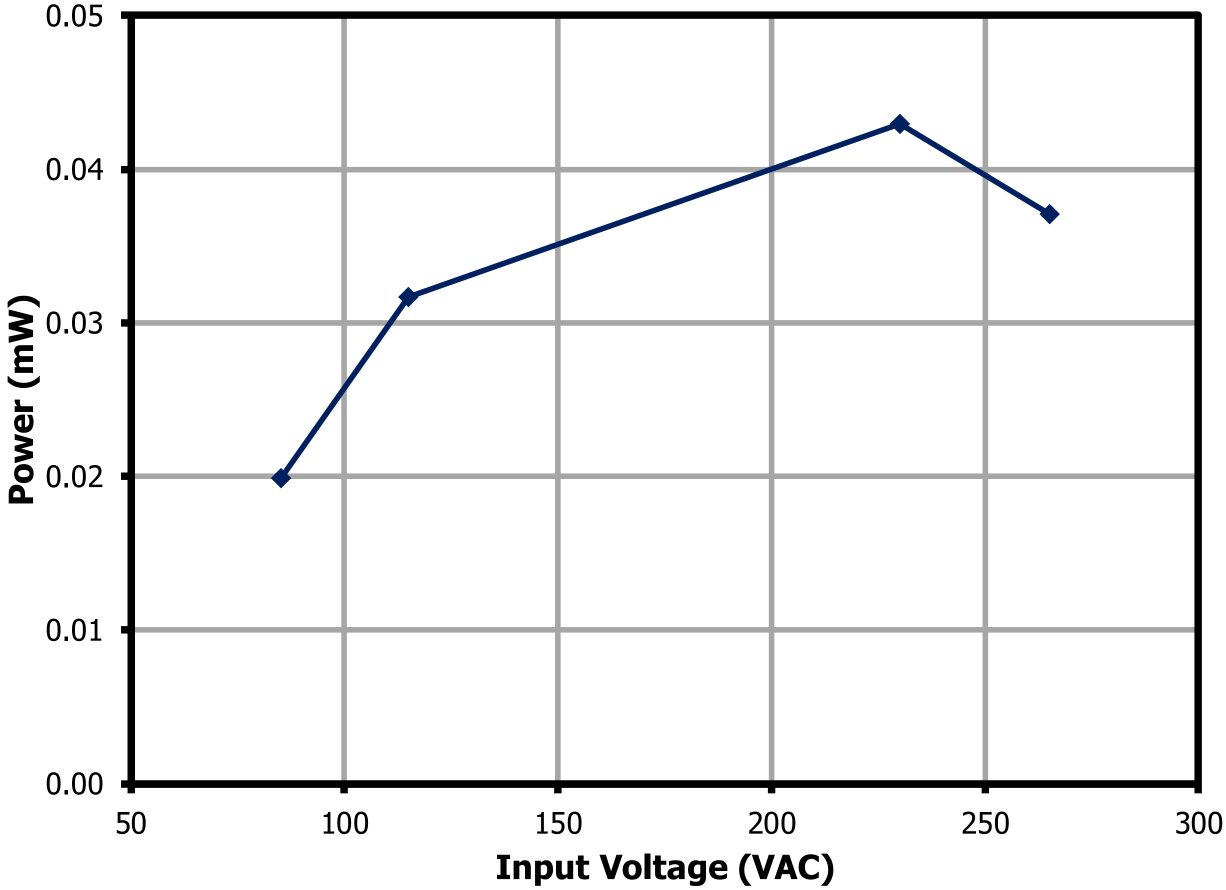

Figure 11 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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11 Line Regulation

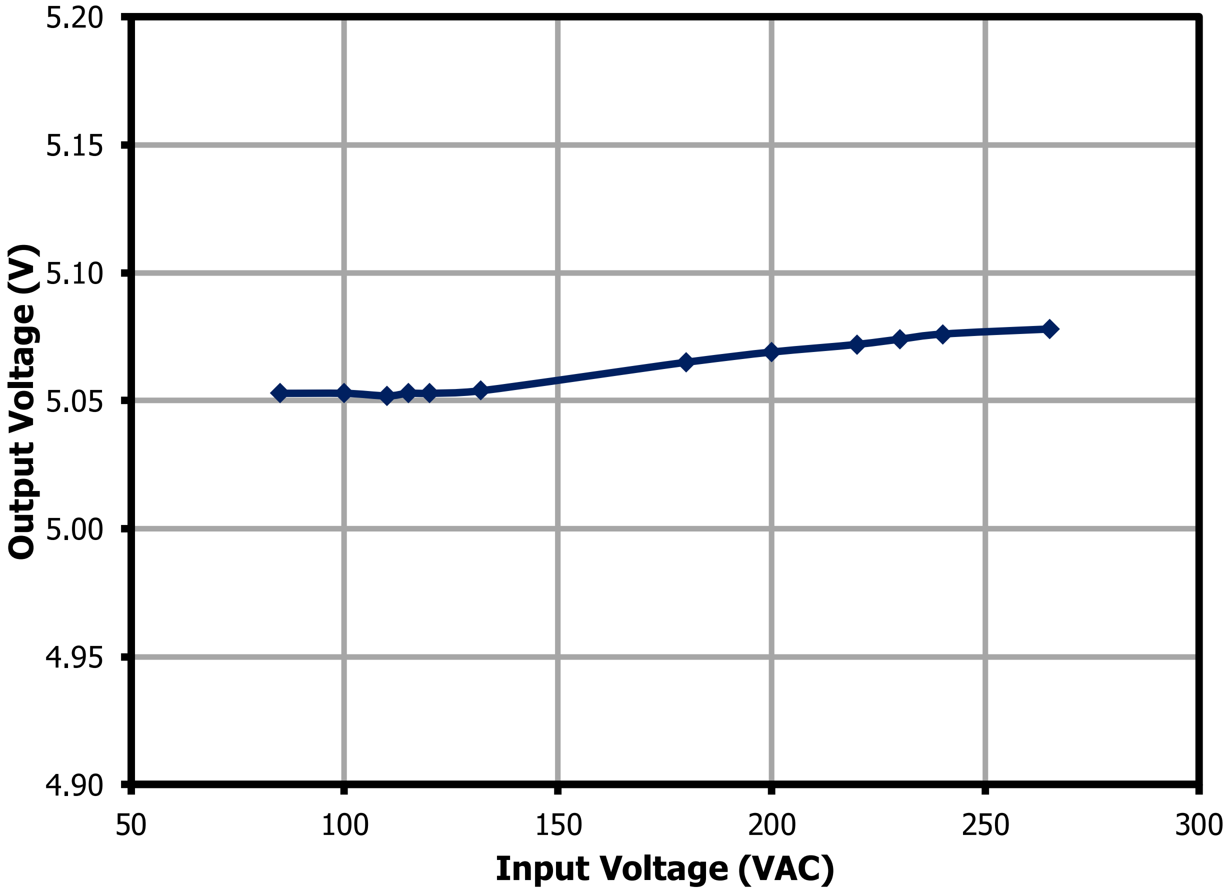

Figure 12 – Full Load Line Regulation.

12 Load Regulation

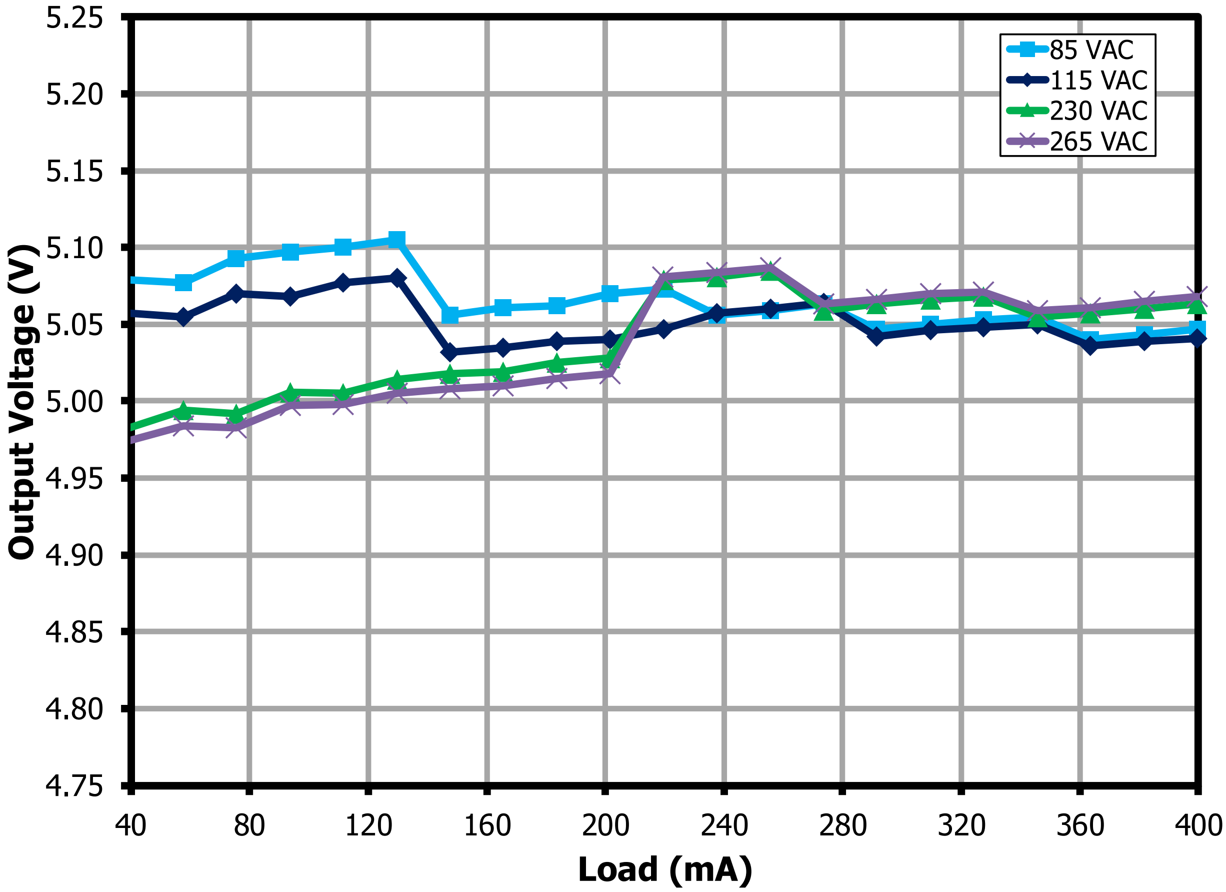

Figure 13 – Load Regulation (Across PCB Connector).

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13 CV/CC Curve

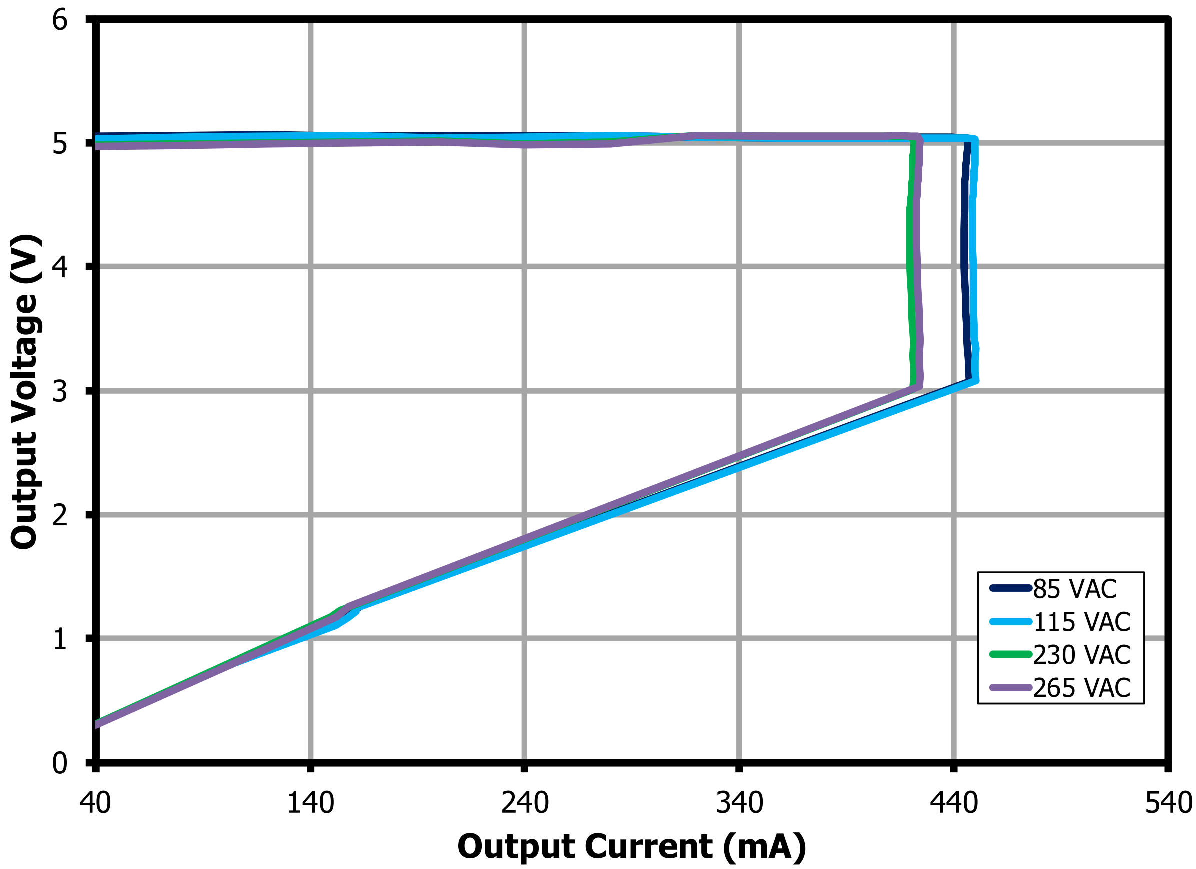

Figure 14 – CV/CC Curve (Measured Across PCB Connector).

14 Thermal Performance

14.1 *Thermal Scan at Room Temperature*

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Temperature was measured using a thermal camera. Soak time at full load is 2 hours.

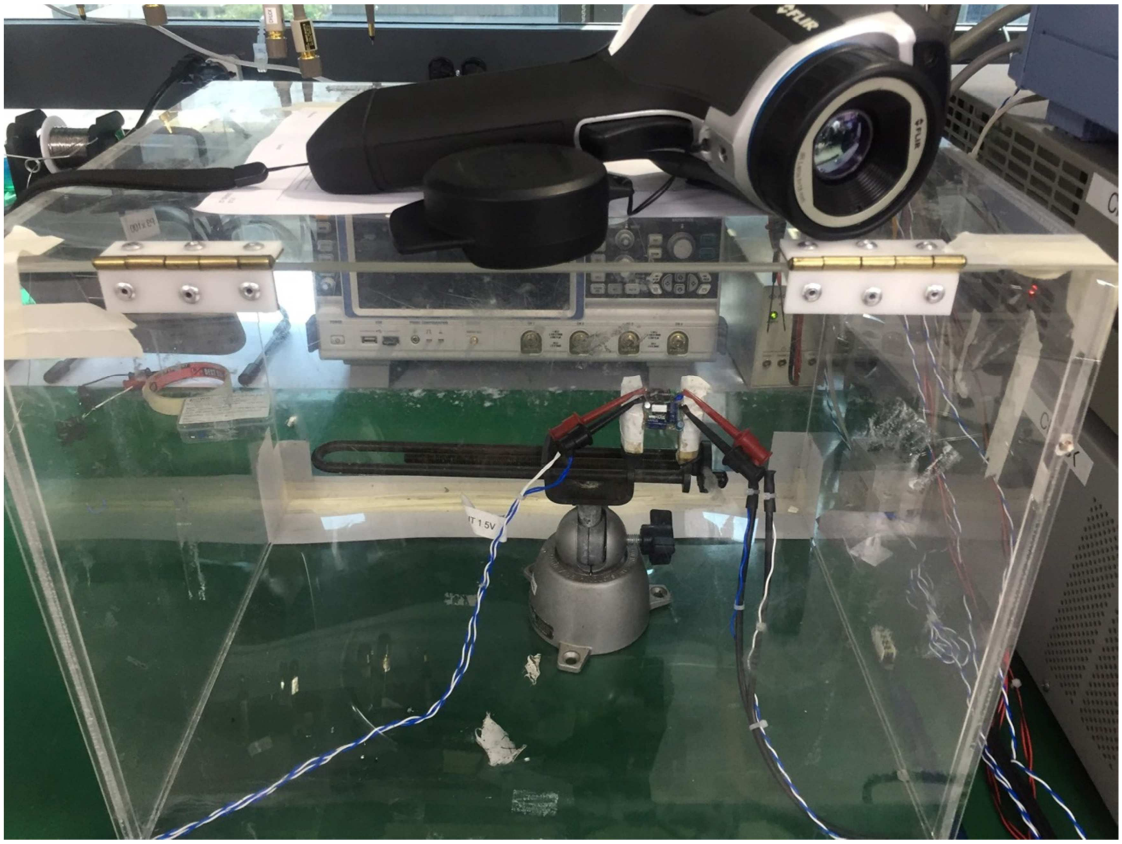

Figure 15 – Test Set-up.

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14.1.1 85 VAC

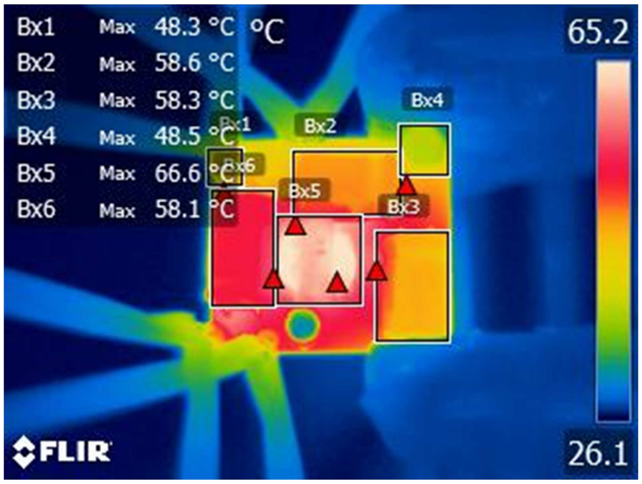

Figure 16 – 85 VAC, 0.4 A Load. Top Side. Ambient = 26.1 ºC.

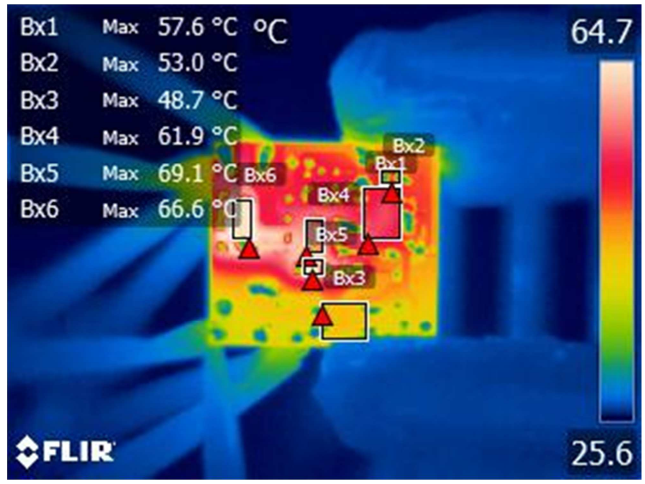

Figure 17 – 85 VAC, 0.4 A Load. Bottom Side. Ambient = 25.6 ºC.

TOP		BOTTOM	
Component	**Temperature (°C)**	**Component**	**Temperature (°C)**
Fusible Resistor (RF1)	48.3	LNK6404D (U1)	57.6
Input Capacitor (C1)	58.6	BP Capacitor (C4)	53.0
Input Capacitor (C2)	58.3	Bridge Rectifier (BR1)	48.7
Input Choke (L1)	48.5	Primary Clamp Diode (D3)	61.9
Transformer (T1)	66.6	Primary Clamp Resistor (R2)	69.1
Output Capacitor (C8)	58.1	Output Diode (D4)	66.6

14.1.2 265 VAC

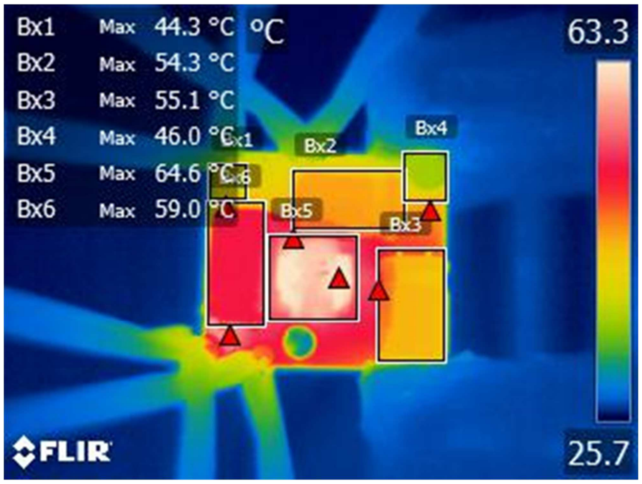

Figure 18 – 265 VAC, 0.4 A Load. Top Side.
Ambient = 25.7 ºC.

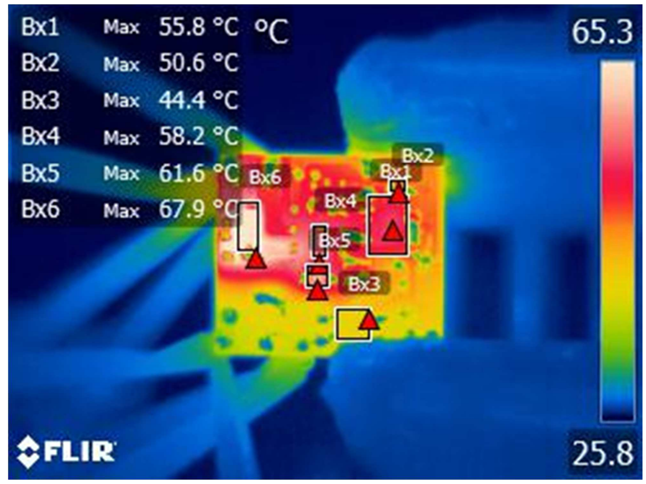

Figure 19 – 265 VAC, 0.4 A Load. Bottom Side.
Ambient = 25.8 ºC.

TOP		**BOTTOM**	
Component	**Temperature (°C)**	**Component**	**Temperature (°C)**
Fusible Resistor (RF1)	44.3	LNK6404D (U1)	55.8
Input Capacitor (C1)	54.3	BP Capacitor (C4)	50.6
Input Capacitor (C2)	55.1	Bridge Rectifier (BR1)	44.4
Input Choke (L1)	46.0	Primary Clamp Diode (D3)	58.2
Transformer (T1)	64.6	Primary Clamp Resistor (R2)	61.6
Output Capacitor (C8)	59.0	Output Diode (D4)	67.9

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15 Test Waveforms

15.1 *Load Transient Response*

15.1.1 10% - 100% Load Condition 1 kHz 50% duty 0.8 A/μsec.

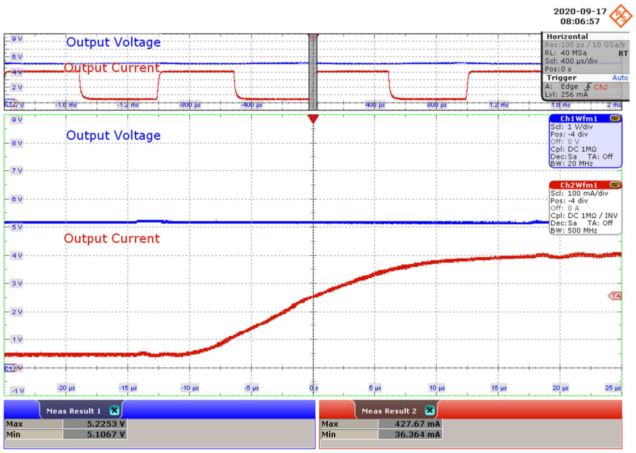

Figure 20 – 85 VAC 60 Hz, 10% - 100% Load.
CH1: V_{OUT}, 1 V / div., 400 μs / div.
CH2: I_{LOAD}, 100 mA / div., 400 μs / div.
Zoom: 5 μs / div.
V_{MAX}: 5.23 V, V_{MIN}: 5.11 V.

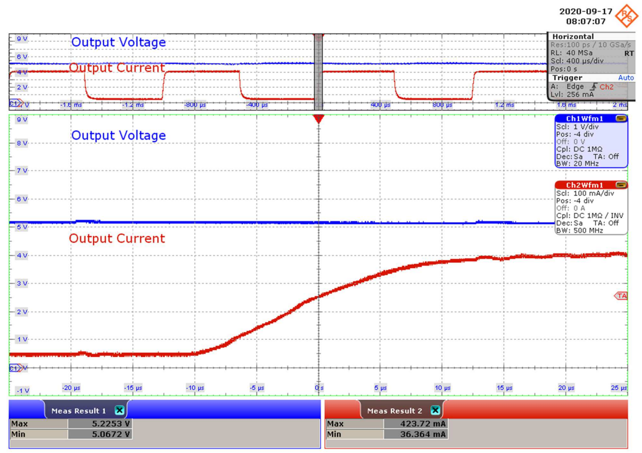

Figure 21 – 115 VAC 60 Hz, 10% - 100% Load.
CH1: V_{OUT}, 1 V / div., 400 μs / div.
CH2: I_{LOAD}, 100 mA / div., 400 μs / div.
Zoom: 5 μs / div.
V_{MAX}: 5.23 V, V_{MIN}: 5.07 V.

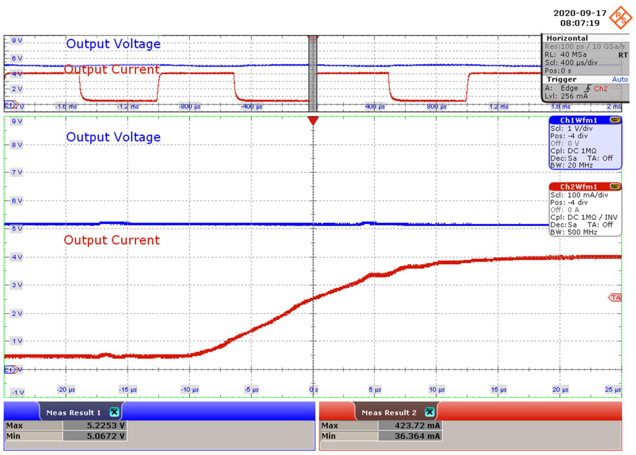

Figure 22 – 230 VAC 50 Hz, 10% - 100% Load.
CH1: V_{OUT}, 1 V / div., 400 μs / div.
CH2: I_{LOAD}, 100 mA / div., 400 μs / div.
Zoom: 5 μs / div.
V_{MAX}: 5.23 V, V_{MIN}: 5.07 V.

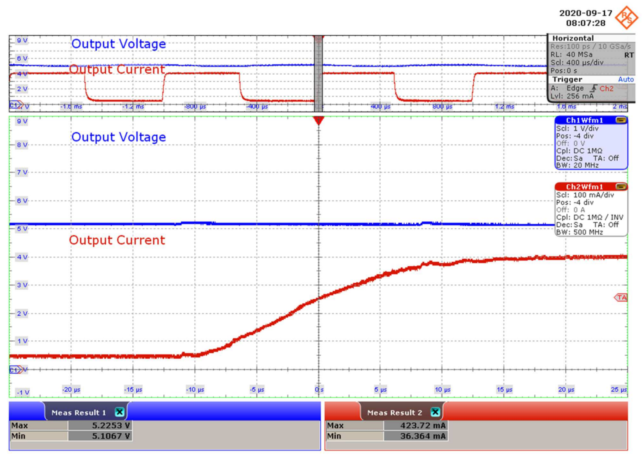

Figure 23 – 265 VAC 50 Hz, 10% - 100% Load.
CH1: V_{OUT}, 1 V / div., 400 μs / div.
CH2: I_{LOAD}, 100 mA / div., 400 μs / div.
Zoom: 5 μs / div.
V_{MAX}: 5.23 V, V_{MIN}: 5.11 V.

15.2 ***Output Voltage at Start-up***

15.2.1 CC mode

15.2.1.1 100% Load

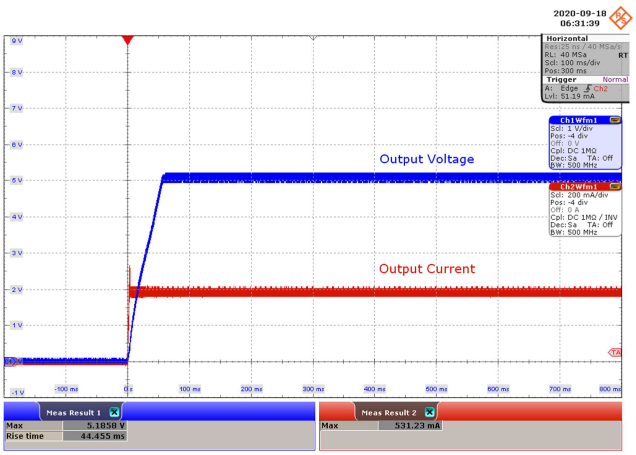

Figure 24 – 85 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

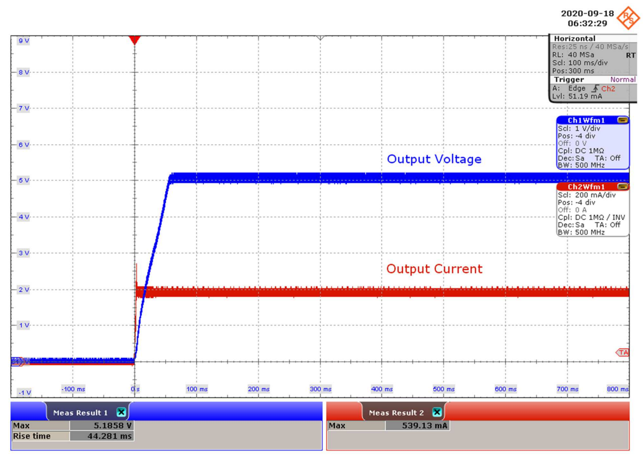

Figure 25 – 115 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

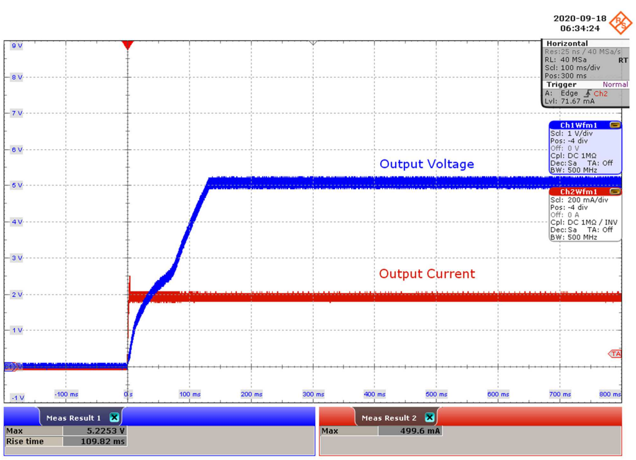

Figure 26 – 230 VAC 50 Hz, Full Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

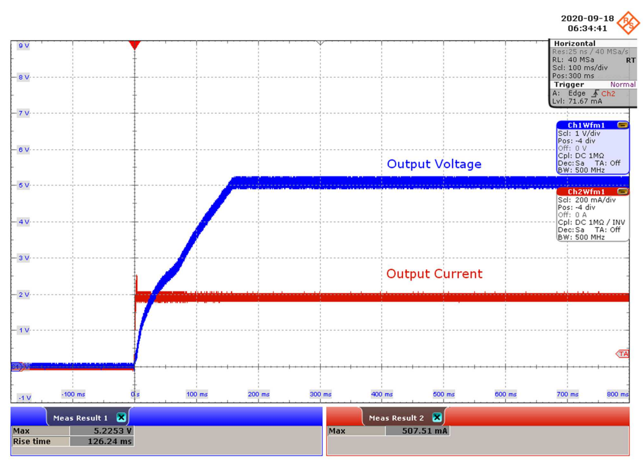

Figure 27 – 265 VAC 50 Hz, Full Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

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15.2.1.2 10% Load

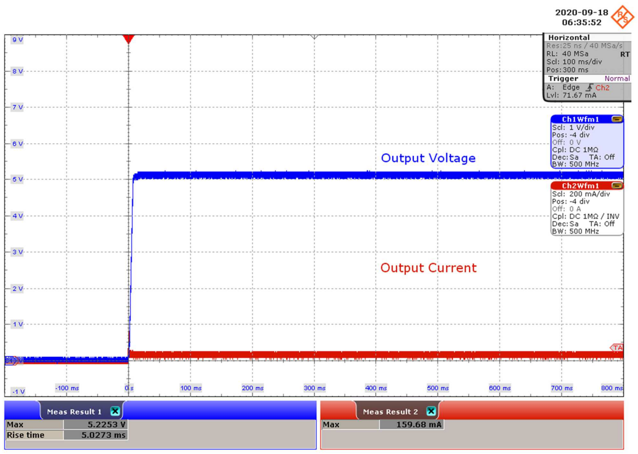

Figure 28 – 85 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

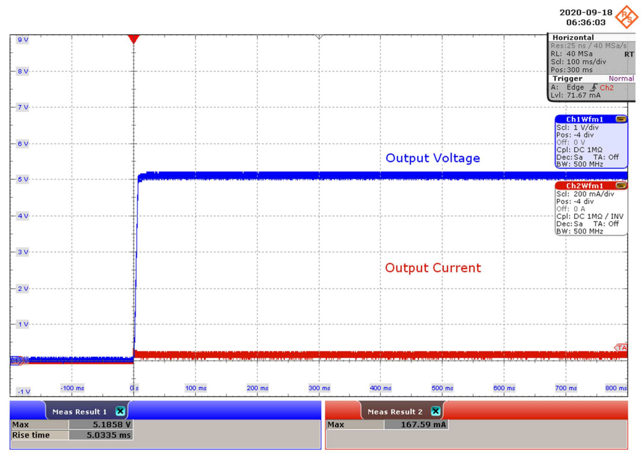

Figure 29 – 115 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

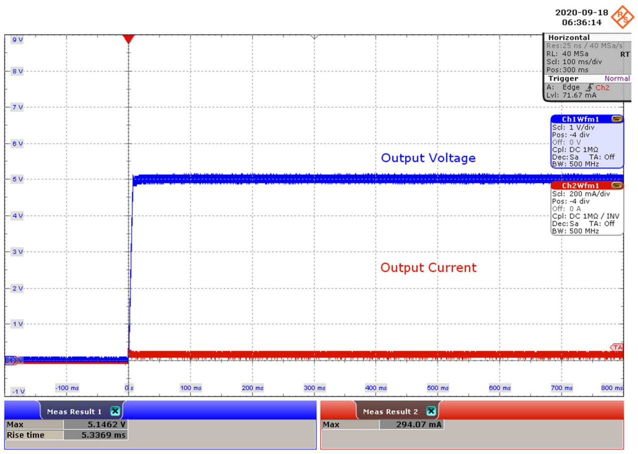

Figure 30 – 230 VAC 50 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

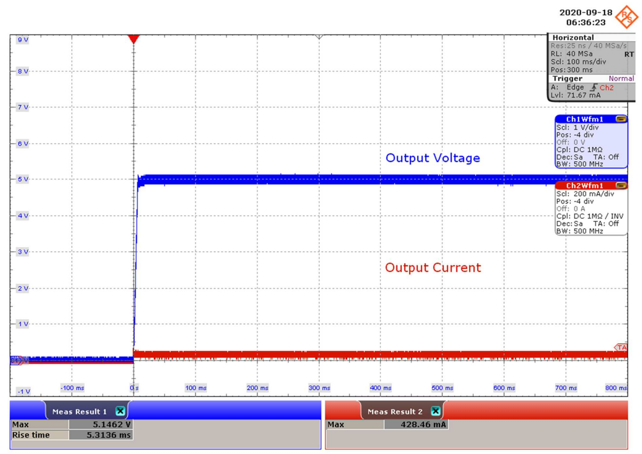

Figure 31 – 265 VAC 50 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

15.2.1 CR mode

15.2.1.1 100% Load

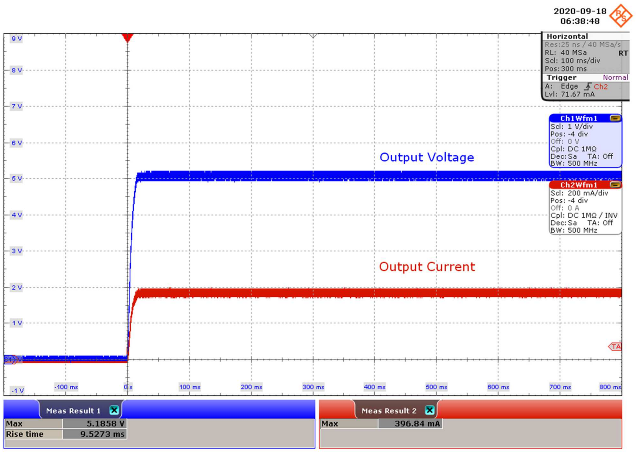

Figure 32 – 85 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

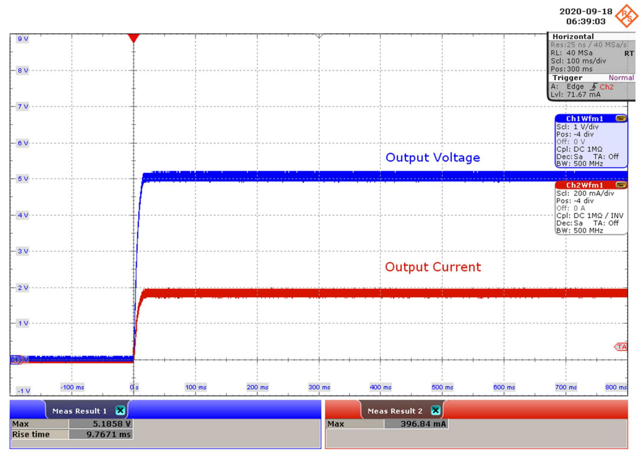

Figure 33 – 115 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

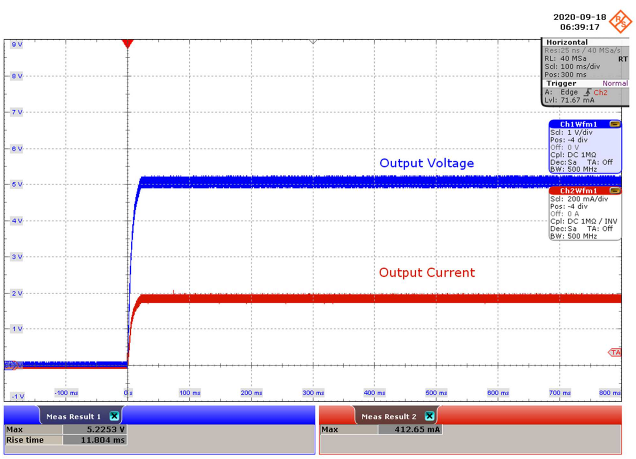

Figure 34 – 230 VAC 50 Hz, Full Load Start-up.
Upper: V_{OUT},1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

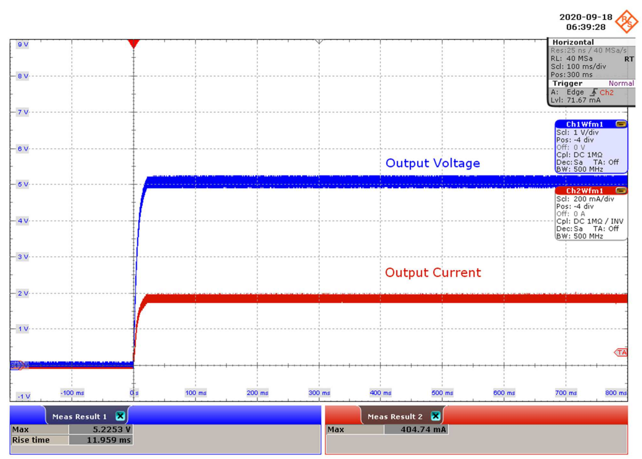

Figure 35 – 265 VAC 50 Hz, Full Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

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15.2.1.2 10% Load

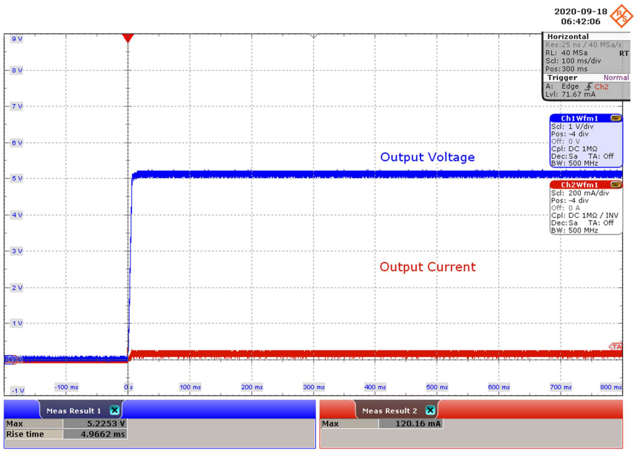

Figure 36 – 85 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

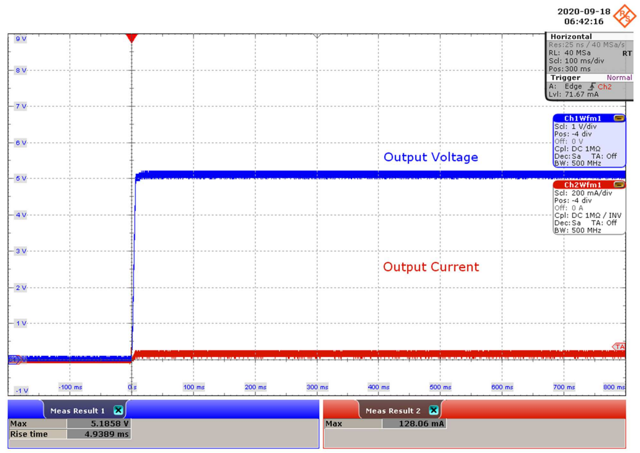

Figure 37 – 115 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

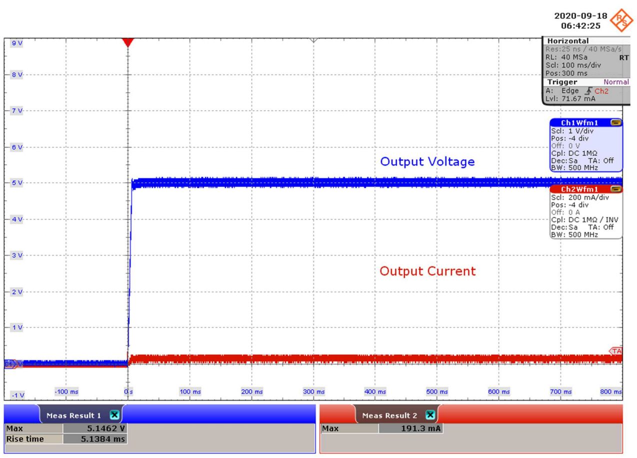

Figure 38 – 230 VAC 50 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

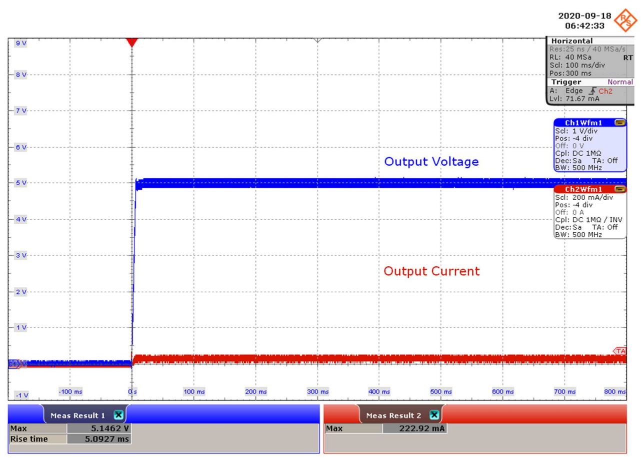

Figure 39 – 265 VAC 50 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 1 V / div., 100 ms / div.
Lower: I_{OUT}, 200 mA / div., 100 ms / div.
Output Rise Monotonically.

15.3 *Switching Waveforms*

15.3.1 Drain-to-Source Voltage and Current at Normal Operation

15.3.1.1 100% Load

Figure 40 – 85 VAC 60 Hz, Full Load.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 258.6 V, $I_{DS(MAX)}$ = 273.52 mA.

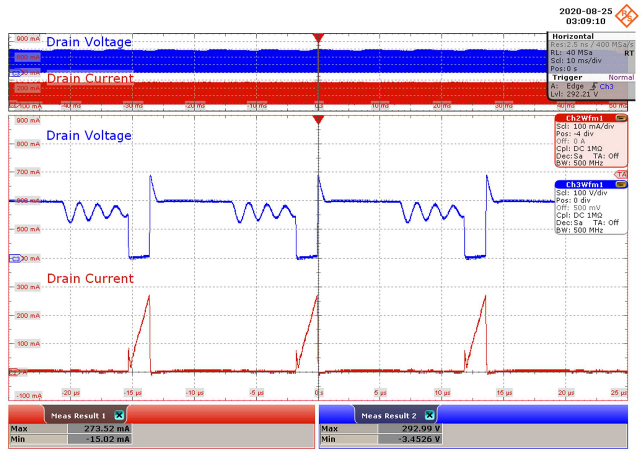

Figure 41 – 115 VAC 60 Hz, Full Load.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 292.99 V, $I_{DS(MAX)}$ = 273.52 mA.

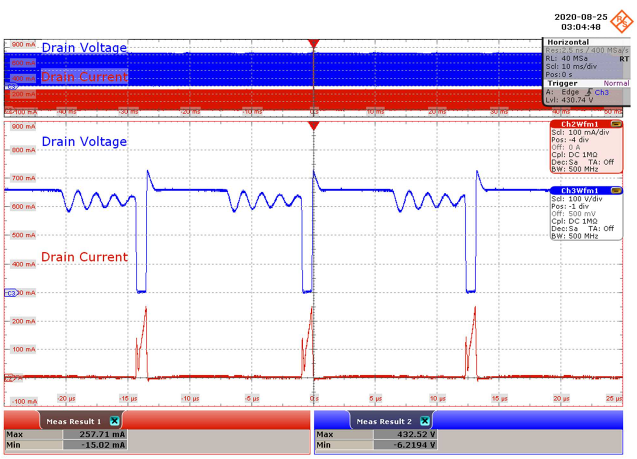

Figure 42 – 230 VAC 50 Hz, Full Load.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 432.52 V, $I_{DS(MAX)}$ = 257.71 mA.

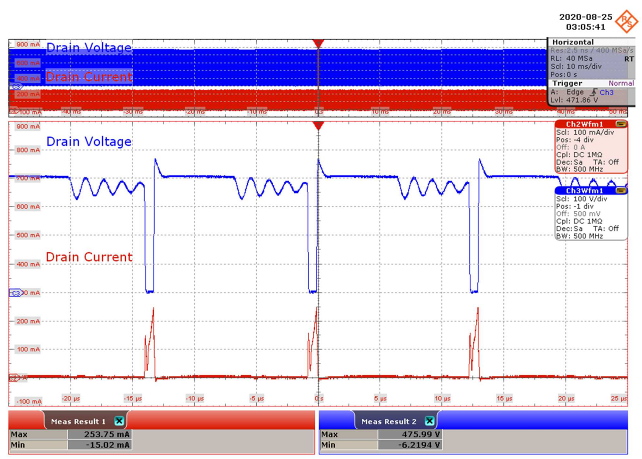

Figure 43 – 265 VAC 50 Hz, Full Load.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 475.99 V, $I_{DS(MAX)}$ = 253.75 mA.

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15.3.1.2 Minimum Load (10% Load)

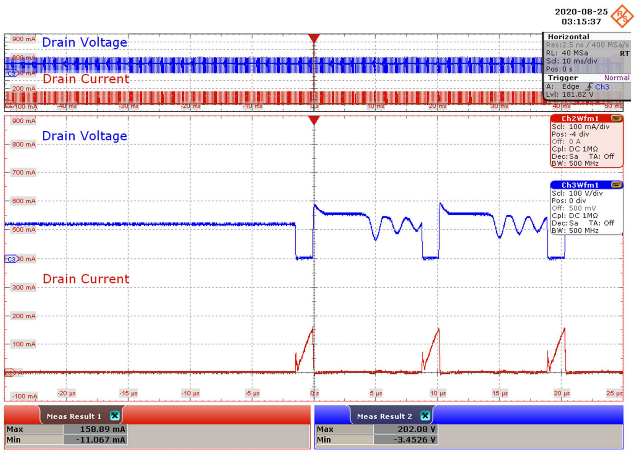

Figure 44 – 85 VAC 60 Hz, Minimum Load
CH2: I_{DS}, 100 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 202.08 V, $I_{DS(MAX)}$ = 158.89 mA.

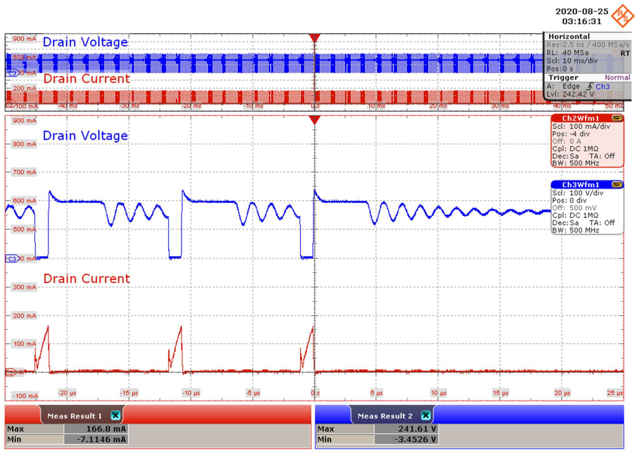

Figure 45 – 115 VAC 60 Hz, Minimum Load
CH2: I_{DS}, 100 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 241.61 V, $I_{DS(MAX)}$ = 166.8 mA.

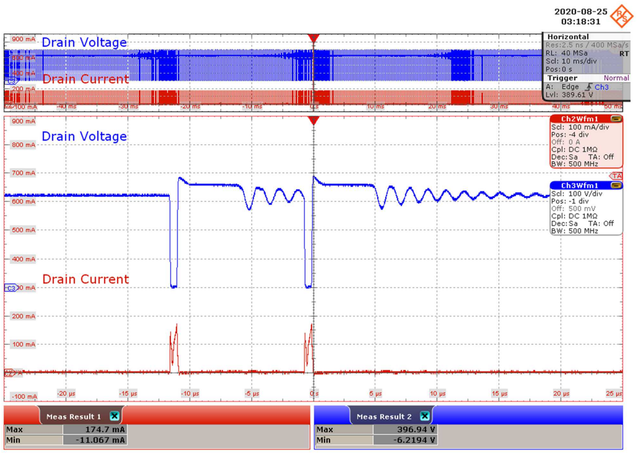

Figure 46 – 230 VAC 50 Hz, Minimum Load
CH2: I_{DS}, 100 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 396.94 V, $I_{DS(MAX)}$ = 174.7 mA.

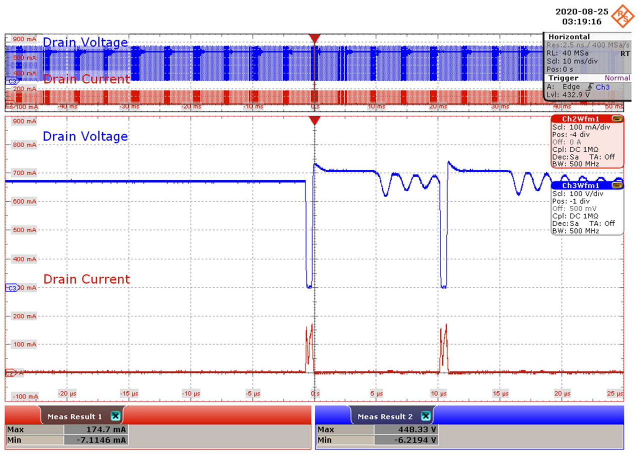

Figure 47 – 265 VAC 50 Hz, Minimum Load
CH2: I_{DS}, 100 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 448.33 V, $I_{DS(MAX)}$ = 174.7 mA.

15.3.2 Drain-to-Source Voltage and Current at Start-up Operation

15.3.2.1 100% Load

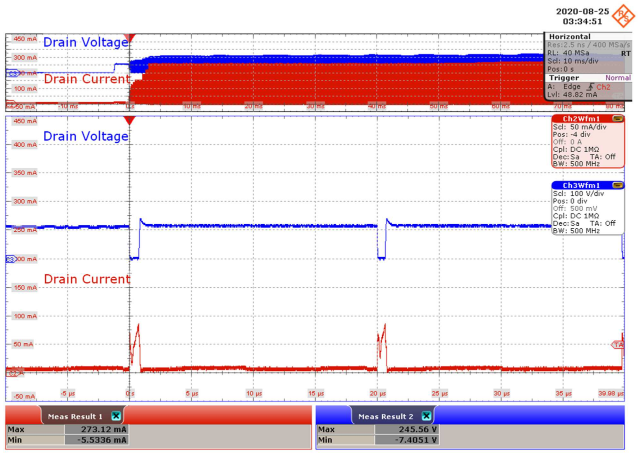

Figure 48 – 85 VAC 60 Hz, Full Load Start-up.
CH2: I_{DS}, 50 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 245.56 V, $I_{DS(MAX)}$ = 273.12 mA.

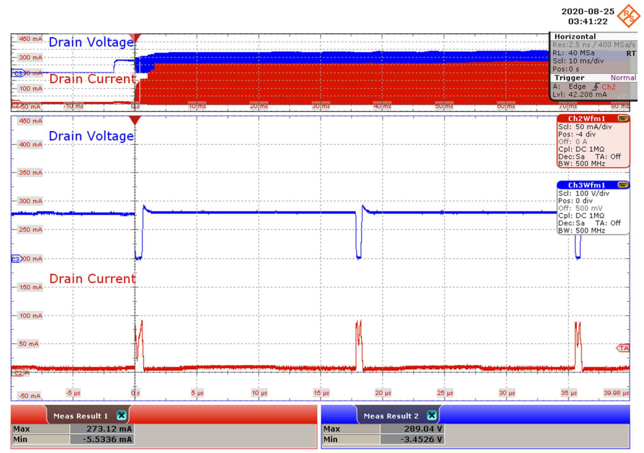

Figure 49 – 115 VAC 60 Hz, Full Load Start-up.
CH2: I_{DS}, 50 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 289.04 V, $I_{DS(MAX)}$ = 273.12 mA.

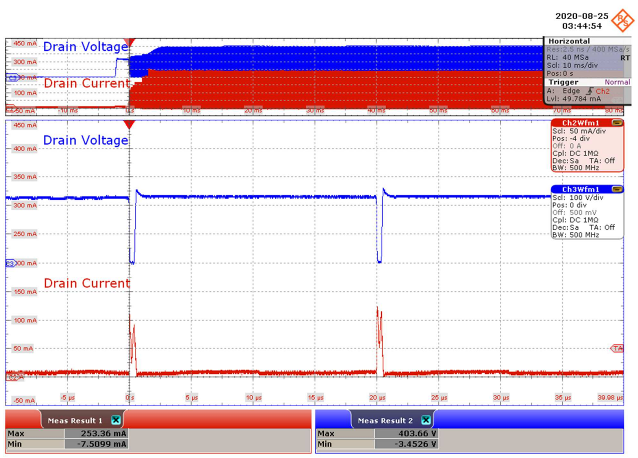

Figure 50 – 230 VAC 50 Hz, Full Load Start-up.
CH2: I_{DS}, 50 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 403.66 V, $I_{DS(MAX)}$ = 253.36 mA.

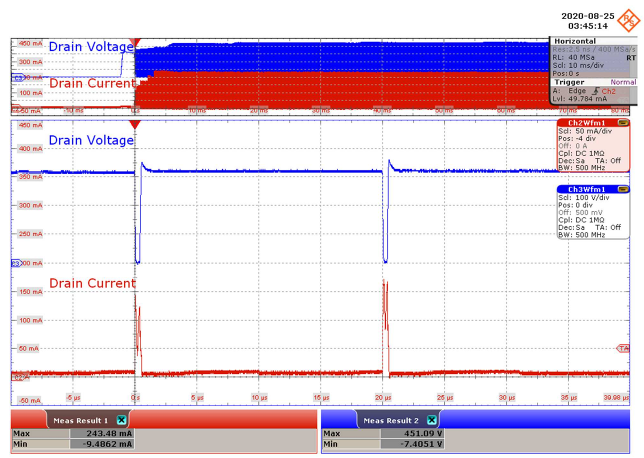

Figure 51 – 265 VAC 50 Hz, Full Load Start-up
CH2: I_{DS}, 50 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 451.09 V, $I_{DS(MAX)}$ = 243.48 mA.

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15.3.2.2 Minimum Load (10% Load)

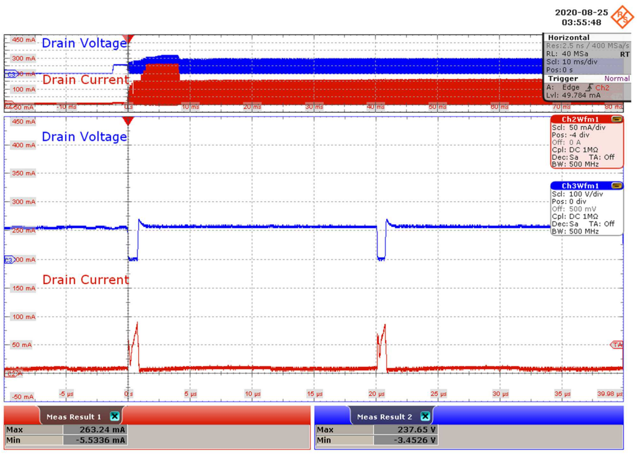

Figure 52 – 85 VAC 60 Hz, Minimum Load Start-up.
CH2: I_{DS}, 50 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 237.65 V, $I_{DS(MAX)}$ = 263.24 mA.

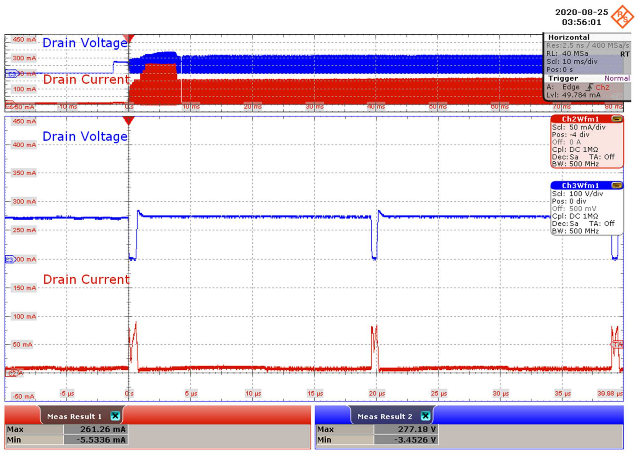

Figure 53 – 115 VAC 60 Hz, Minimum Load Start-up.
CH2: I_{DS}, 50 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 277.18 V, $I_{DS(MAX)}$ = 261.26 mA.

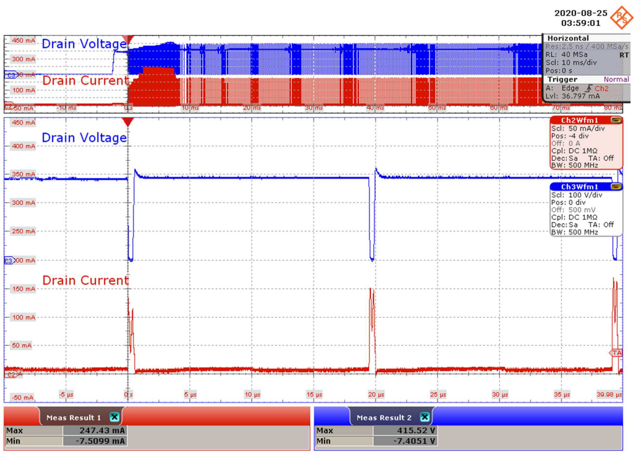

Figure 54 – 230 VAC 50 Hz, Minimum Load Start-up.
CH2: I_{DS}, 50 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 415.52 V, $I_{DS(MAX)}$ = 247.43 mA.

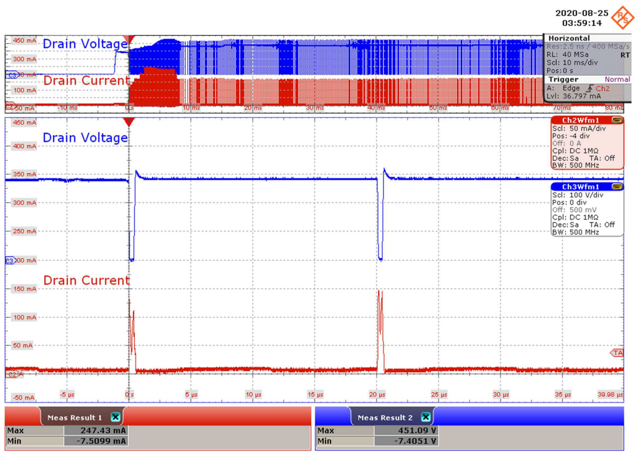

Figure 55 – 265 VAC 50 Hz, Minimum Load Start-up.
CH2: I_{DS}, 50 mA / div., 10 ms / div.
CH3: V_{DS}, 100 V / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 451.09 V, $I_{DS(MAX)}$ = 247.43 mA.

15.3.3 Output Diode Voltage and Current at Normal Operation

15.3.3.1 100% Load

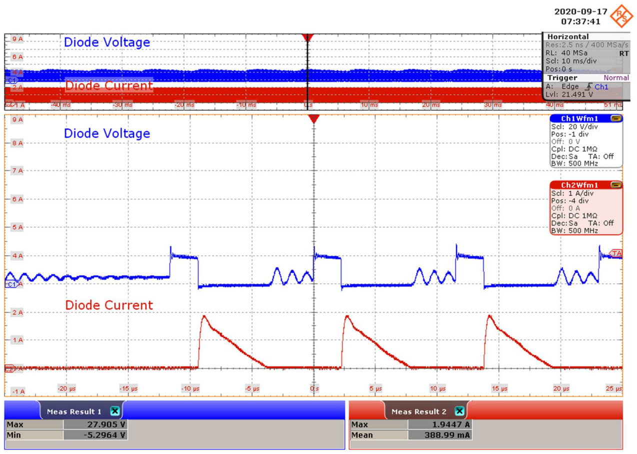

Figure 56 – 85 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 27.91 V.

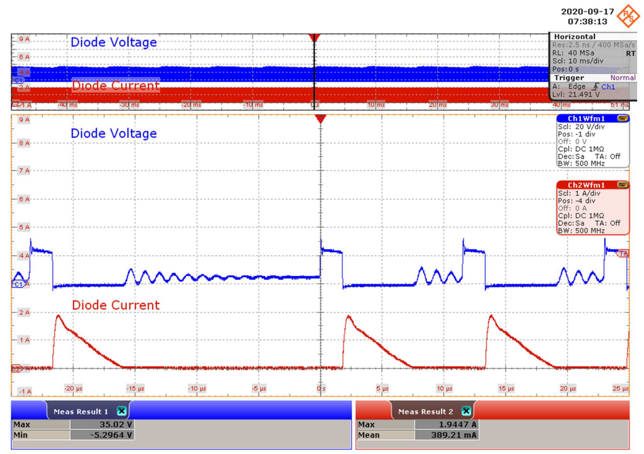

Figure 57 – 115 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 35.02 V.

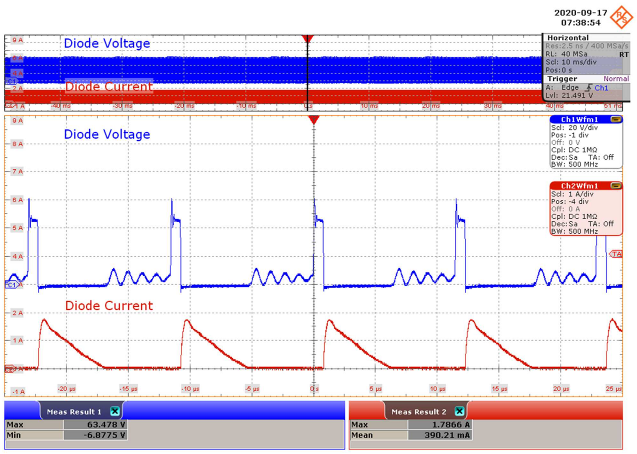

Figure 58 – 230 VAC 50 Hz, Full Load.
CH1: V_{FWL_Diode} - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 63.48 V.

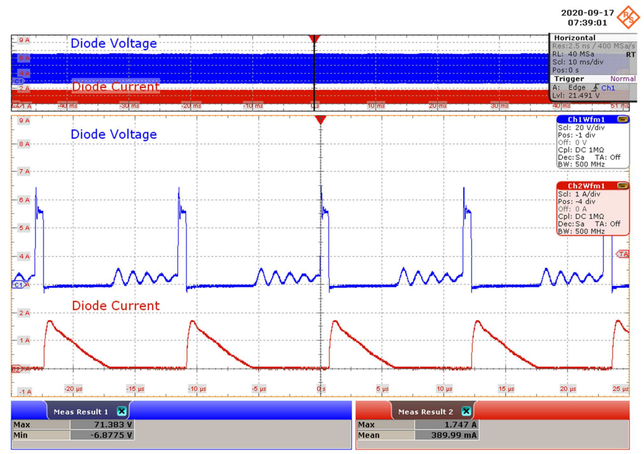

Figure 59 – 265 VAC 50 Hz, Full Load.
CH1: V_{FWL_Diode} - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 71.38 V.

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15.3.3.2 10% Load

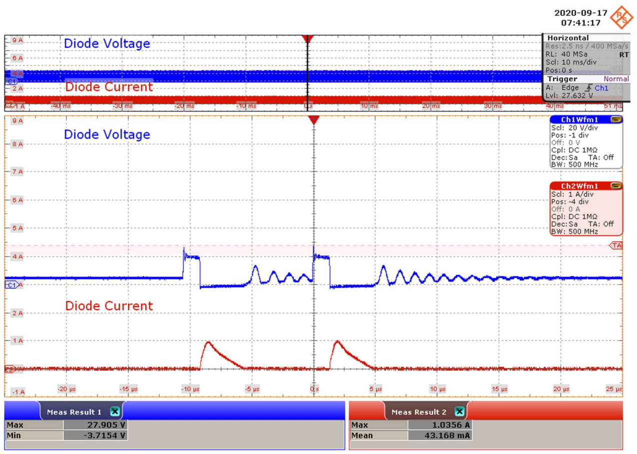

Figure 60 – 85 VAC 60 Hz, Minimum Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{FWD}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 27.91 V.

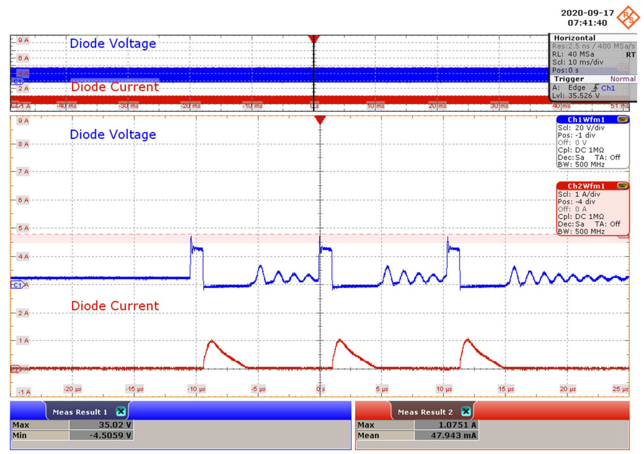

Figure 61 – 115 VAC 60 Hz, Minimum Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{FWD}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 35.02 V.

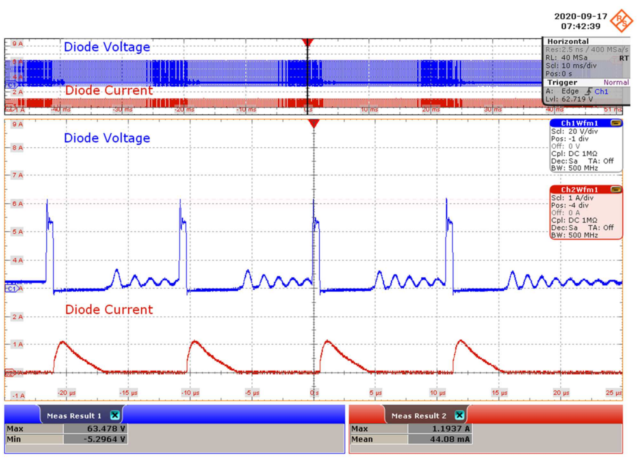

Figure 62 – 230 VAC 60 Hz, Minimum Load.
CH1: V_{FWL_Diode} - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 63.48 V.

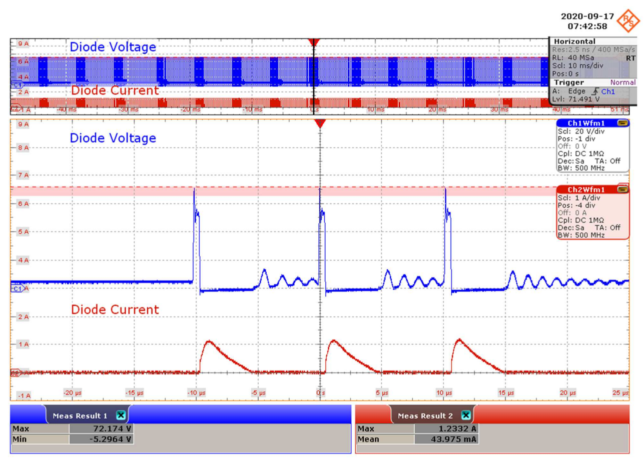

Figure 63 – 265 VAC 60 Hz, Minimum Load.
CH1: V_{FWL_Diode} - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 72.17 V.

15.3.4 Output Diode Voltage and Current at Start-up Operation

15.3.4.1 100% Load

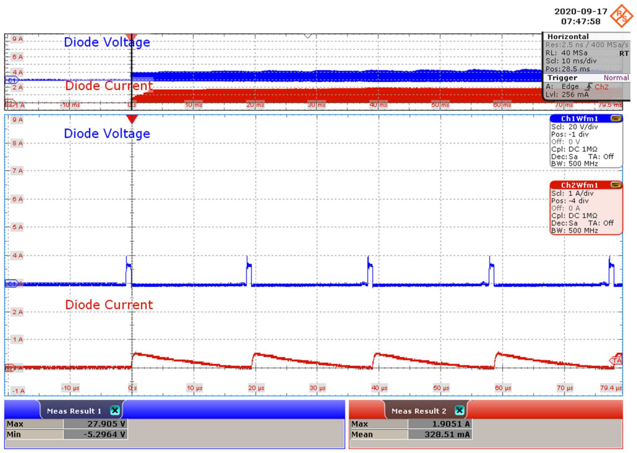

Figure 64 – 85 VAC 60 Hz, Full Load.
CH1: $V_{FWL(DIODE)}$ - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 mA / div., 10 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 27.91 V.

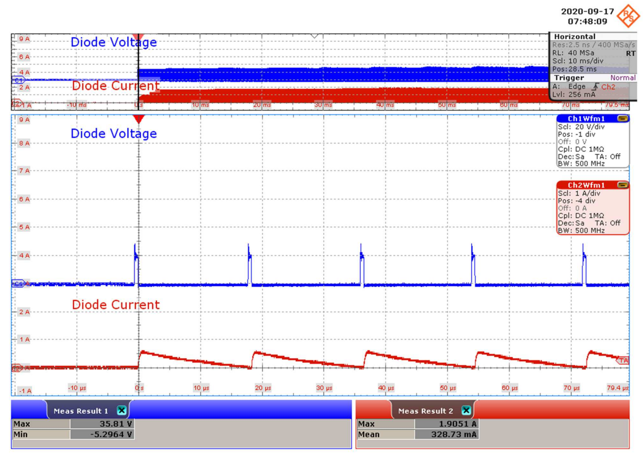

Figure 65 – 115 VAC 60 Hz, Full Load.
CH1: $V_{FWL(DIODE)}$ - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 mA / div., 10 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 35.81 V.

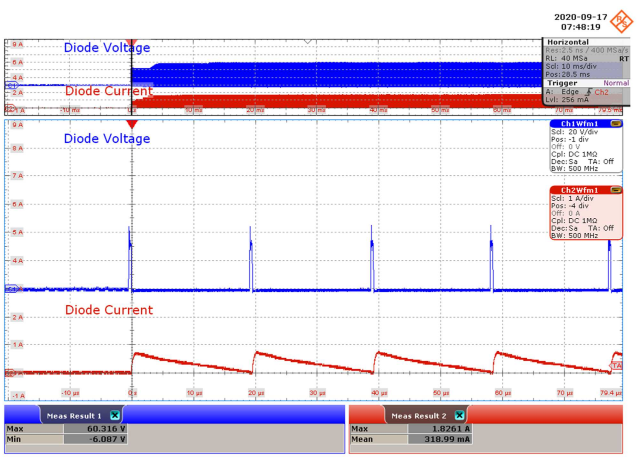

Figure 66 – 230 VAC 50 Hz, Full Load.
CH1: $V_{FWL(DIODE)}$ - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 mA / div., 10 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 68.32 V .

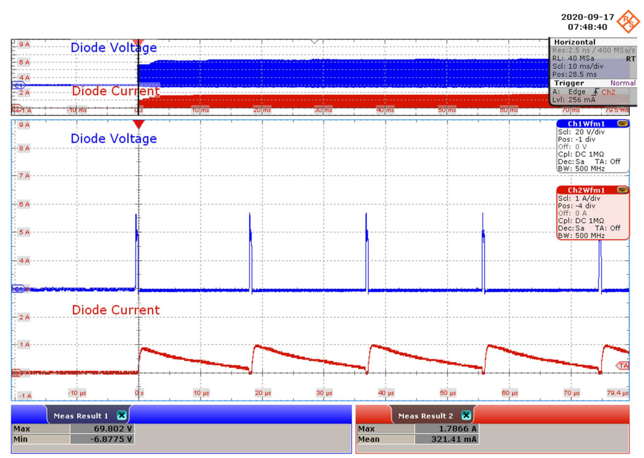

Figure 67 – 265 VAC 50 Hz, Full Load.
CH1: $V_{FWL(DIODE)}$ - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 mA / div., 10 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 69.80 V.

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15.3.4.2 10% Load

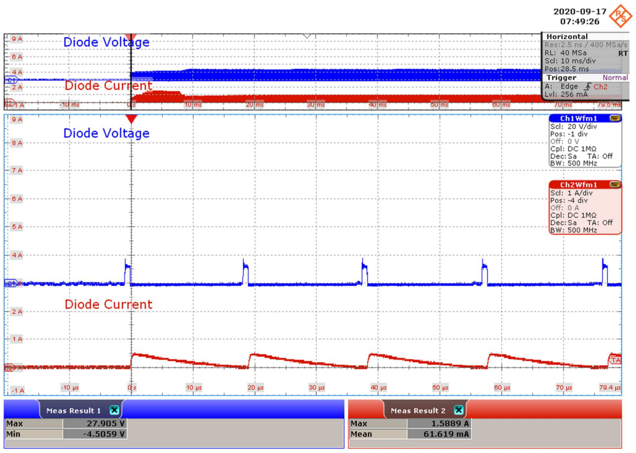

Figure 68 – 85 VAC 60 Hz, Minimum Load.
CH1: $V_{FWL(DIODE)}$ - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 mA / div., 10 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 27.91 V.

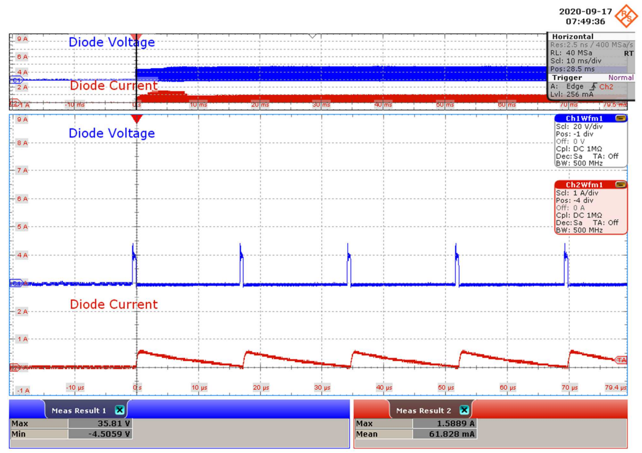

Figure 69 – 115 VAC 60 Hz, Minimum Load.
CH1: $V_{FWL(DIODE)}$ - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 mA / div., 10 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 35.81 V.

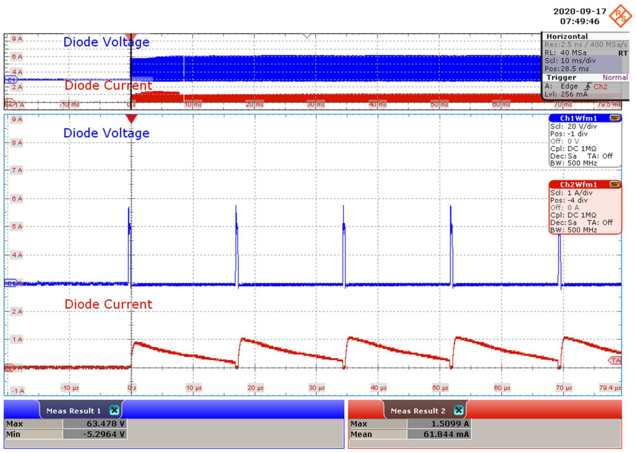

Figure 70 – 230 VAC 50 Hz, Minimum Load.
CH1: $V_{FWL(DIODE)}$ - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 mA / div., 10 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 63.48 V.

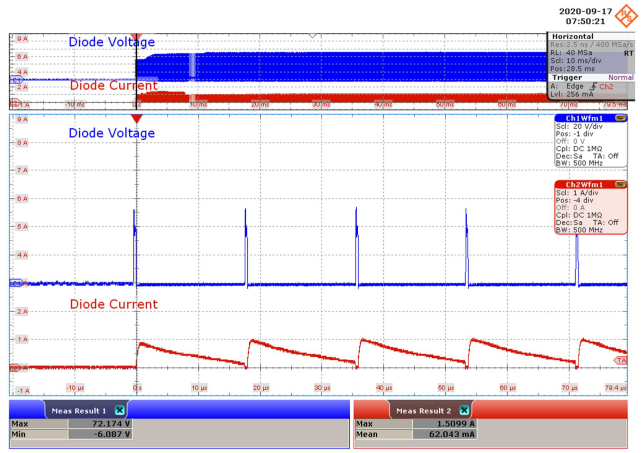

Figure 71 – 265 VAC 50 Hz, Minimum Load.
CH1: $V_{FWL(DIODE)}$ - 20 V / div., 10 ms / div.
CH2: I_{FWD}, 1 mA / div., 10 ms / div.
Zoom: 10 µs / div.
PIV_{MAX} = 72.17 V.

15.4 *Output Short-Circuit Auto-restart Test*

Output is shorted at the end of the cable.

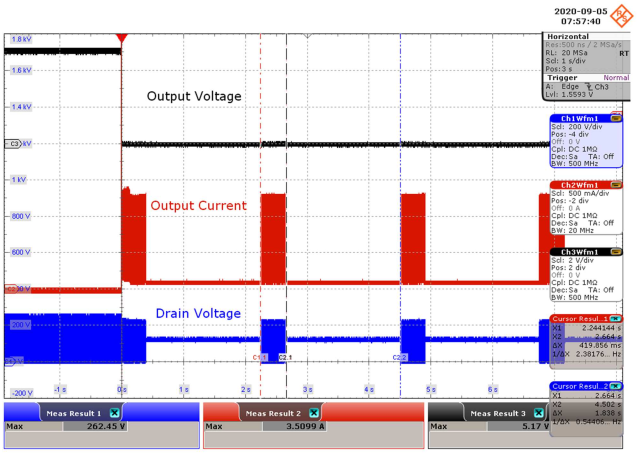

Figure 72 – 90 VAC, Normal Operation.
CH1: V_{DS}, 200 V / div., 1 s /div.
CH2: I_{OUT}, 500 mA / div., 1 s / div.
CH3: V_{OUT}, 2 V / div., 1 s / div.
$t_{AR(ON)}$: 420 ms.
$t_{AR(OFF)}$: 1.84 s.

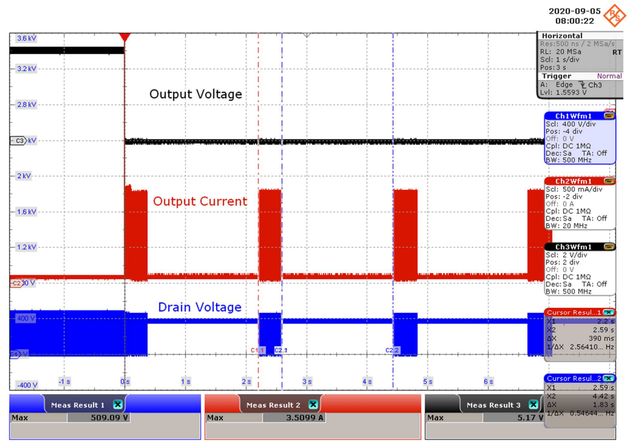

Figure 73 – 265 VAC, Normal Operation.
CH1: V_{DS}, 400 V / div., 1 s /div.
CH2: I_{OUT}, 500 mA / div., 1 s / div.
CH3: V_{OUT}, 2 V / div., 1 s / div.
$t_{AR(ON)}$: 390 ms.
$t_{AR(OFF)}$: 1.83 s.

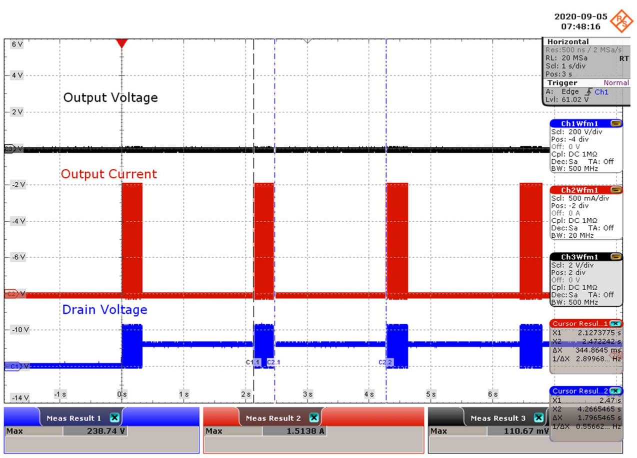

Figure 74 – 90 VAC, Start-up Operation.
CH1: V_{DS}, 200 V / div., 1 s /div.
CH2: I_{OUT}, 500 mA / div., 1 s / div.
CH3: V_{OUT}, 2 V / div., 1 s / div.
$t_{AR(ON)}$: 345 ms.
$t_{AR(OFF)}$: 1.80 s.

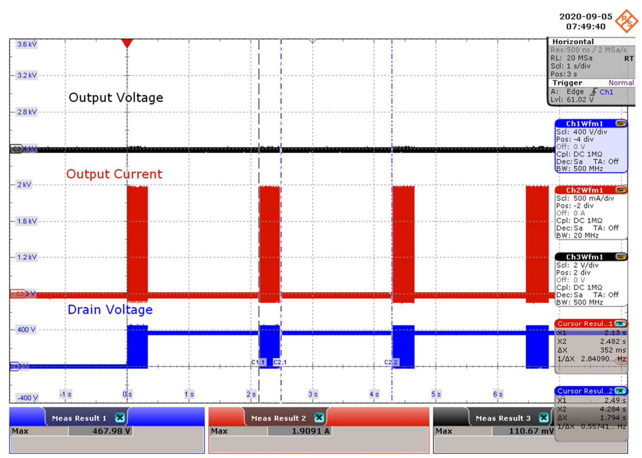

Figure 75 – 265 VAC, Start-up Operation.
CH1: V_{DS}, 400 V / div., 1 s /div.
CH2: I_{OUT}, 500 mA / div., 1 s / div.
CH3: V_{OUT}, 2 V / div., 1 s / div.
$t_{AR(ON)}$: 352 ms.
$t_{AR(OFF)}$: 1.79 s.

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15.5 ***Output Ripple Measurements***

15.5.1 Output Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

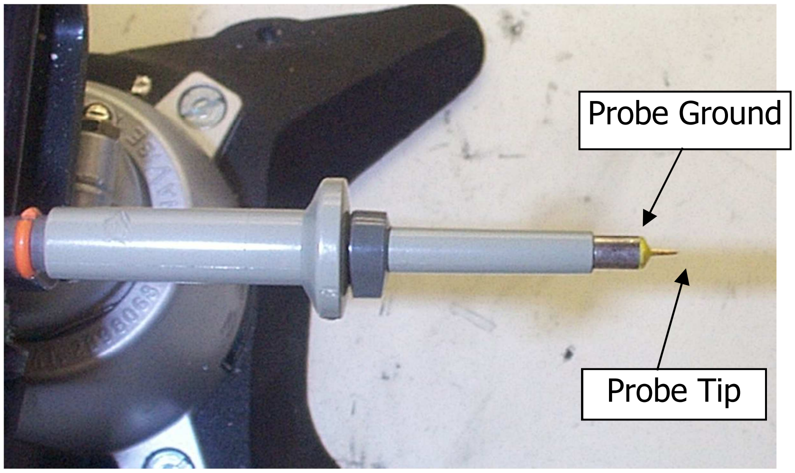

Figure 76 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

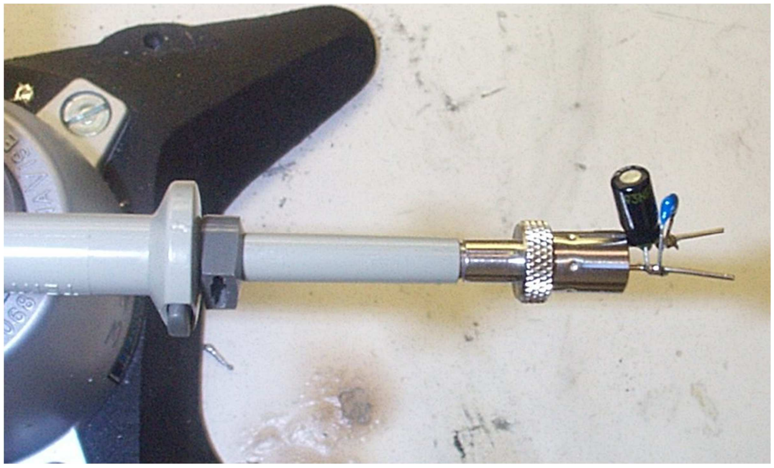

Figure 77 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

15.5.2 Measurement Results

Measured across the PCB connector.

15.5.2.1 100% Load Condition

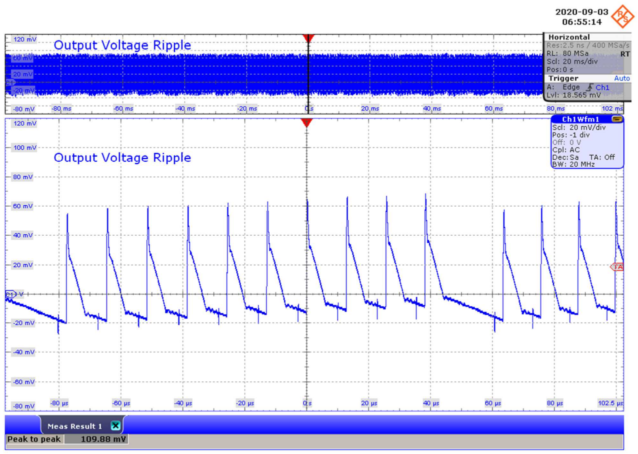

Figure 78 – 85 VAC 60 Hz, 100% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 110 mV).

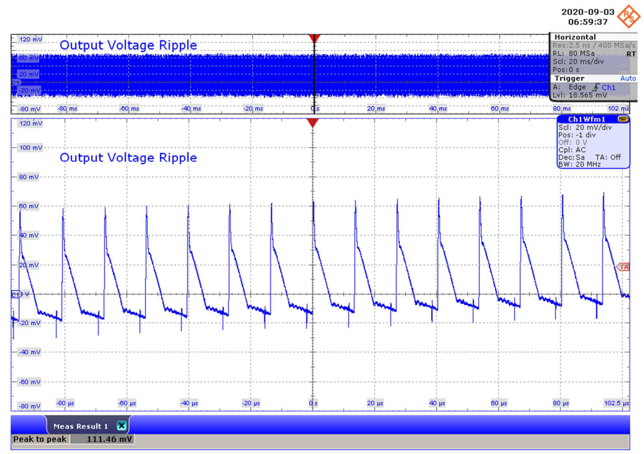

Figure 79 – 115 VAC 60 Hz, 100% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 111 mV).

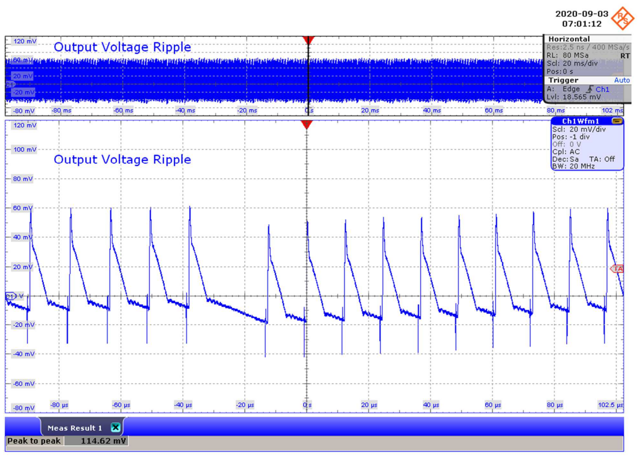

Figure 80 – 230VAC 50 Hz, 100% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 115 mV).

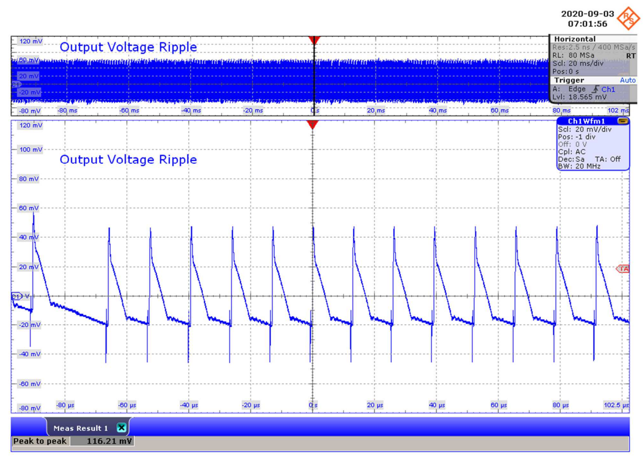

Figure 81 – 265VAC 50 Hz, 100% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 116 mV).

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15.5.2.2 75% Load Condition

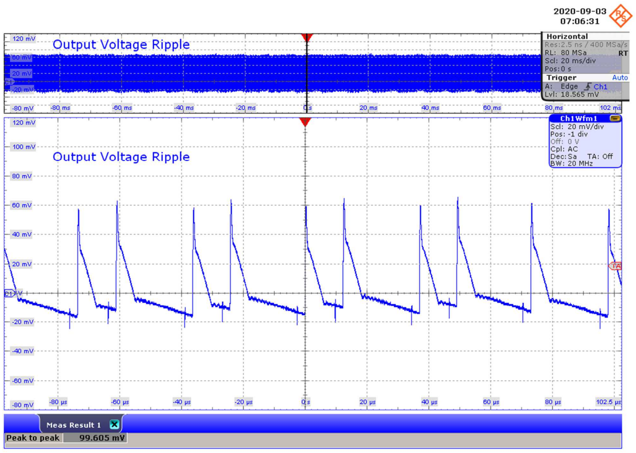

Figure 82 – 85 VAC 60 Hz, 75% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 100 mV).

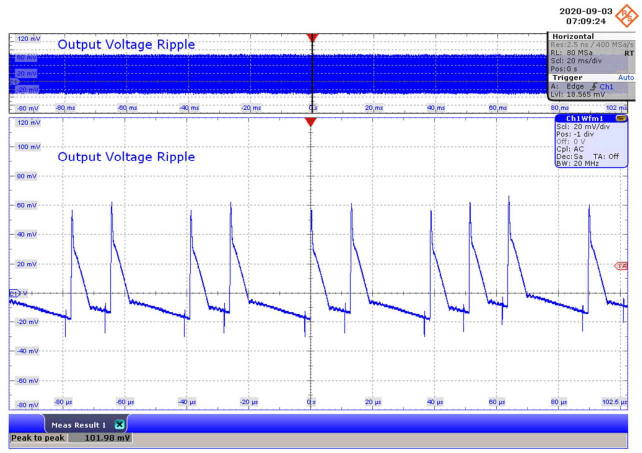

Figure 83 – 115 VAC 60 Hz, 75% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 102 mV).

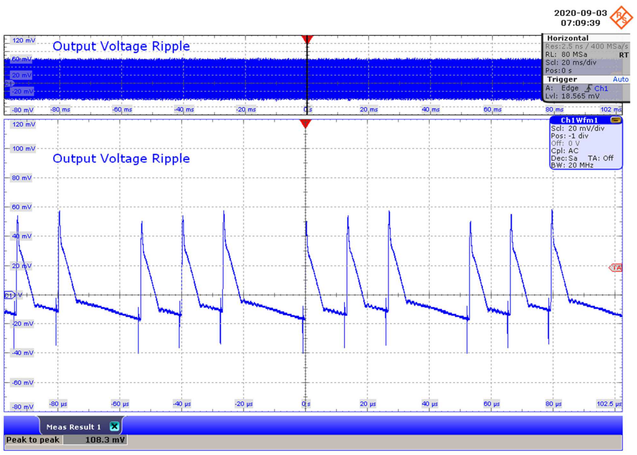

Figure 84 – 230 VAC 65 Hz, 75% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 108 mV).

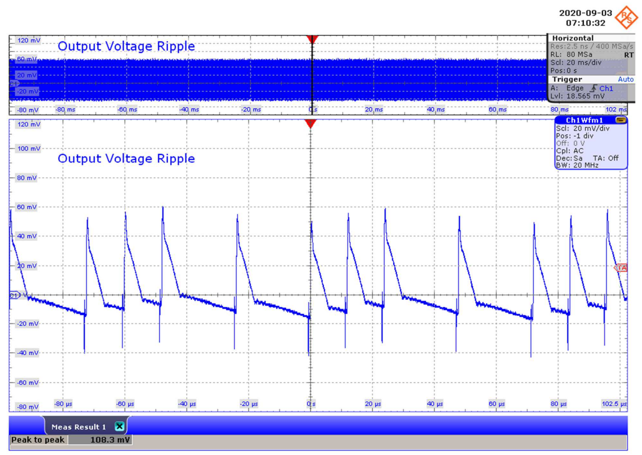

Figure 85 – 265 VAC 50 Hz, 75% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 108 mV).

15.5.2.3 50% Load Condition

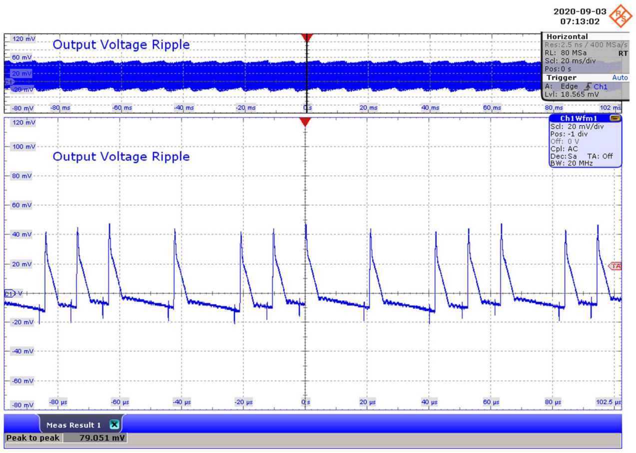

Figure 86 – 85 VAC 60 Hz, 50% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 79 mV).

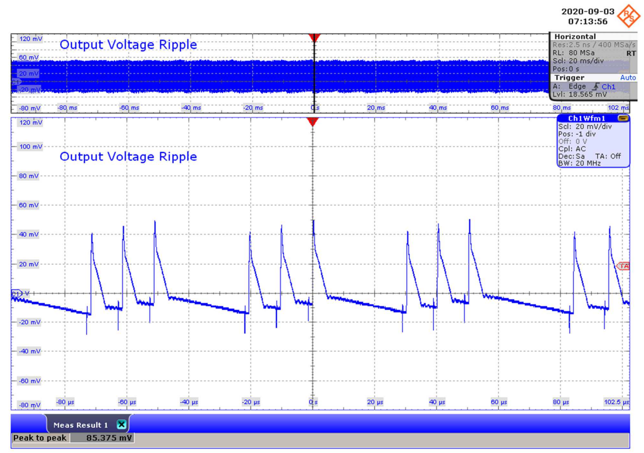

Figure 87 – 115 VAC 60 Hz, 50% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 85 mV).

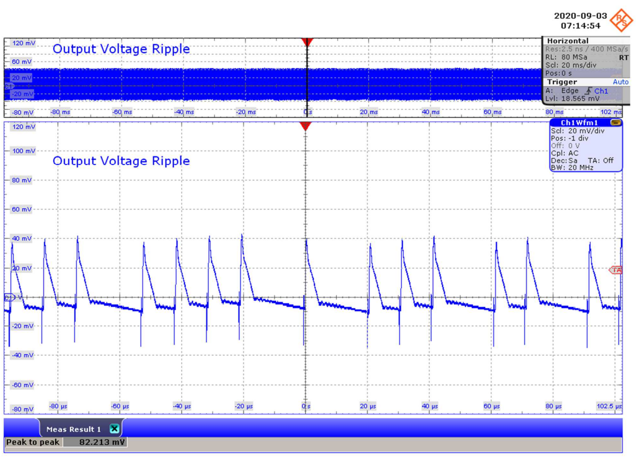

Figure 88 – 230 VAC 50 Hz, 50% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 82 mV).

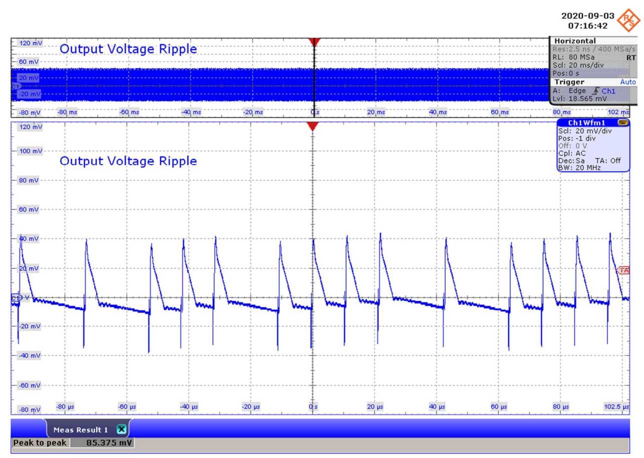

Figure 89 – 265 VAC 50 Hz, 50% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 85 mV).

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15.5.2.4 25% Load Condition

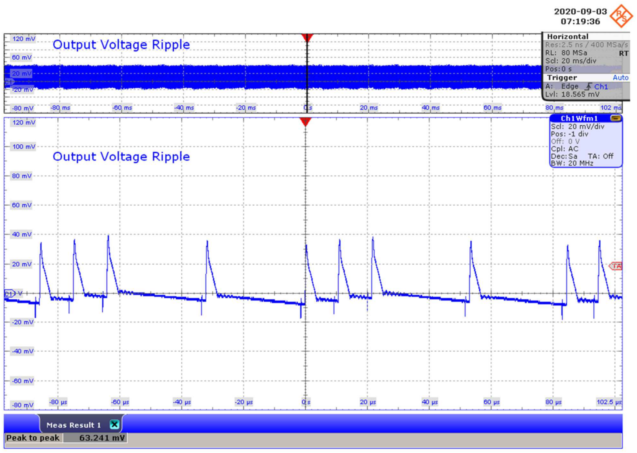

Figure 90 – 85 VAC 60 Hz, 25% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 63 mV).

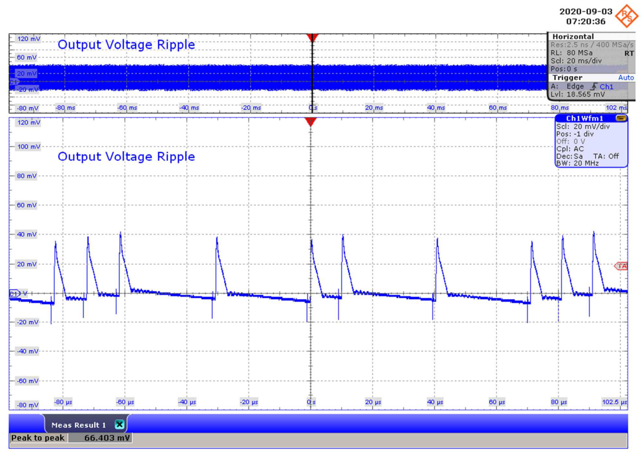

Figure 91 – 115 VAC 60 Hz, 25% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 66 mV).

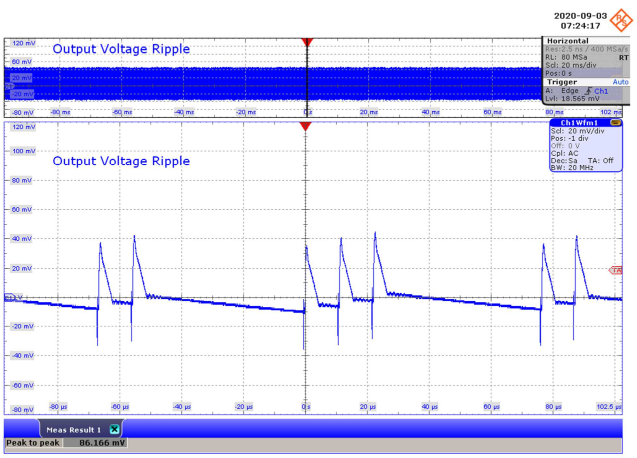

Figure 92 – 230 VAC 50 Hz, 25% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 86 mV).

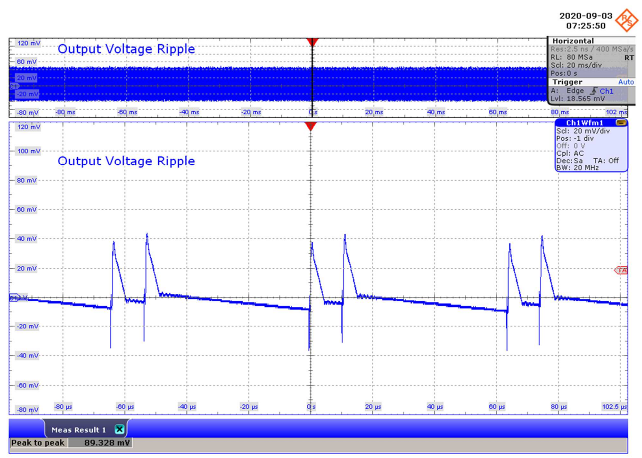

Figure 93 – 265 VAC 50 Hz, 25% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 89 mV).

15.5.2.5 10% Load Condition

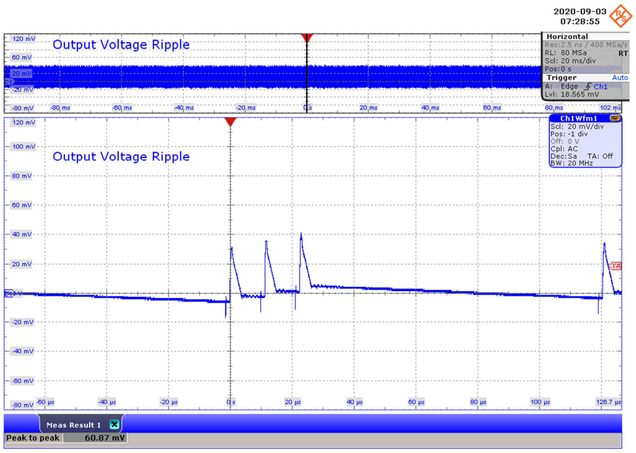

Figure 94 – 85 VAC 60 Hz, 10% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 61 mV).

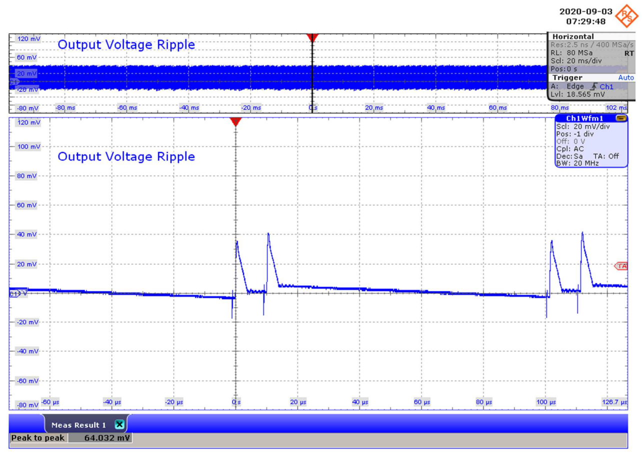

Figure 95 – 115 VAC 60 Hz, 10% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 64 mV).

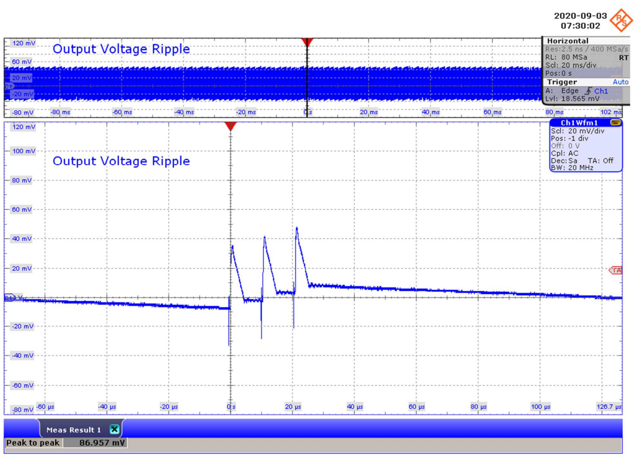

Figure 96 – 230 VAC 60 Hz, 10% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ =87 mV).

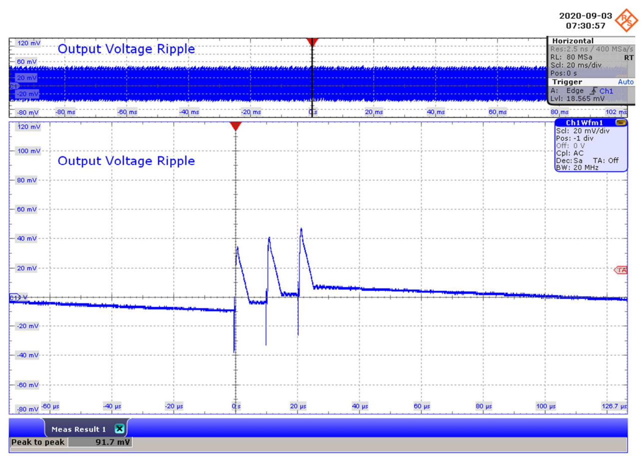

Figure 97 – 265 VAC 60 Hz, 10% Load.
CH1: V_{OUT}, 20 mV / div., 20 ms / div.
Zoom: 20 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 92 mV).

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15.5.3 Output Ripple at Room Temperature

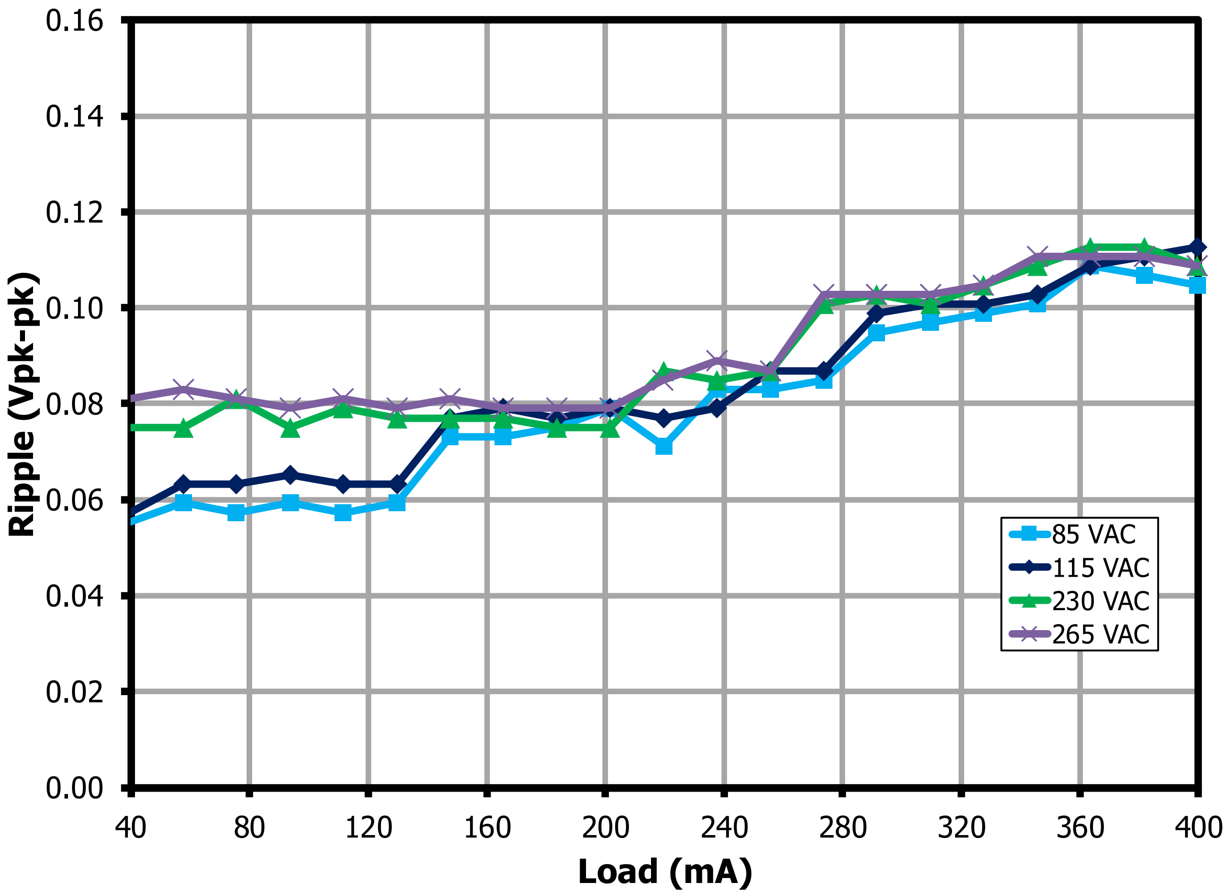

Figure 98 – Output Ripple at Room Temperature.

16 Conducted EMI

16.1 *Test Set-up*

16.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture.
5. Full Load with input voltage set at 230 VAC and 115 VAC.

Figure 99 – Conducted EMI Test Set-up.

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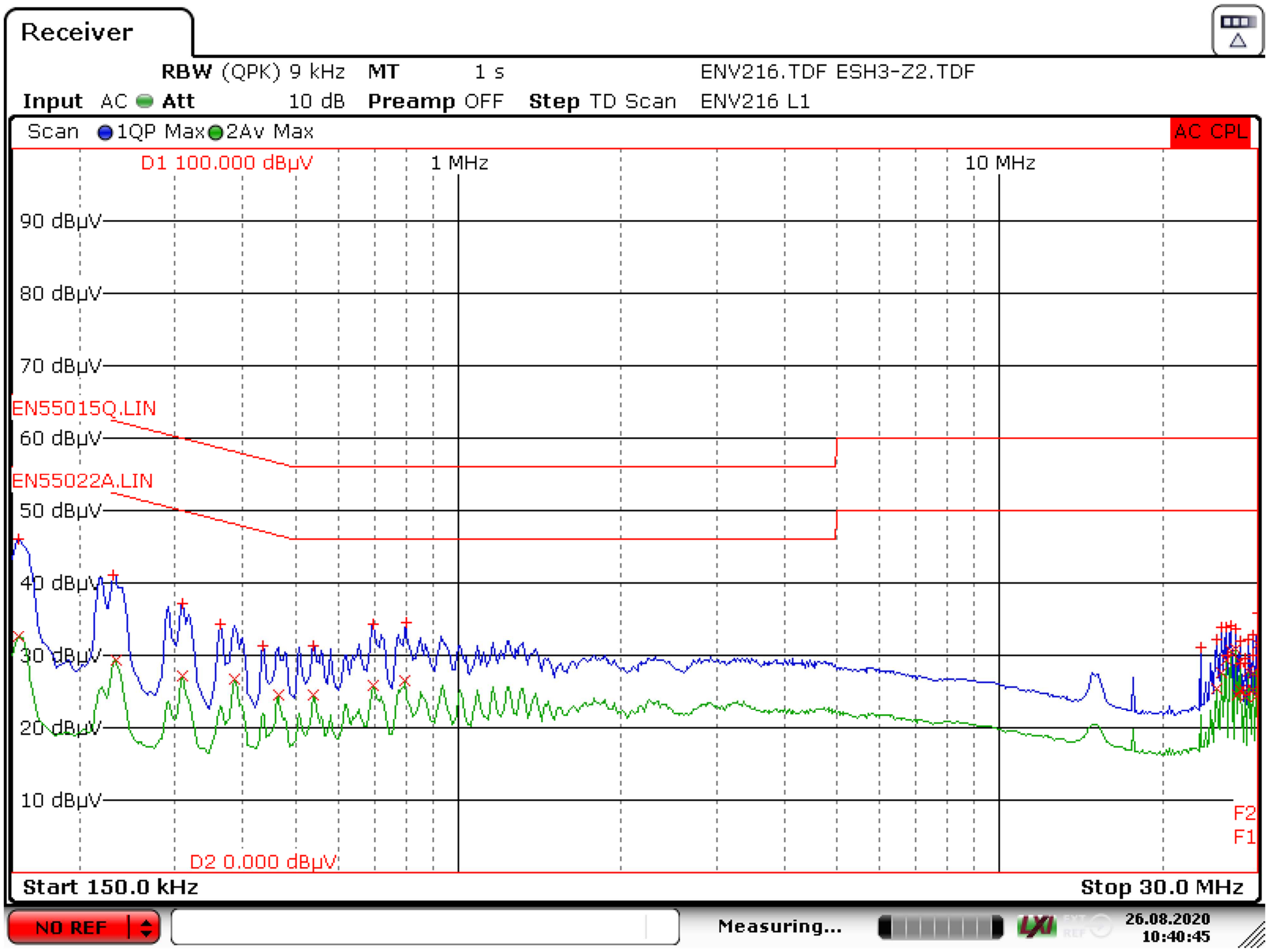
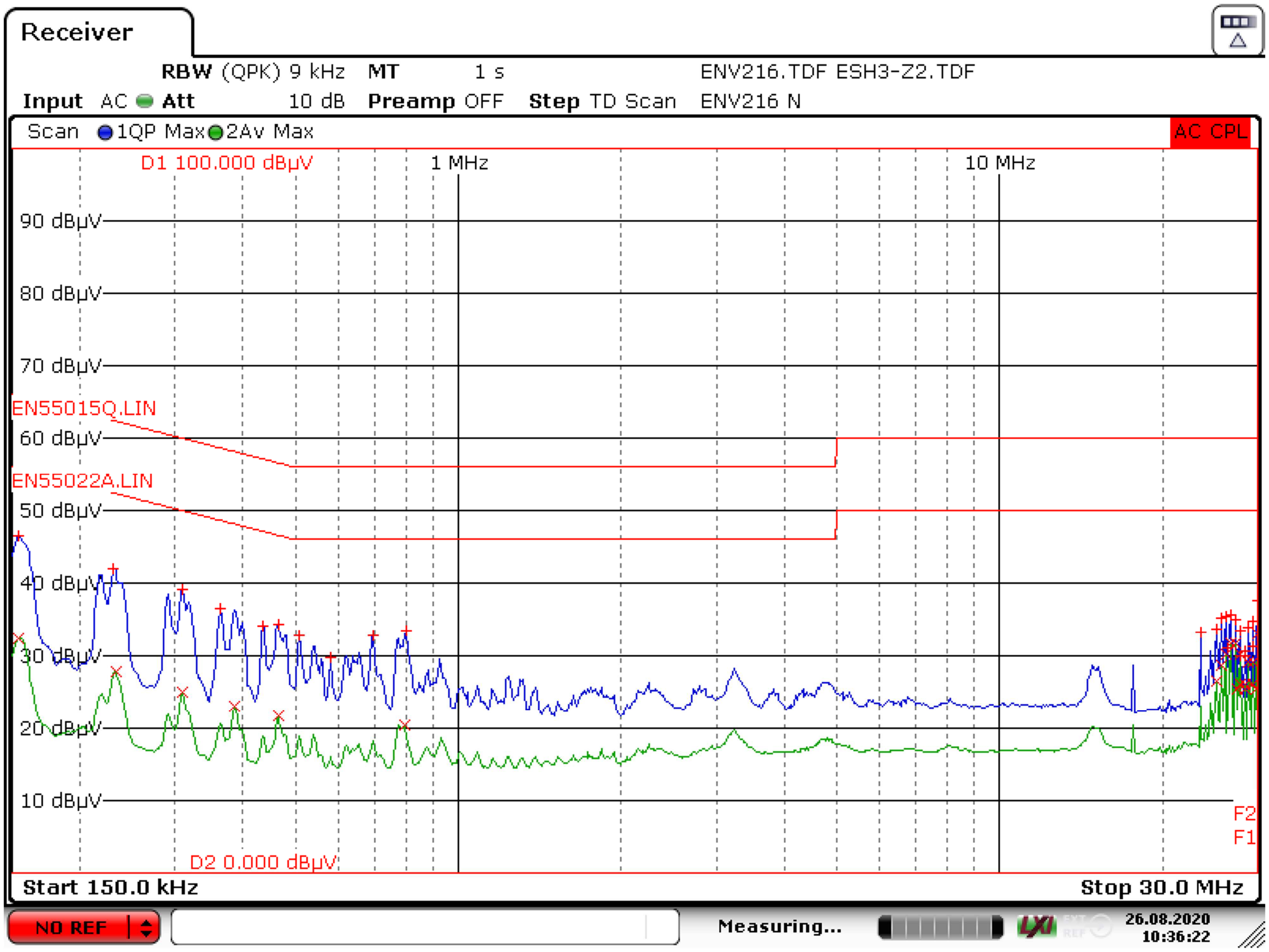
16.2 *2 W Resistive Load, Floating Output*

16.2.1 115 VAC



Date: 26.AUG.2020 10:40:45

Figure 100 – Floating Ground EMI at 115 VAC, Line.



Date: 26.AUG.2020 10:36:23

Figure 101 – Floating Ground EMI at 115 VAC, Neutral.

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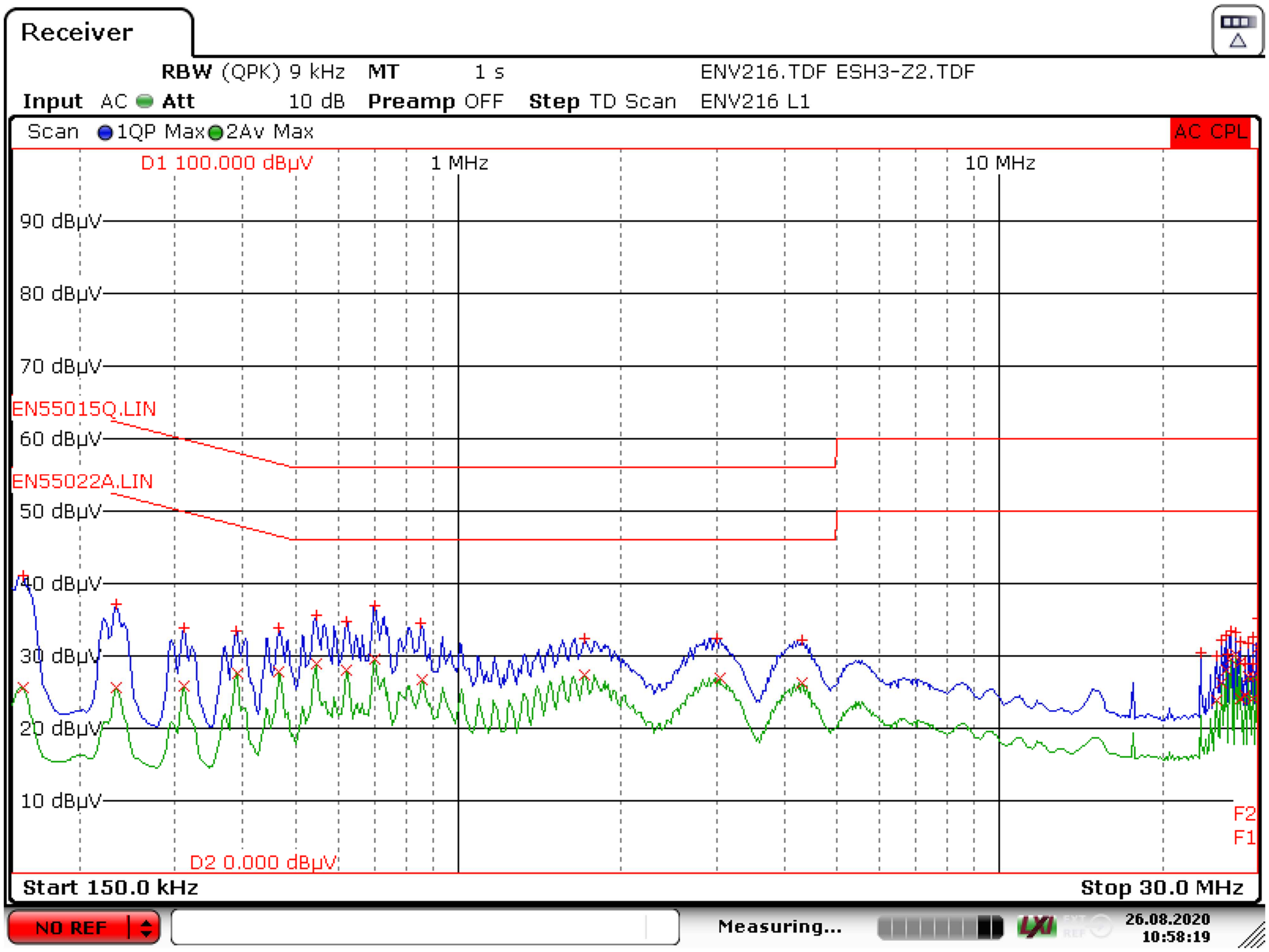
16.2.2 230 VAC



Date: 26.AUG.2020 10:58:20

Figure 102 – Floating Ground EMI at 230 VAC, Line.

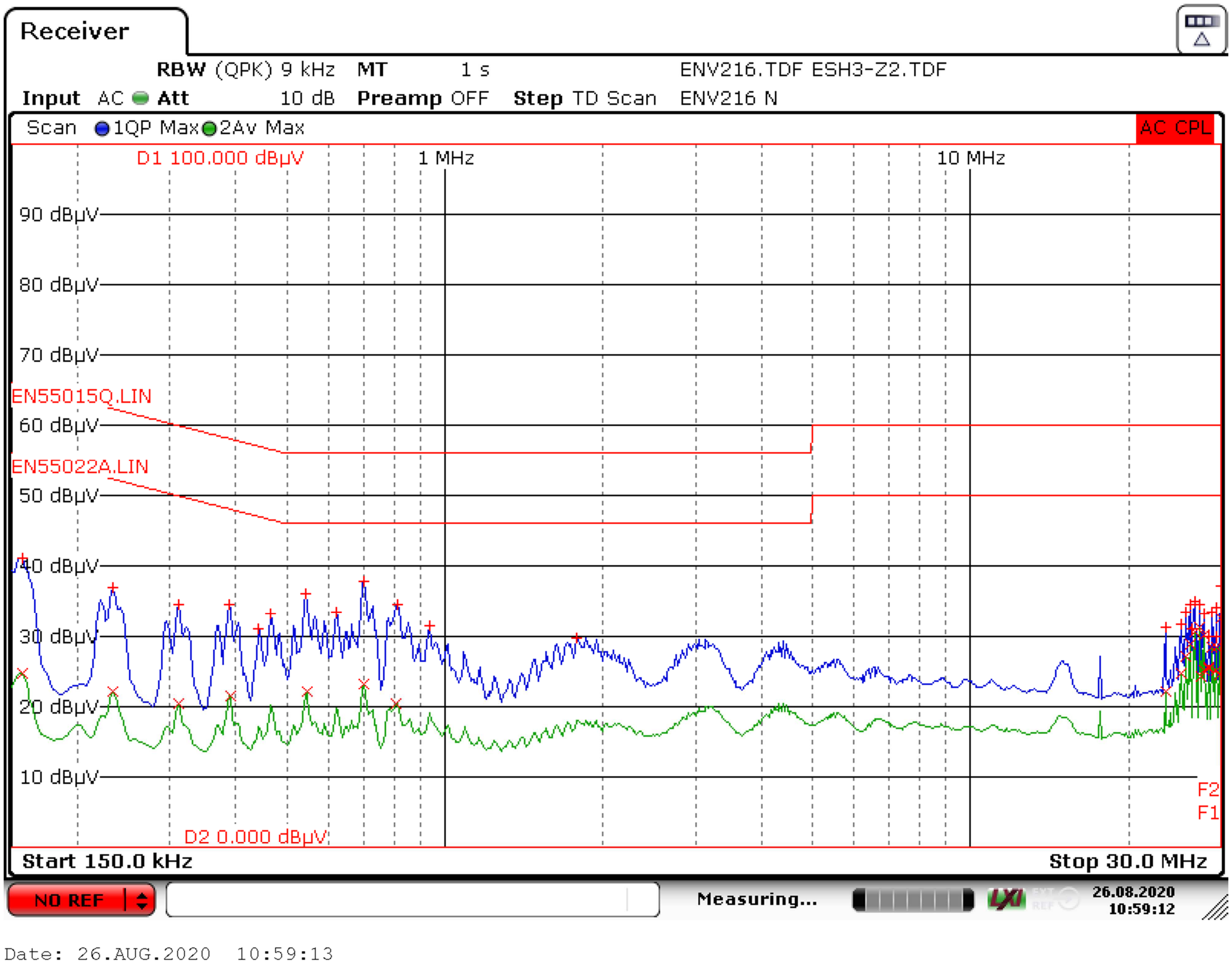


Figure 103 – Floating Ground EMI at 230 VAC, Neutral.

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17 Line Surge

The unit was subjected to ±1000 V differential surge test using 10 strikes at each condition. A test failure is defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

17.1 *Differential Surge Test*

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+1	0	L1 / L2	2	10	PASS
-1	0	L1 / L2	2	10	PASS
+1	90	L1 / L2	2	10	PASS
-1	90	L1 / L2	2	10	PASS
+1	180	L1 / L2	2	10	PASS
-1	180	L1 / L2	2	10	PASS
+1	270	L1 / L2	2	10	PASS
-1	270	L1 / L2	2	10	PASS

Note: In all PASSED results, no damage and no auto-restart were observed.

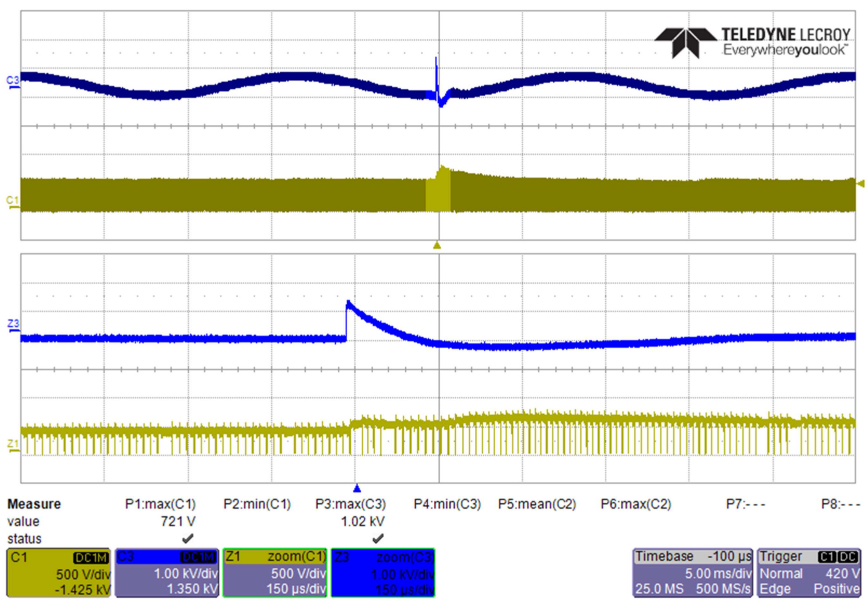

Figure 104 – Input AC Voltage vs. U1 MOSFET V_{DS} during 1 kV Differential Surge.

18 Audible Noise

18.1 *Audible Noise Test Set-up [DER 880 only]*

The unit under test was placed inside an acoustic chamber and the microphone was positioned 10 centimeters above the power supply.

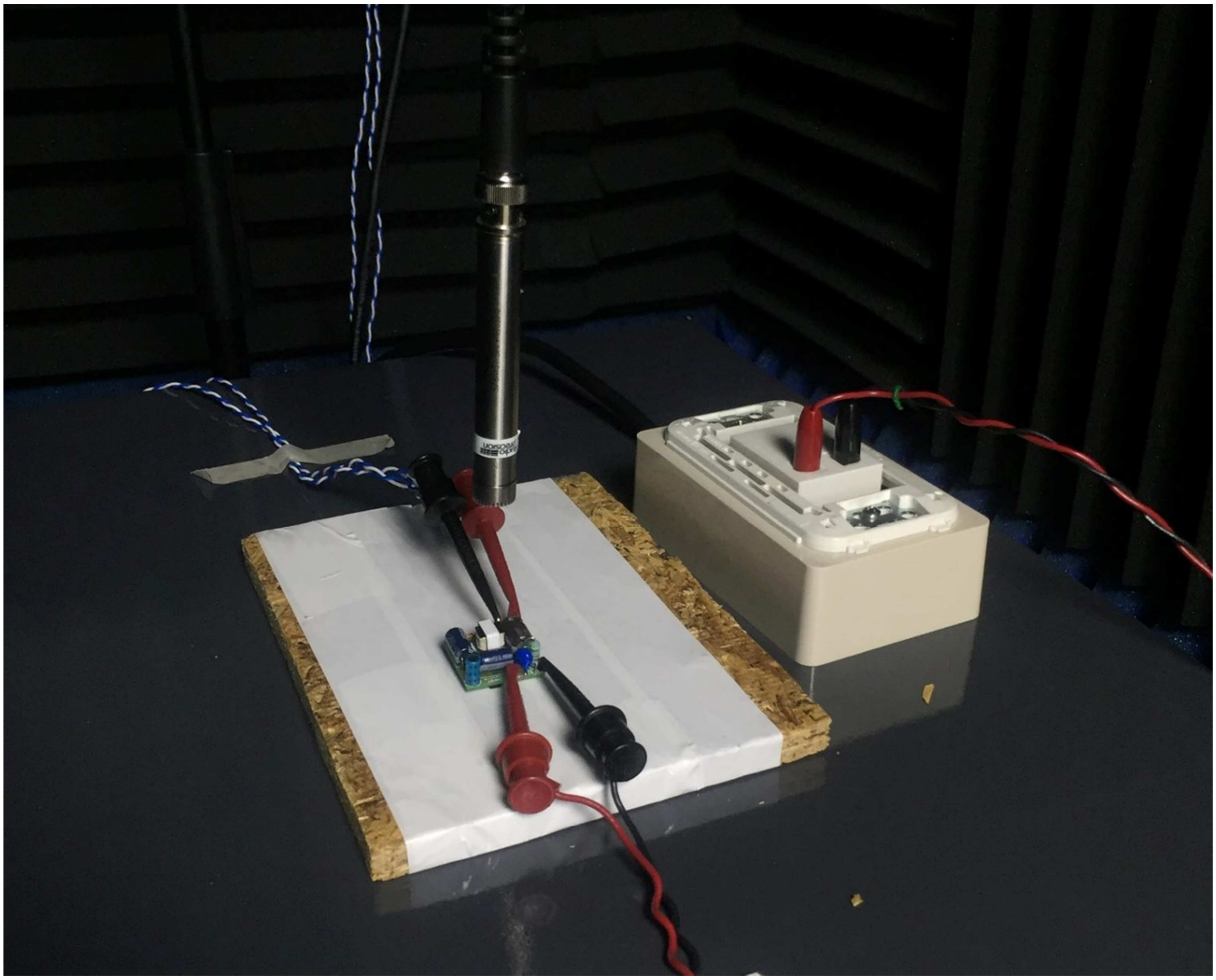

Figure 105 – Acoustic Scan Test Set-up

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18.2 ***DER880 Audible Noise Measurements***

Load Sweep: 400 mA to 40 mA with 10 mA decrement

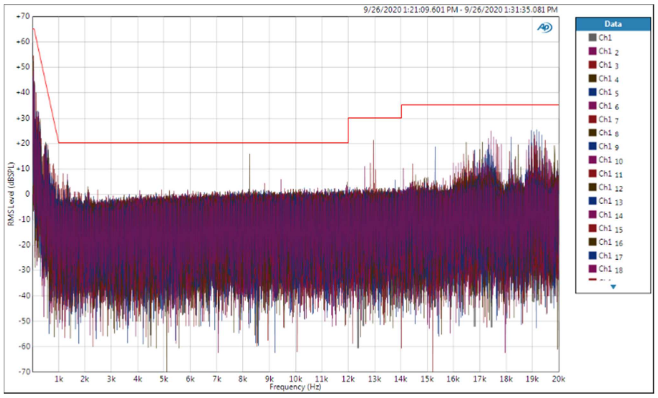

Figure 106 – 115 VAC

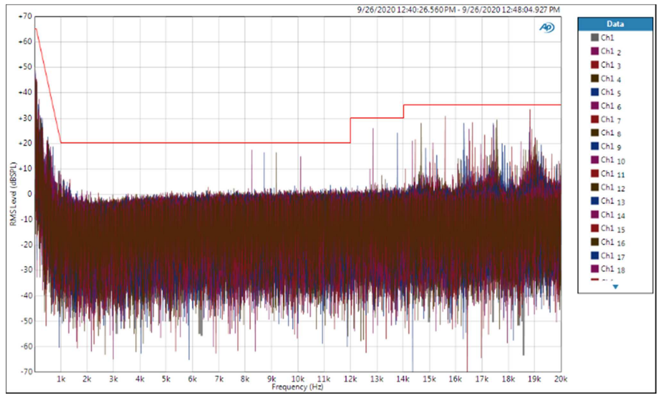

Figure 107 – 230 VAC

18.3 ***Audible Noise Test Set-up [Smart Plug with DER 880]***

The Smart Plug unit under test was placed inside an acoustic chamber and the microphone was positioned 10 centimeters above the Smart Plug.

Audible noise test was performed on the aftermarket Smart Plug. Afterwards, the Smart Plug was reworked to change the power supply to DER-880. Audible noise of uncased Smart Plug and uncased Smart Plug with DER-880 was compared.

Figure 108 – Reworked After Market Smart Plug with DER-880 Inside

18.4 *Audible Noise Measurements [Smart Plug with DER 880]*

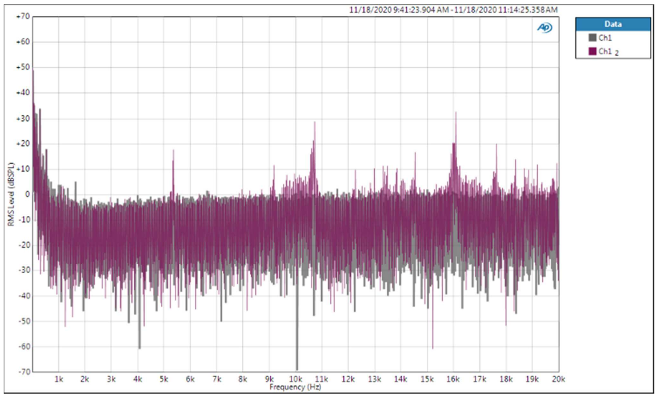

Figure 109 – Uncased Smart Plug.
100 VAC 60 Hz, Smart Plug Disabled.

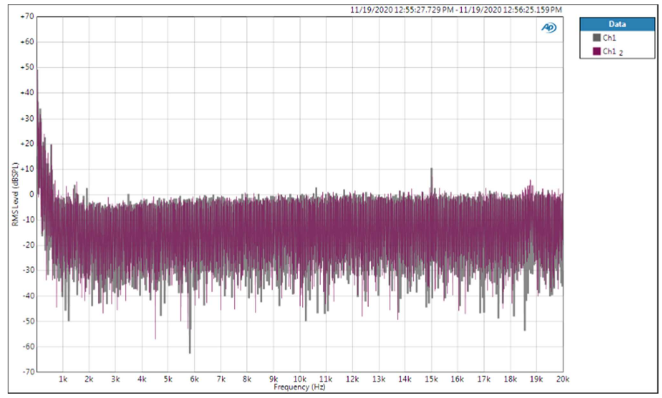

Figure 110 – Uncased Smart Plug with DER 880.
100 VAC 60 Hz, Smart Plug Disabled.

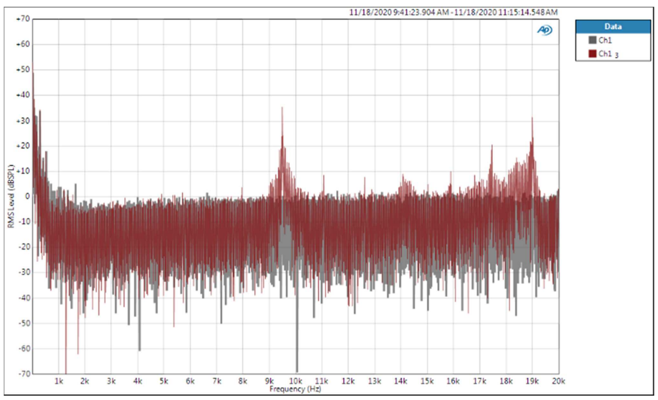

Figure 111 – Uncased Smart Plug.
100 VAC 60 Hz, Smart Plug Enabled.

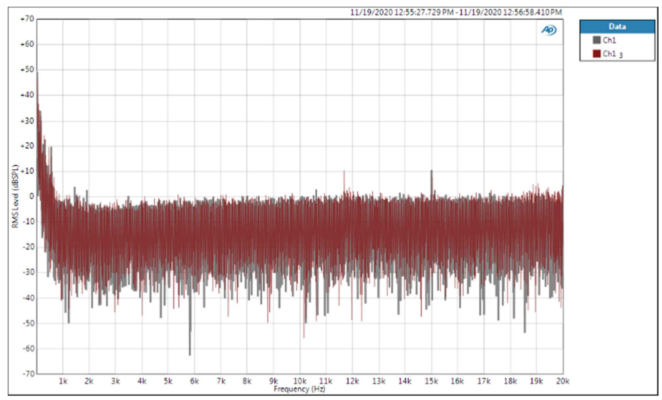

Figure 112 – Uncased Smart Plug with DER 880.
100 VAC 60 Hz, Smart Plug Enabled.

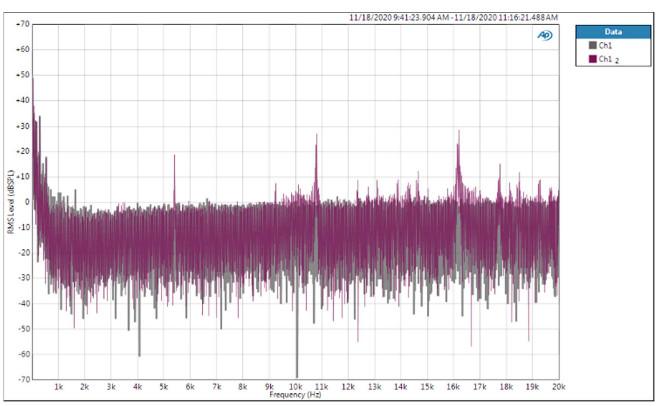

Figure 113 – Uncased Smart Plug.
120 VAC 60 Hz, Smart Plug Disabled.

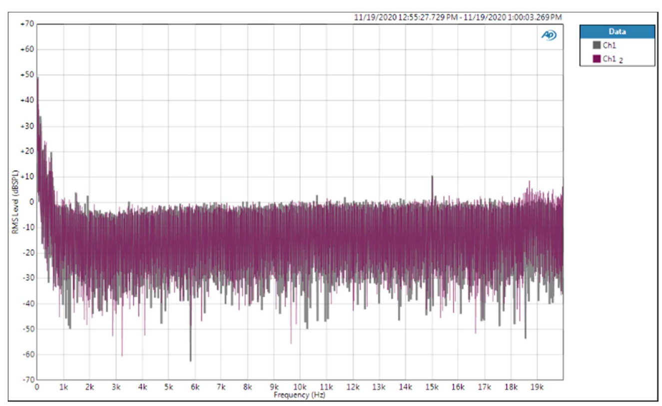

Figure 114 – Uncased Smart Plug with DER 880.
120 VAC 60 Hz, Smart Plug Disabled.

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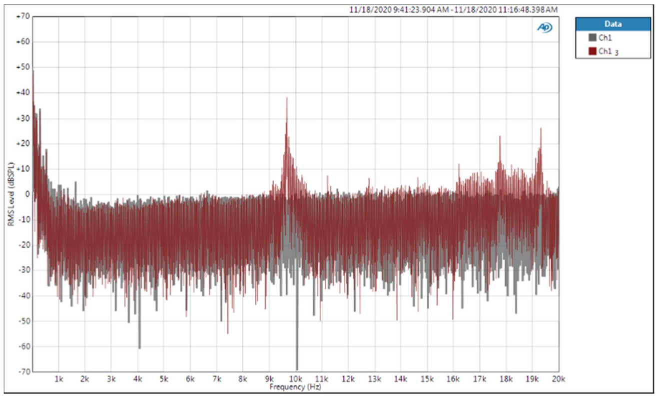

Figure 115 – Uncased Smart Plug.
120 VAC 60 Hz, Smart Plug Enabled.

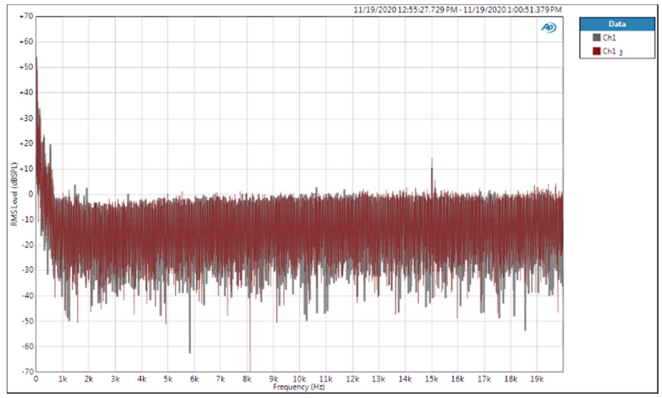

Figure 116 – Uncased Smart Plug with DER 880.
120 VAC 60 Hz, Smart Plug Enabled.

19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
20-Nov-20	MAGM/JKB/ RPA/CMC	1.0	Initial Release	Apps & Mktg

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