Design Example Report

Title	***100 W USB PD 3.0 Power Supply with 3.3 V – 21 V / 5 A (100 W Power-limited) PPS Output Using InnoSwitch™4-Pro PowiGaN™ INN4375F-H341, ClampZero™ CPZ1075M, HiperPFS-5 PFS5274F, and Injoinic IP2726S Controller***
Specification	90 VAC – 265 VAC Input; 5 V / 5 A, 9 V / 5 A, 12 V / 5 A, 15 V / 5 A, 20 V / 5 A, or 3.3 V – 21 V / 5 A PPS (100 W Power-limited) Outputs
Application	USB PD / PPS Power Adapter
Author	Applications Engineering Department
Document Number	DER-960
Date	October 21, 2022
Revision	1.0

Summary and Features

- InnoSwitch4-Pro: Digitally Controllable Off-Line CV/CC ZVS Flyback Integrated Switcher IC with 750 V PowiGaN, Active Clamp Drive and Synchronous Rectification
  - Comprehensive protection features with telemetry for power supply status and fault monitoring
- Meets DOE6 and CoC v5 2016 Average Efficiency requirements with at least 2.0% pass margin
  - 5 V Output: 91.51% at 115 VAC (6.51% margin); 91.30% at 230 VAC (6.3% margin)
  - 9 V Output: 92.20% at 115 VAC (3.35% margin); 92.83% at 230 VAC (3.98% margin)
  - 12 V Output: 92.32% at 115 VAC (3.32% margin); 93.27% at 230 VAC (4.27% margin)
  - 15 V Output: 92.08% at 115 VAC (3.08% margin); 93.19% at 230 VAC (4.19% margin)
  - 20 V Output: 91.99% at 115 VAC (2.99% margin); 93.35% at 230 VAC (4.35% margin)
- Meets CoC v5 2016 10% Load Efficiency requirements with high margin (>9.5%) for all PDOs
- <50 mW no-load input power at 230 VAC
- Meets CISPR22 / EN55022 Class B conducted EMI with at least 6 dB margin
- High power density: 16.1 W / inch^3 without enclosure (3.42” x 2.04” x 0.89” form factor)
- Low component count: 124 total

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www.power.com

Table of Contents

Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a 100 W USB PD 3.0 power supply using InnoSwitch4-Pro INN4375F-H341 and ClampZero CPZ1075M for the flyback stage, HiperPFS-5 PFS5274F for the PFC front-end, and Injoinic IP2726S for the USB PD controller. The USB PD source capabilities of the power supply are listed below.

- PDO1: 5 V / 5 A (Fixed Supply)
- PDO2: 9 V / 5 A (Fixed Supply)
- PDO3: 12 V / 5 A (Fixed Supply)
- PDO4: 15 V / 5 A (Fixed Supply)
- PDO5: 20 V / 5 A (Fixed Supply)
- PDO6: 3.3 V – 21 V / 5 A (Programmable Power Supply, 100 W power-limited)

This design shows the high power density and efficiency that is possible due to the high level of integration of the HiperPFS-5 and InnoSwitch4-Pro controllers providing exceptional performance.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics specifications, and performance data.

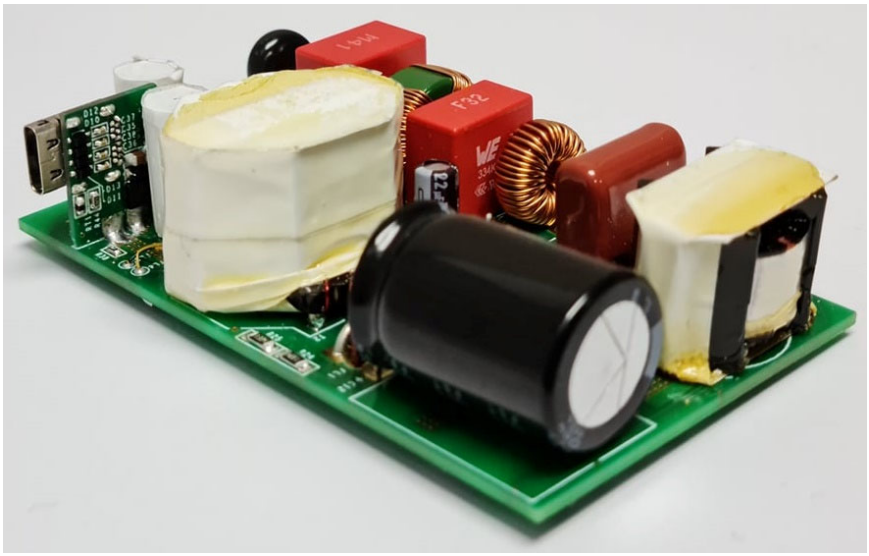


Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

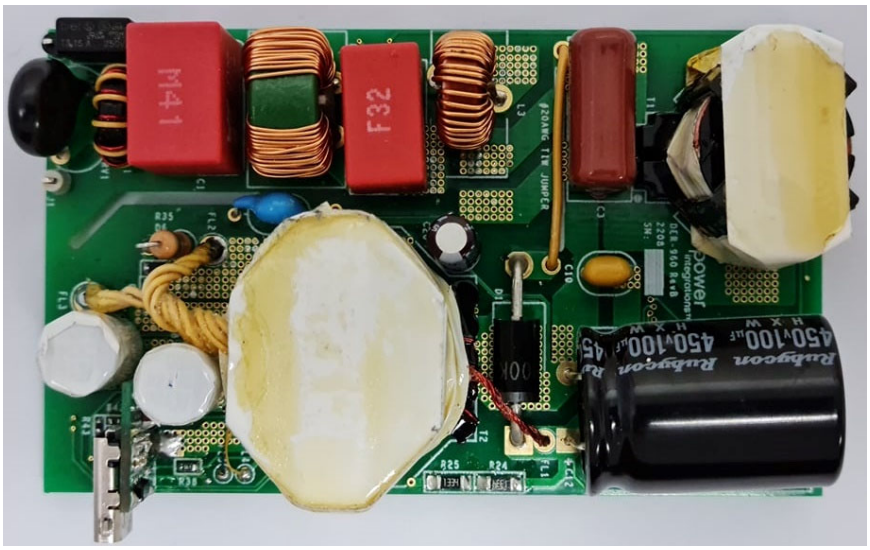


Figure 2 – Populated Circuit Board Photograph - Top.

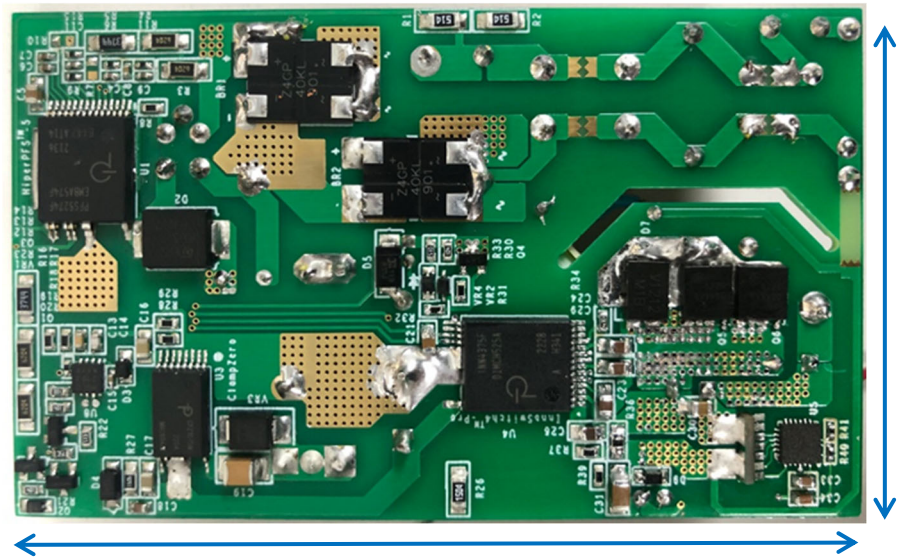


Figure 3 – Populated Circuit Board Photograph - Bottom.

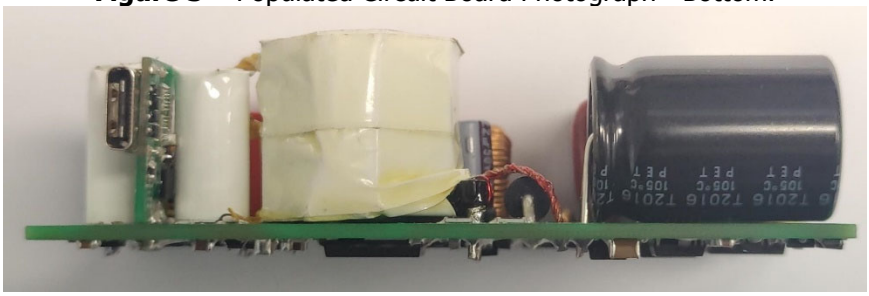


Figure 4 – Populated Circuit Board Photograph - Side.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Input Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Input Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power				48	mW	Measured at 230 VAC
USB PD 3.0 Output: Fixed Supply PDOs						
5 V / 5 A Fixed Supply PDO1						
Output Voltage	$V_{OUT(5\ V)}$		5.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(5\ V)}$			100	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(5\ V)}$			5.0	A	See Note C.
Average Efficiency	$\eta_{(5\ V)}$	91.0			%	Average Efficiency at 115 VAC with VOUT Measured on the Board.
Continuous Output Power	$P_{OUT(5\ V)}$			25	W	
9 V / 5 A Fixed Supply PDO2						
Output Voltage	$V_{OUT(9\ V)}$		9.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(9\ V)}$			90	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(9\ V)}$			5.0	A	See Note C.
Average Efficiency	$\eta_{(9\ V)}$	91.7			%	Average Efficiency at 115 VAC with VOUT Measured on the Board.
Continuous Output Power	$P_{OUT(9\ V)}$			45	W	
12 V / 5 A Fixed Supply PDO3						
Output Voltage	$V_{OUT(12\ V)}$		12.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(12\ V)}$			65	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(12\ V)}$			5.0	A	See Note C.
Average Efficiency	$\eta_{(12\ V)}$	91.8			%	Average Efficiency at 115 VAC with VOUT Measured on the Board.
Continuous Output Power	$P_{OUT(12\ V)}$			60	W	
15 V / 5 A Fixed Supply PDO4						
Output Voltage	$V_{OUT(15\ V)}$		15.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(15\ V)}$			55	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(15\ V)}$			5.0	A	See Note C.
Average Efficiency	$\eta_{(15\ V)}$	91.5			%	Average Efficiency at 115 VAC with VOUT Measured on the Board.
Continuous Output Power	$P_{OUT(15\ V)}$			75	W	
20 V / 5 A Fixed Supply PDO5						
Output Voltage	$V_{OUT(20\ V)}$		20.0		V	See Note A.
Output Voltage Ripple	$V_{RIPPLE(20\ V)}$			50	mV	Measured at End of 100 mΩ Cable. See Note B.
Output Current	$I_{OUT(20\ V)}$			5.0	A	See Note C.
Average Efficiency	$\eta_{(20\ V)}$	91.5			%	Average Efficiency at 115 VAC with VOUT Measured on the Board.
Continuous Output Power	$P_{OUT(20\ V)}$			100	W	

Description	Symbol	Min	Typ	Max	Units	Comment
USB PD 3.0 Output: Programmable Power Supply APDOs						
3.3 V – 21 V / 5 A PPS APDO6						
Programmable Output Voltage Range	$V_{OUT(PDO6)}$	3.3		21	V	APDO Minimum and Maximum Voltage. See Note A.
Programmable Output Current Limit Range	$I_{OUT(PDO6)}$	1.0		5.0	A	See Note D.
PPS Voltage Step	$V_{STEP(PDO6)}$		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	$I_{STEP(PDO6)}$		50		mA	PPS Current Step (USB PD 3.0).
Continuous Output Power	$P_{OUT(PDO6)}$			100	W	PPS Power Limited bit = 1 (USB PD 3.0). See Note E.
Conducted EMI Margin		6			dB	Meets CISPR22B / EN55022B
Ambient Temperature	T_{AMB}	0		45	ºC	Open Frame, Sea Level.

Note A: Output Voltage Regulation compliant with USB PD 3.0 Specifications.
B: Output Voltage Ripple measured at the end of 100 mΩ cable with the probe having decoupling capacitors 47 uF electrolytic and 100 nF ceramic in parallel.
C: Maximum Operating Current for the Fixed Supply PDO. Output Over Current Protection Threshold nominally set at 250 mA above the Operating Current requested by the USB PD Sink.
D: Output Current Limit Accuracy is within ±150 mA for Operating Current between 1 A and 3 A, or ±5% for Operating Current > 3 A; compliant with USB PD 3.0 Specifications.
E: For PPS APDOs with Power Limited bit set to 1, whenever the USB PD Sink sends a valid Output Voltage and Current Limit request that exceeds 100 W, the power supply will provide the requested output voltage and an output current limit that matches 100 W maximum output power.

Note: To use this design for a charger/adapter with a different shape and form factor, the changes in the circuit board layout must be carefully evaluated to meet the target specifications for EMI, ESD, and Line Surge performance.

3 Schematic

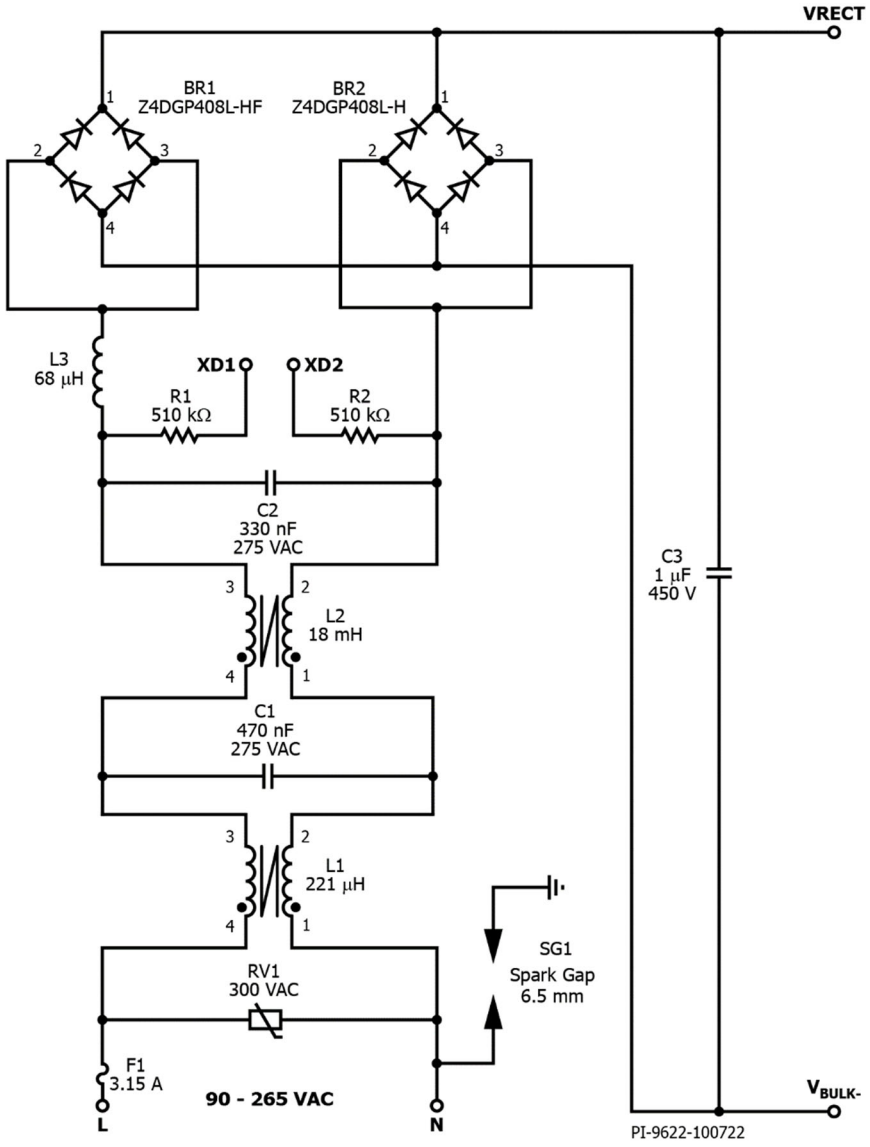


Figure 5 – DER-960 Rev B Schematic – Input Section.

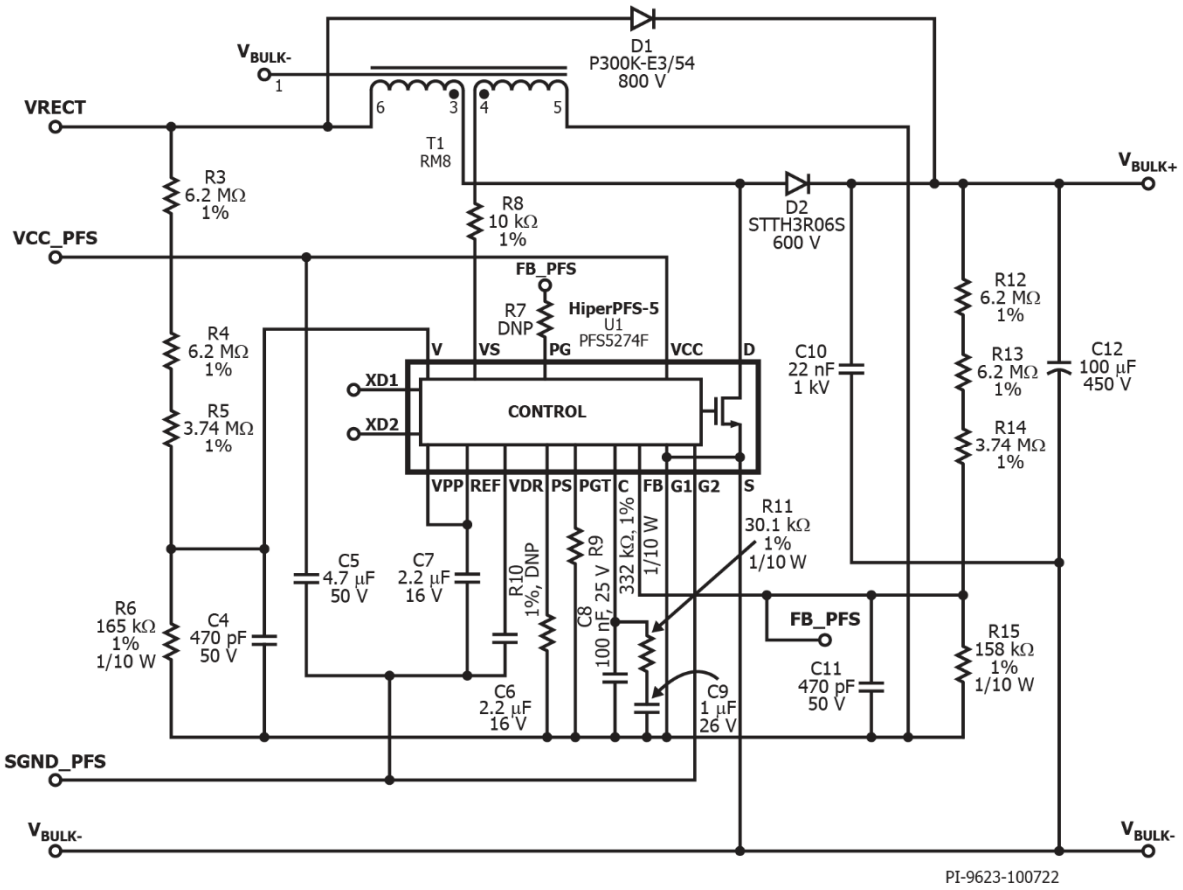


Figure 6 – DER-960 Rev B Schematic – PFC Section.

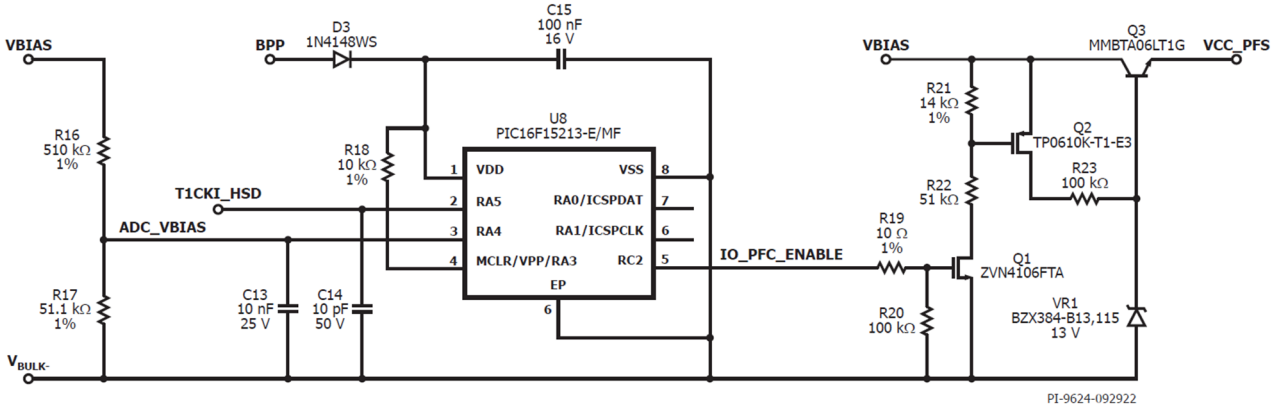


Figure 7 – DER-960 Rev B Schematic – PFC Bias Control Section.

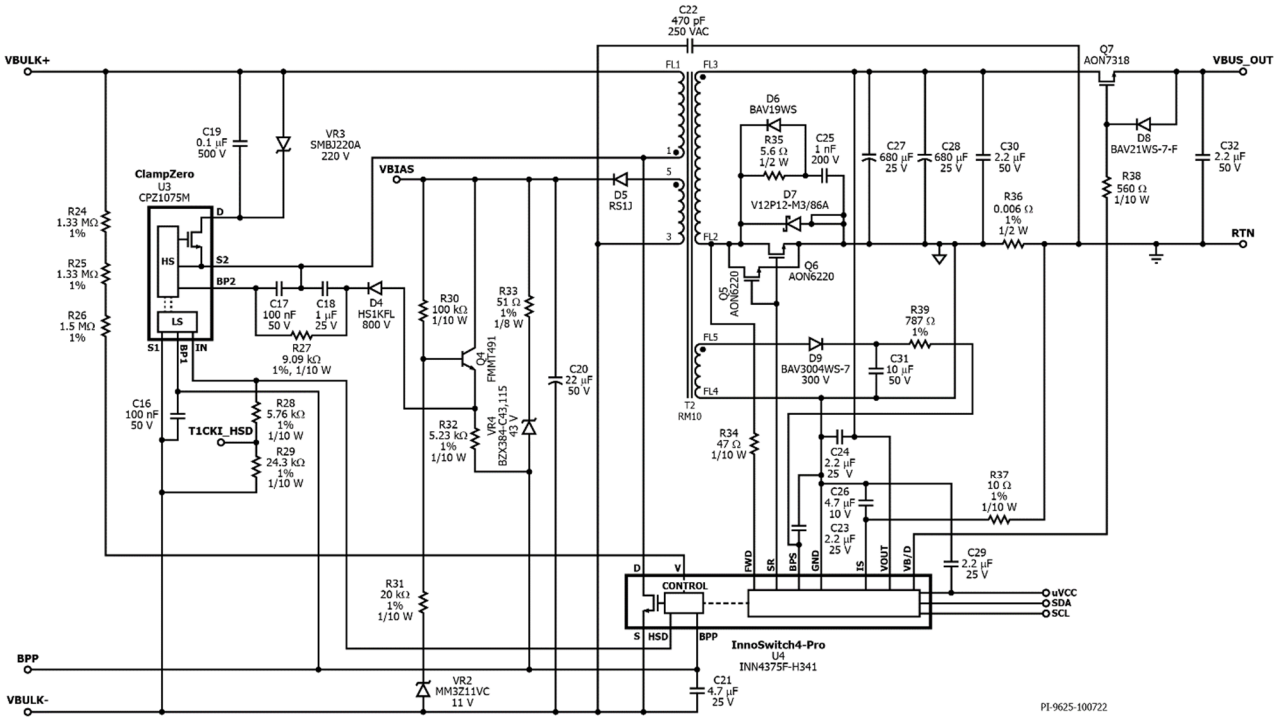


Figure 8 - DER-960 Rev B Schematic – Flyback Section.

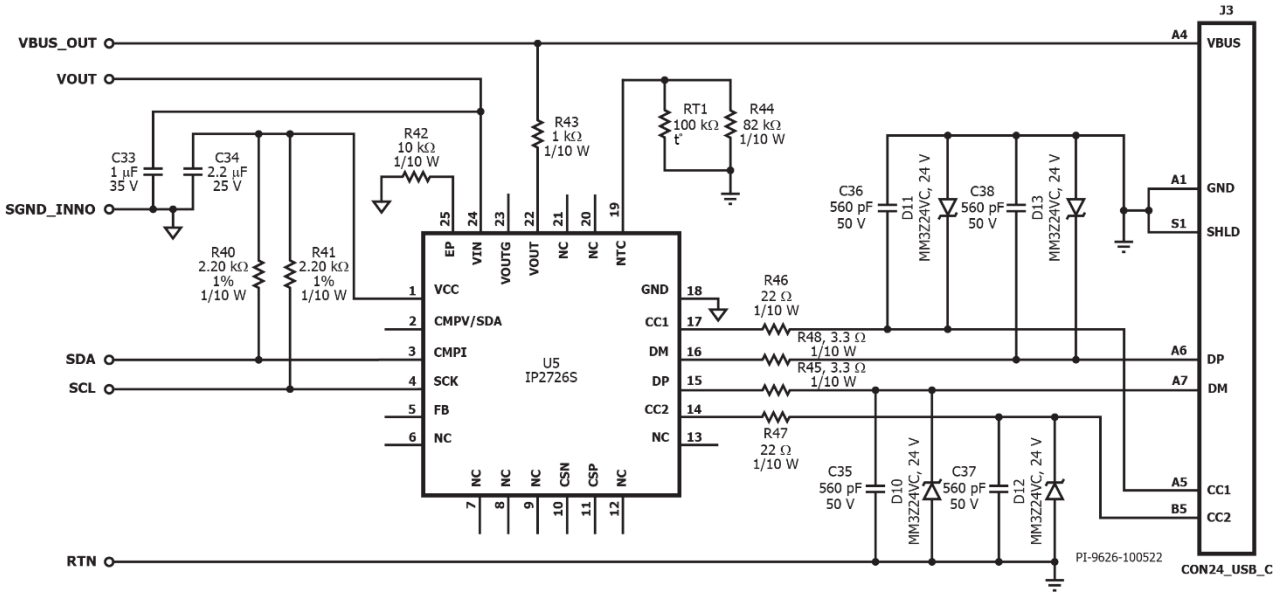


Figure 9 – DER-960 Rev B Schematic – USB PD Controller Section.

4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

The input fuse F1 isolates the circuit and provides protection from component failure. Metal oxide varistor RV1 offers protection during line surge events by effectively clamping the input voltage seen by the power supply. Common mode chokes L1 and L2, differential mode choke L3, along with capacitors C1, C2, and C3 provide common mode and differential mode noise filtering for EMI attenuation. Bridge rectifiers BR1 and BR2 rectify the AC line voltage to have a full-wave rectified DC.

The resistors R1 and R2 are connected to the integrated X-capacitor discharge pins in the HiperPFS-5 IC U1 to bring down the voltage across C1 and C2 to safe levels when the power supply is disconnected from the AC mains. HiperPFS-5 eliminates static losses in R1 and R2 by only connecting these components across the X-capacitors when AC input is removed.

4.2 *HiperPFS-5 PFS5274F PFC Boost Converter*

The PFC boost converter power stage consists of the HiperPFS-5 IC U1, boost inductor T1, ultrafast diode D2, and output filter capacitor C12. With an active PFC boost converter as a front-end stage of the power supply, a sinusoidal input current with low harmonic content is maintained while having a regulated DC voltage to the Flyback DC-DC converter stage of the power supply.

Diode D1 acts as a pre-charge diode, preventing a resonant build-up of output voltage during start-up by bypassing T1 while simultaneously charging C12.

Capacitor C10 provides a short, high-frequency return path from PFC output B+ to primary ground VBULK- for improved EMI performance and reduce voltage overshoot across the MOSFET drain-source inside U1 at each turn-off edge.

Valley switching is achieved by sensing the inductor voltage from an auxiliary winding in the PFC choke that is fed to U1 through resistor R8. Resistor R10 is used to program the power delivery of HiperPFS-5 IC, and R10 is left open in this design to deliver 100% of the nominal power. Resistor R9 is used to set the bulk voltage level in which the PG pin will be in a high-impedance state.

Capacitor C6 is used as a bypass capacitor to supply the driver section of U1. Capacitor C7 is used as an external bypass capacitor to supply the control circuitry of U1.

4.2.1 PFC Input Line Feed-Forward Sense Circuit

The rectified DC voltage at the PFC input is sensed by HiperPFS-5 IC U1 using resistors R3-R6. These resistors have large values to minimize power dissipation and standby power consumption and are selected to have a 1:100 scaling ratio. Capacitor C4 filters any switching noise present on the rectified DC bus into the VOLTAGE MONITOR pin.

4.2.2 PFC Output Feedback Circuit

Components C8, C9, and R11 are required for shaping the loop response of the feedback network. Output voltage divider network comprising of resistors R12-R15 are used to scale the output voltage and provide feedback to the IC. The resistor values are set to have a PFC output voltage of 400 V. Capacitor C11 filters noise coupled into the FEEDBACK pin.

4.2.3 PFC Enable / Disable Circuit

The HiperPFS-5 IC can operate with a wide range of bias power, from 6.5 to 35 VDC, supplied into the VCC pin. Capacitor C5 provides noise filtering to the VCC pin. Bringing the VCC pin voltage below the shutdown VCC voltage threshold will trigger an undervoltage lock-out protection and disable switching of the HiperPFS-5 device.

The PFC bias supply is derived from the flyback stage auxiliary output as shown previously in Figure 7. VBIAS, which is the filtered supply voltage using the flyback auxiliary winding, diode rectifier D5, and filter capacitor C20, is passed to a linear regulator formed by NPN BJT Q3, Zener VR1, P-channel MOSFET Q2, resistors R21, R22, and R23, and N-channel MOSFET Q1. When Q1 is in off-state, the linear regulator is disabled and effectively disabling the HiperPFS-5 device. Similarly, when Q1 is in on-state, the resistor divider R21 and R22 provides enough gate-source voltage across Q2 to turn it on and resulting into 12.4 V at the linear regulator output and effectively turning on the PFC stage. Q1 is driven by Microcontroller U8 through series gate resistor R19 and static gate-source pull-down resistor R20.

Microcontroller U8 is a low-cost, 8-pin MCU from Microchip (PIC16F15213) which ensures that the PFC stage is enabled when the power supply input power is 75 W or higher, considering tolerances in flyback transformer primary magnetizing inductance and primary switch current limit. At lower input power conditions, the PFC stage is disabled to improve system efficiency. Estimate of power supply input power is based on flyback switching frequency, obtained from InnoSwitch4-Pro HSD signal scaled down by resistors R28 and R29 and filtered with capacitor C14. Estimate of flyback output voltage is monitored by U8 with VBIAS, resistors R16 and R17, and filter capacitor C13. Operating at low output voltage results in U8 to also disable the PFC stage and enter deep sleep mode to minimize power consumption. U8 supply is taken from BPP of InnoSwitch4-Pro IC U4 through series diode D3 and then filtered with capacitor C15 across VDD and VSS pins.

4.3 *InnoSwitch4-Pro IC Primary*

One end of the Flyback transformer T2 primary winding is connected to the PFC stage output capacitor and the other end is connected to the drain terminal of the switch inside the InnoSwitch4-Pro IC (U4). Resistors R24-R26 provide input voltage sensing for protection in case of Flyback input under-voltage or over-voltage.

Capacitor C21 is chosen based on the desired current limit of the InnoSwitch4-Pro IC. The BYPASS pin of InnoSwitch4-Pro IC also supplies the ClampZero IC (U3) BP1 pin during

start-up. The primary clamp capacitor C19 limits the peak drain voltage of U4 at the instant of turn-off of the switch inside U4. The energy stored in the leakage inductance of transformer T2 will be transferred to capacitor C19. Part of the magnetizing energy will also get transferred to C19 depending on the capacitance value used. Zener diode VR3 is used as a fail-safe to protect the InnoSwitch4-Pro IC from excessive drain voltages during abnormal conditions applied to the power supply.

When the FluxLink signal is received from the secondary side, the InnoSwitch4-Pro IC (U4) generates an HSD signal to turn on the ClampZero device. When the ClampZero IC (U3) turns on, to achieve soft switching of the InnoSwitch4-Pro primary switch, clamp capacitor C19 starts to charge the leakage inductance of the transformer in the case of CCM operation, and both the leakage and the magnetizing inductance of the transformer in the case of DCM operation. A small delay is provided from the instant the high-side switch turns off to achieve zero voltage switching on the primary switch. This delay is either programmable by resistors R28 and R29 value at low-line input voltage, or a fixed 500ns delay at high-line input voltage. The transition between programmable delay and fixed delay is based on input line voltage information at the V pin of InnoSwitch4-Pro.

Capacitor C16 is used to provide local decoupling at the BP1 pin of IC U3. Capacitor C17 provides the decoupling for the BP2 pin. Diode D4 and capacitor C18 form a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R27 limits the current flowing into the BP2 pin.

The InnoSwitch4-Pro IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C21 when AC is first applied. During normal operation, the primary side block is powered from an auxiliary winding on the transformer T1. VBIAS, which is the filtered supply voltage using the auxiliary winding, diode rectifier D5, and filter capacitor C20, is used to power the InnoSwitch4-Pro IC (U4) primary-side and ClampZero IC (U3). A linear regulator comprising resistor R30, R31, BJT Q4, and Zener diode VR2 ensures sufficient current flows through R32 into the BPP pin of the InnoSwitch4-Pro IC such that the internal current source of U4 is not required to charge C21 to minimize power consumption during no-load condition and at normal operation.

Zener diode VR4 offers primary sensed output overvoltage protection. In a Flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR4 which then causes excess current to flow into the BPP pin of InnoSwitch4-Pro IC. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch4-Pro controller will latch off and prevent any further increase in output voltage. Resistor R33 limits the current injected to BPP pin when the output overvoltage protection is triggered.

4.4 *InnoSwitch4-Pro IC Secondary*

The secondary side of the InnoSwitch4-Pro IC provides output voltage, output current sensing, and gate drive to a FET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side synchronous rectifier FET (SR FET) Q5, Q6, and diode D7, and filtered by capacitors C27, C28, C30. High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced via RCD snubber R35, C25, and D6. Diode D6 minimizes the dissipation in resistor R35.

The gate of Q5 and Q6 is turned on by the secondary-side controller inside IC U4, based on the secondary winding voltage sensed via resistor R34 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectifier operation.

The secondary side of the IC U4 is self-powered from either the secondary winding forward voltage or the output voltage. However, to improve the system efficiency and reduce the secondary-side internal consumption, a secondary bias winding circuit was used. Bias winding voltage is rectified by diode D9 and filtered by capacitor C31. Resistor R39 limits the current flowing to the BPS pin of U4. Capacitor C23 connected to the BPS pin of IC U4 provides decoupling for the internal circuitry.

The secondary side of the InnoSwitch4-Pro can also provide a 3.6V supply for an external controller through the uVCC pin. Capacitor C29 is used to decouple its output.

The output current is sensed by monitoring the voltage drop across resistor R36. The current measurement is filtered with resistor R37 and capacitor C26, and then monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold up to approximately 32 mV configured by the USB PD controller via I2C interface is used to reduce the losses. Once the threshold is exceeded, the InnoSwitch4-Pro IC responds depending on its configuration to either maintain a fixed output current by using variable frequency and variable primary switch peak current limit control schemes to maintain a fixed output current or to shut down the power supply.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch4-Pro IC. Similar with current regulation, the output voltage is also compared to an internal voltage threshold that is set via the integrated secondary controller of the InnoSwitch4-Pro IC and the USB-PD controller IC, and output voltage regulation is achieved by variable

frequency and variable primary switch peak current limit control schemes. Capacitor C24 is used as decoupling capacitor for the VOUT pin.

4.5 *USB Type-C and PD Interface*

In this design, Injoinic IP2726S (U5) is the USB Type-C and PD controller. The IP2726S device is powered by the filtered flyback transformer output.

The IP2726S IC communicates with InnoSwitch4-Pro IC through the I2C interface using the SCL and SDA lines in which it sets several command registers, such as the CV, CC, VKP, OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch4-Pro IC, respectively. The status of the InnoSwitch4-Pro IC is read by the IP2726S IC from the telemetry registers also using the I2C interface. The USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which the Type-C plug is connected.

N-channel MOSFET Q7 functions as the bus switch which connects or disconnects the output of the Flyback converter from the USB Type-C receptacle. MOSFET Q7 is controlled by the VB/D pin on the InnoSwitch4-Pro IC. Diode D8 is connected across the Source and Gate terminals of Q7 and R38 is connected from the Gate of Q7 to the VB/D pin to provide a discharge path for the bus voltage when the Q7 is turned off. Capacitor C32 is used at the output for ESD protection and output voltage ripple reduction.

Capacitor C33 is used as a decoupling capacitor on VIN pin of U5 and capacitor C34 is used as decoupling capacitor on VCC pin of U5. Resistors R40 and R41 are used as pull-up resistors for SDA and SCL lines, respectively.

Resistors R45-R48, capacitors C35-C38, and Zener diodes D10-D13 are used to protect the DP, DM, CC1, and CC2 lines from ESD surge events. Thermistor RT1 and resistor R44 are used to sense USB Type-C connector temperature using NTC function of U5.

5 PCB Layout

Layers:	Two (2)
Board Material:	FR4
Main Board Thickness:	1.6 mm.
Daughterboard Thickness:	1 mm.
Copper Weight:	2 oz.

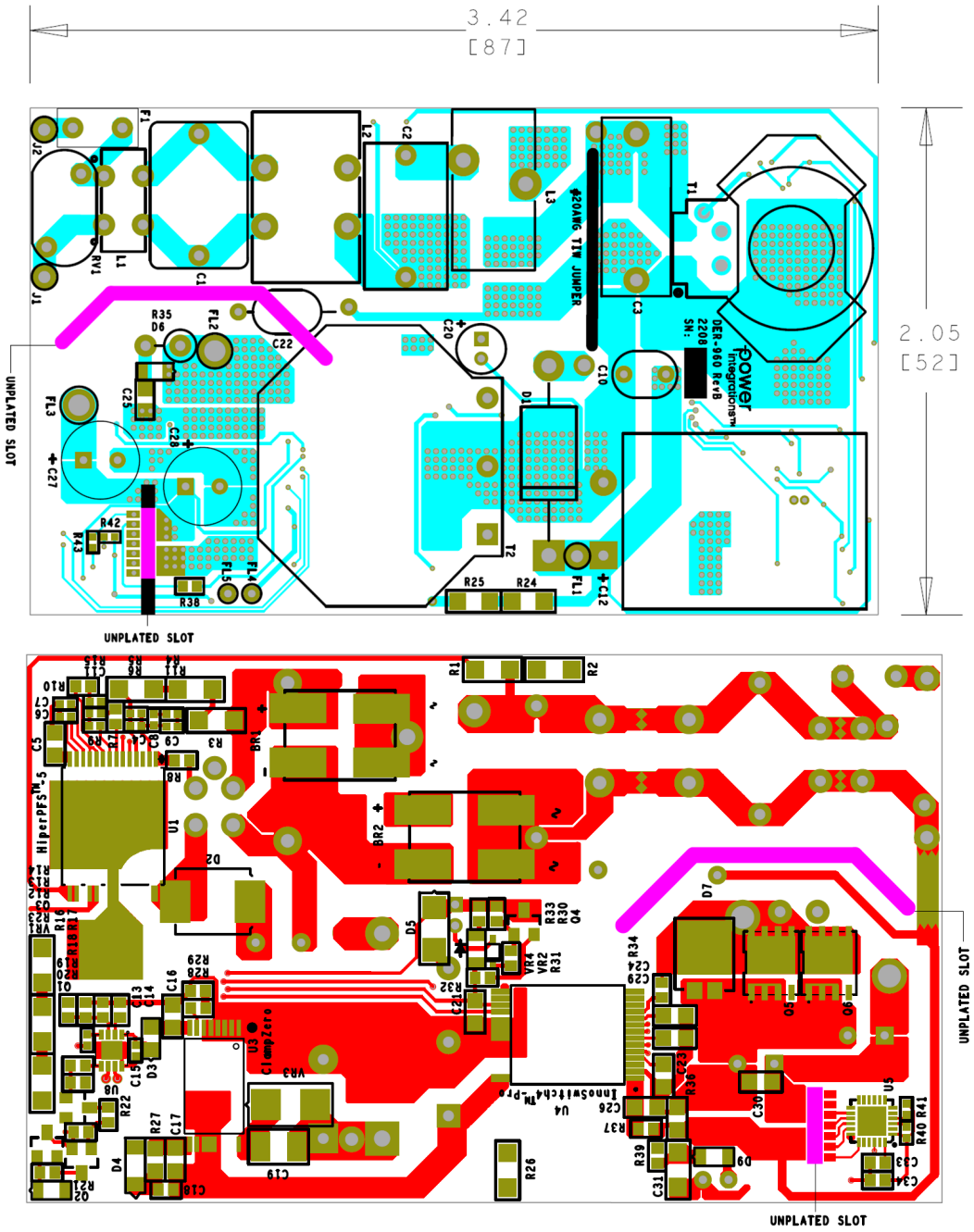


Figure 10 – DER-960 Rev B Main Board PCB Layout, Top and Bottom.

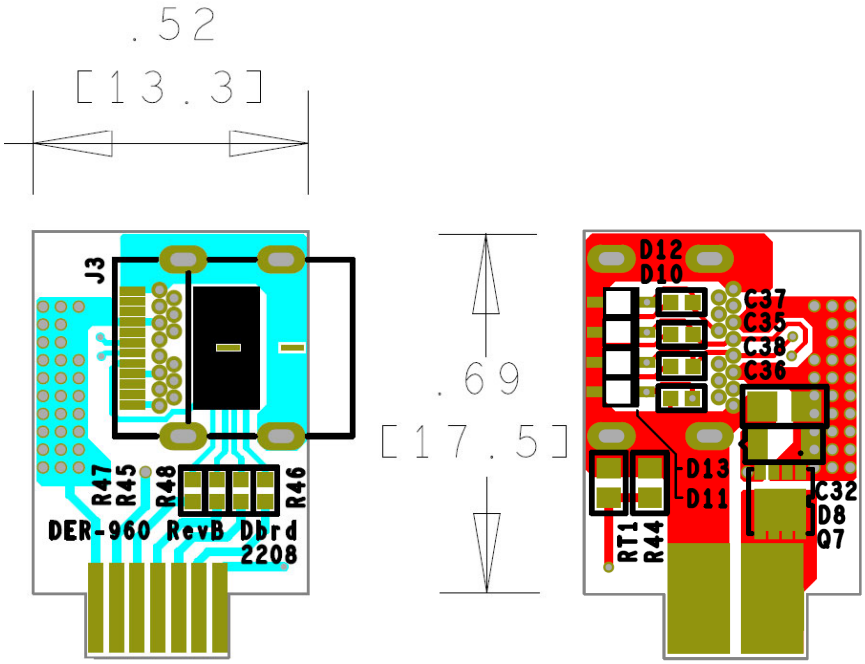


Figure 11 – DER-960 Rev B Daughterboard PCB Layout, Top and Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	BR1 BR2	RECT BRIDGE, GP, 800 V, 4 A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	FILM, 0.47 µF, 10%, 275 VAC, X2, RAD	890324024005	Würth
3	1	C2	330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00 mm x 8.50 mm	890324024003CS	Wurth
4	1	C3	1.0 µF, 450 V, Polyester Film	ECQ-E2W105KH	Panasonic
5	2	C4 C11	470 pF, ±5%, 50V, C0G, NP0, -55 °C ~ 125 °C, Low ESL, 0402	C0402C471J5GACTU	Kemet
6	1	C5	4.7 µF, 50 V, Ceramic, X5R, 0805	CL21A475KBQNNNE	Samsung
7	2	C6 C7	2.2 µF, ±10%, 16 V, Ceramic, X7R, -55°C ~ 85°C, 0402	GRM155R61C225KE44D	Murata
8	2	C8 C15	100 nF 16 V, Ceramic, X7R, 0402	L05B104KO5NNNC	Samsung
9	1	C9	1 µF 25 V, Ceramic, X5R, 0402	TMK105BJ105MV-F	Taiyo Yuden
10	1	C10	0.022 µF, ±10%, 1 kV, X7R, Radial, -55 °C ~ 125 °C, 0.217" L x 0.157" W (5.50 mm x 4.00 mm)	RDER73A223K3M1H03A	Murata
11	1	C12	100 uF, 450 V, Electrolytic, (18 x 25)	450HXW100MEFR18X25	Rubycon
12	1	C13	10 nF, 0.01 µF, ±10%, 25 V, Ceramic, X7R, General Purpose, -55 °C ~ 125 °C, 0603	CL10B103KA8NFNC	Samsung
13	1	C14	10 pF, ±0.25 pF, 50 V, Ceramic, C0G, NP0, 0603	CC0603CRNPO9BN100	Yageo
14	2	C16 C17	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
15	1	C18	1 µf, ±10%, 25 V, Ceramic, X7R, 0603	CGA3E1X7R1E105K080AE	TDK
16	1	C19	0.1 µF, ±10%, 500 V, Ceramic, X7R, 1210	C1210V104KCRACTU	Kemet
17	1	C20	22 µF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
18	1	C21	4.7 µF ±10%, 25 V, X7R, 0805,-55 °C ~ 125 °C	TMK212AB7475KG-T	Taiyo Yuden
19	1	C22	470 pF, ±10%, 250V AC, X1, Y1, Ceramic, B, Radial, Disc	DE1B3RA471KA4BN01F	Murata
20	3	C23 C24 C29	2.2 µF, ±10%, 25 V, X7R, r, -55 °C ~ 125 °C, 0805	CL21B225KAFVPNE	Samsung
21	1	C25	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
22	1	C26	4.7 µF, 10 V, Ceramic, X5R, 0805	C0805C475K8PACTU	Kemet
23	2	C27 C28	680 µF, ±20%, 25 V, Aluminum - Polymer Radial, Can 16 mOhm 2000 Hrs @ 105 °C (8 mm x 16 mm)	A750KW687M1EAAE016	KEMET
24	2	C30 C32	2.2 µF, ±10%, 50 V, Ceramic, X7R, 0805	UMK212BB7225KG-T	Taiyo Yuden
25	1	C31	10 µF, 10%, 50 V, Ceramic, X7R, -55 °C ~ 125 °C, 1206, 0.126" L x 0.063" W (3.20 mm x 1.60 mm)	CL31B106KBHNNNE	Samsung
26	1	C33	1 µF, ±10%,35 V, Ceramic, X7R, 0603	CGA3E1X7R1V105K080AE	TDK
27	1	C34	2.2 µF, ±10%, 25 V, Ceramic, X7R, 0603,-55 to 125 °C	GRM188Z71E225KE43D	Murata
28	4	C35-C38	560 pF ±10% 50 V Ceramic X7R 0402	CCCC0402KRX7R9BB561	Yageo
29	1	D1	Diode, Standard, 800 V, 3A, Through Hole, DO-201AD Diode, Standard, 800 V, 3A, Through Hole, DO-201AD, alternate part	P300K-E3/54 1N5407-E3/54	Vishay Vishay
30	1	D2	600 V, 3 A, SMC, DO-214AB	STTH3R06S	ST Micro
31	1	D3	Diode, GEN PURP, 75,V 150,MA, SOD323	1N4148WS-7-F	Diodes, Inc.
32	1	D4	800V, 1 A, High Efficiency Fast Recovery, SOD-123FL	HS1KFL	Taiwan Semi
33	1	D5	600 V, 1 A, Fast Recovery, 250 ns, SMA	RS1J-13-F	Diodes, Inc.
34	1	D6	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diode, Inc.
35	1	D7	Diode, Schottky, 120 V, 12 A, SMT, TO-277A (SMPC)	V12P12-M3/86A	Vishay
36	1	D8	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
37	1	D9	Diode, GEN PURP, FAST RECOVERY, 300 V, 225 mA, SOD323	BAV3004WS-7	Diodes, Inc.
38	4	D10-D13	Diode, ZENER, 24 V, 200 MW, SC-90, SOD-323F	MM3Z24VC	ON Semi
39	1	F1	3.15 A, 250 V, Slow, RST	RST 3.15-BULK	Belfuse
40	1	J3	Connector, "Certified", USB - C, USB 3.1, For 0.062" PCB Material!, Superspeed+, Receptacle Connector, 24 Position, SMT, RA, TH	632723300011	Wurth
41	1	L1	221 µH, Toroidal Common Mode Choke, custom, DER-960, wound on 32-00275-00 core	32-00431-00	Power Integrations

42	1	L2	Custom, CMC, 18 mH @ 10 kHz, Toroidal, 17.5 mm OD x 11.0 mm thick. 40 turns x 2, 0.40 mm wire 190 mOhm max	04291-T231	Sumida
43	1	L3	68 µH, Unshielded Toroidal Inductor, 2 A, 55 mOhm Max, Radial, Vertical (Open)	7447033	Wurth
44	1	Q1	MOSFET, N-Channel, 60 V, 200 mA (Ta,) 350 mW (Ta), SMT SOT-23-3, Micro3™/SOT-23, PG-SOT23, SOT-23F , TO-236-3, SC-59	ZVN4106FTA	Diodes, Inc.
45	1	Q2	60 V, 0.185 A, P-Channel, SOT 23-3	TP0610K-T1-E3	Vishay
46	1	Q3	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
47	1	Q4	NPN, 60 V 1000 mA, SOT-23	FMMT491TA	Zetex
48	2	Q5 Q6	MOSFET, N-CH, 100 V, 48 A (Tc), 113.5 W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
49	1	Q7	N-Channel 30 V 36.5 A (Ta), 50 A (Tc) 4.1 W (Ta), 39 W (Tc) Surface Mount 8-DFN-EP (3.3x3.3), 8DFN, 8-PowerVDFN	AON7318	Alpha & Omega Semi
50	2	R1 R2	RES, 510 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ514V	Panasonic
51	4	R3 R4 R12 R13	RES, 6.2 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm
52	2	R5 R14	RES, 3.74 M, 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay
53	1	R6	RES, 165.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1653X	Panasonic
54	1	R8	RES, 10.0 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
55	1	R9	RES, 332.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3323X	Panasonic
56	1	R11	RES, 30.1 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3012X	Panasonic
57	1	R15	RES, 158.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1583X	Panasonic
58	1	R16	RES, 510 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF5103V	Panasonic
59	1	R17	RES, 51.1 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF5112V	Panasonic
60	1	R18	RES, 10 kΩ, 5%, 1/16 W, Thick Film, 0402	RC0402JR-0710KL	Yageo
61	1	R19	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
62	3	R20 R23 R30	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
63	1	R21	RES, 14 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1402V	Panasonic
64	1	R22	RES, 51 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ513V	Panasonic
65	2	R24 R25	RES, 1.33 MΩ, 1%, 1/4 W, Thick Film, 1206	RC1206FR-071M33L	Yageo
66	1	R26	RES, 1.50 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
67	1	R27	RES, 9.09 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9091V	Panasonic
68	1	R28	RES, 5.76 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF5761V	Panasonic
69	1	R29	RES, 24.3 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2432V	Panasonic
70	1	R31	RES, 20 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2002V	Panasonic
71	1	R32	RES, 5.23 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF5231V	Panasonic
72	1	R33	RES, 51 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ510V	Panasonic
73	1	R34	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
74	1	R35	RES, 5.6 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-5R6	Yageo
75	1	R36	RES, 0.006 Ω, ±1%, 1/2W, 0805, Current Sense, Thick Film, ±300 ppm/°C,-55 °C ~ 155 °C	ERJ-6LWFR006V	Panasonic
76	1	R37	RES, 10 Ω, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
77	1	R38	RES, 560 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ561V	Panasonic
78	1	R39	RES, 787 Ω, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF7870V	Panasonic
79	2	R40 R41	RES, 2.20 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2201X	Panasonic
80	1	R42	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ103X	Panasonic
81	1	R43	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ102X	Panasonic
82	1	R44	RES, 82 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ823V	Panasonic
83	2	R45 R48	RES, 3.3 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ3R3X	Panasonic
84	2	R46 R47	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ220X	Panasonic
85	1	RT1	NTC Thermistor, 100 kΩ, 1%,4250K, 0603	NCU18WF104F60RB	Murata
86	1	RV1	300 Vac, 60 J, 10 mm, RADIAL	ERZ-V10D471	Panasonic
87	1	T1	Custom, DER-960 PFC Inductor Bobbin, RM8, Lp = 276 mH. Vertical, 6 pins		Power Integrations

88	1	T2	Custom, DER-960 Transformer Bobbin, RM10, Lp = 486 mH. Vertical, 5 pins		Power Integrations
89	1	U1	HiperPFS-5, 115 W, Non self-biasing, InSOP-T28F	PFS5274F	Power Integrations
90	1	U8	IC, PIC series Microcontroller IC, 8-Bit, 32MHz, 3.5KB (2K x 14) FLASH, 8-DFN (3x3)	PIC16F15213-E/MF	Microchip
91	1	U3	ClampZero, MinSOP-16	CPZ1075M	Power Integrations
92	1	U4	InnoSwitch4-Pro, InSOP-T28D	INN4375F-H341	Power Integrations
93	1	U5	IC, Fast Charging Physical Layer IC for USB Interfaces	IP2726S	INJOINIC
94	1	VR1	13 V, 2%, 300 mW, SOD-323	BZX384-B13,115	NXP Semi
95	1	VR2	11 V, ±5%, 200 mW, SOD-323	MM3Z11VC	ON Semi
96	1	VR3	TVS DIODE, 220 VWM, 356 VC, SMB	SMBJ220A	Bourns
97	1	VR4	43 V, ±5% , 300 mW, SOD323	BZX384-C43,115	Nexperia

Note: Although there are provisions for including R7 and R10 in the layout, these parts are not needed and hence not assembled.

Total component count: 124

7 Common Mode Choke Specifications (L1)

7.1 *Electrical Diagram*

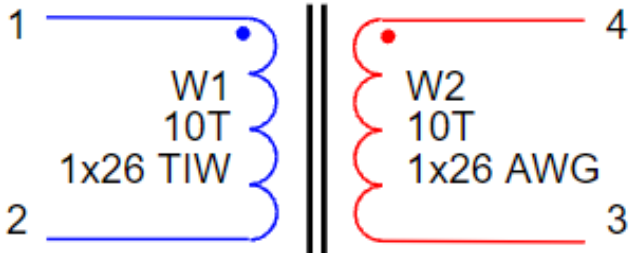


Figure 12 – Inductor Electrical Diagram.

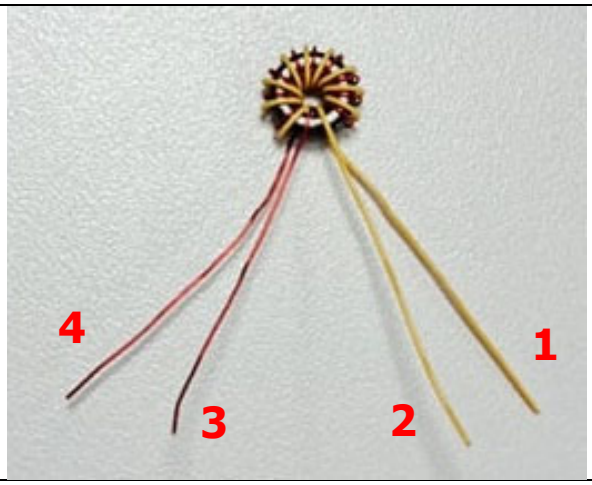
7.2 *Electrical Specifications*

Inductance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open. LCR meter L_S measurement, 100 kHz switching frequency, 1.0 V test level.	221 µH ±30%
DC Resistance	Across pin 1 to pin 2 (or pin 4 to pin 3) with the other winding open.	45 mΩ (Max.)

7.3 *Material List*

Item	Description
[1]	Core, FERRITE INDUCTOR TOROID .415" OD, 9.53 mm O.D. x 4.75 mm I.D. x 3.18 mm L. PI#: 32-00275-00.
[2]	Magnet Wire: #26 AWG, Triple Insulated Wire.
[3]	Magnet Wire: #26 AWG, Double Coated.
[4]	Varnish: Dolph BC-359.

7.4 *Winding Instructions*



Start as pin 1 for Item [2] and pin 4 for Item [3].

Wind together 10 turns to core Item [1].

Mark end of Item [2] as pin 2 and end of Item [3] as pin 3.

Cut the wires with practically short length remaining (~2 inch each) such the CMC can be easily populated into the PCB.

Varnish the CMC using Item [4].

Cut excess wire when soldering into the PCB.

8 PFC Inductor Specification (T1)

8.1 *Electrical Diagram*

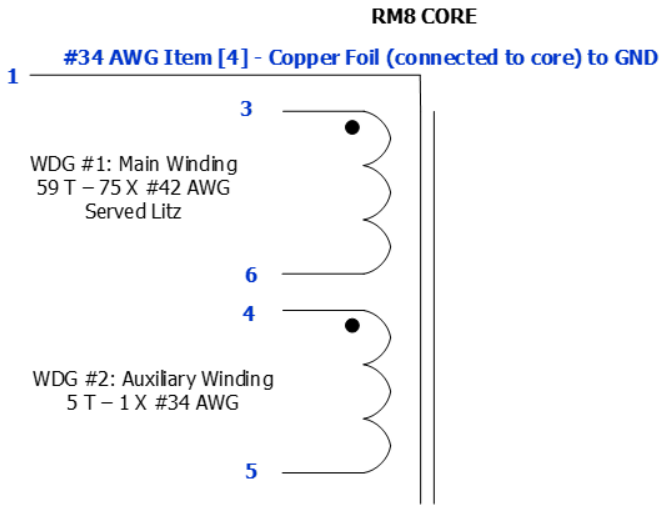


Figure 13 – PFC Inductor Electrical Diagram.

8.2 *Electrical Specifications*

Inductance	Measured across pin 3 to pin 6. LCR meter L_S measurement, 100 kHz switching frequency, 1.0 V test level.	276 µH ±5%

8.3 *Inductor Build Diagram*

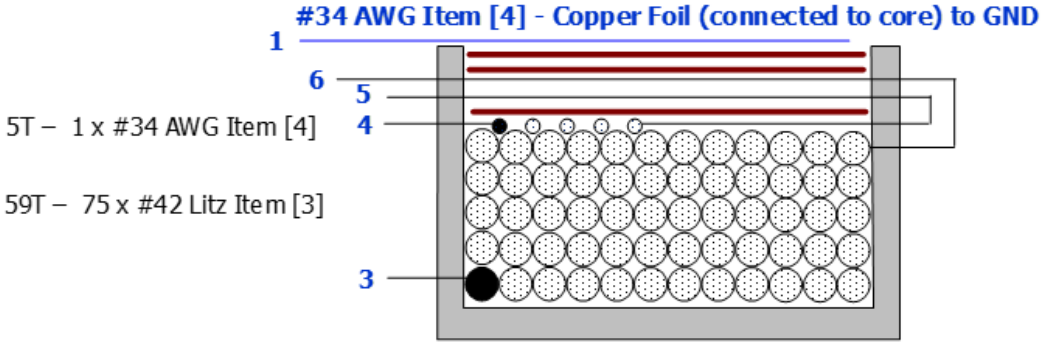
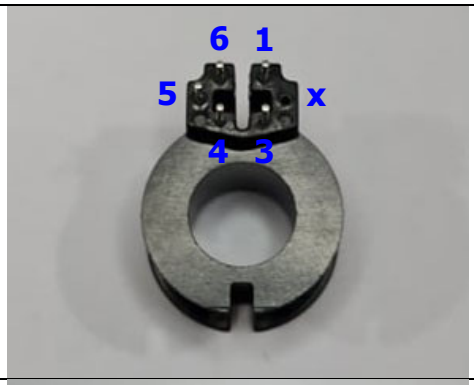
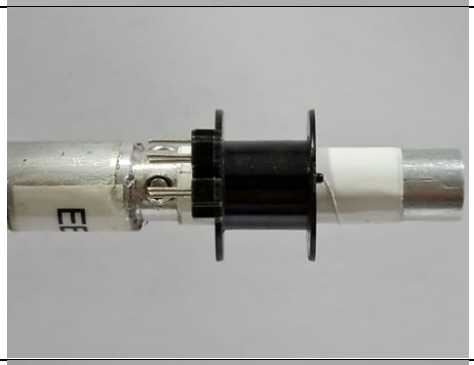
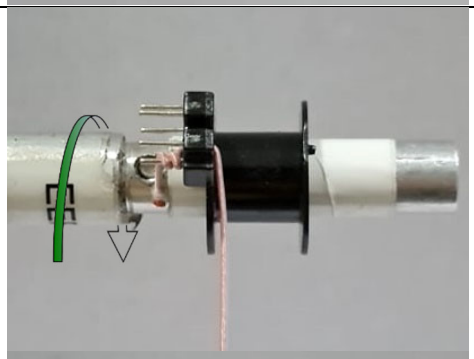
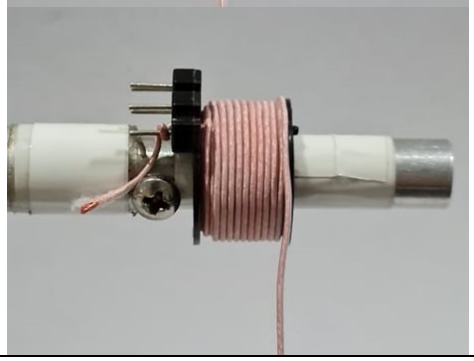


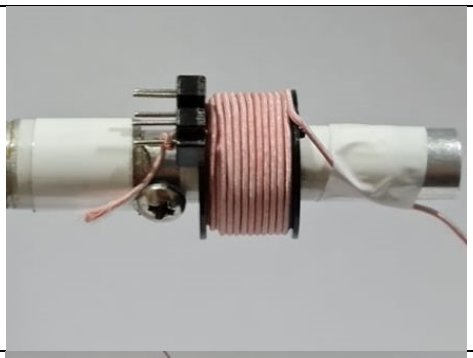
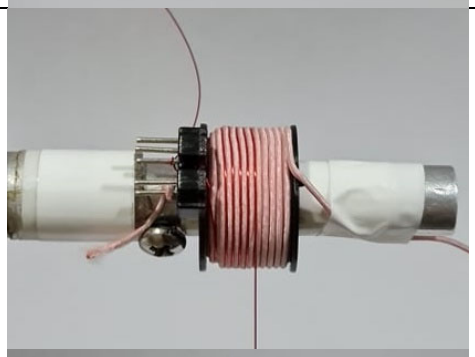
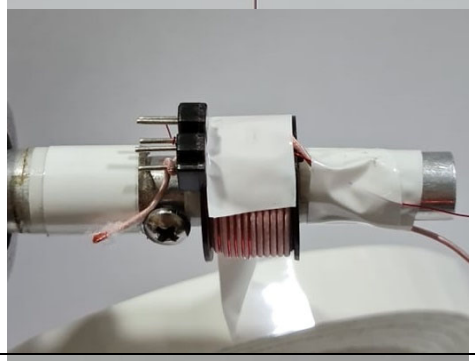
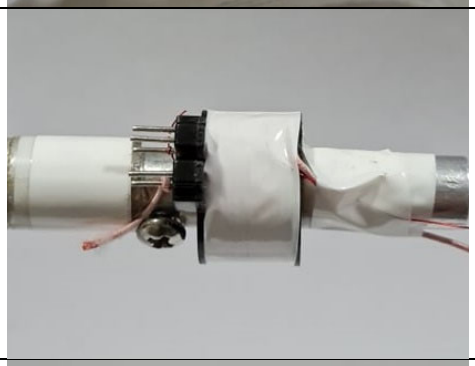
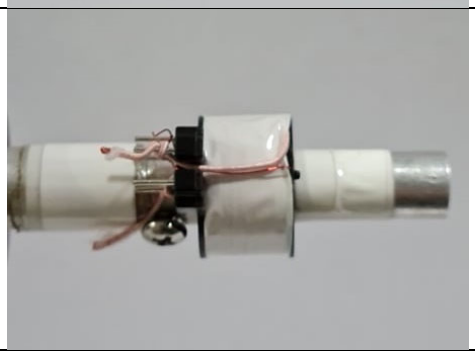
Figure 14 – Inductor Build Diagram.

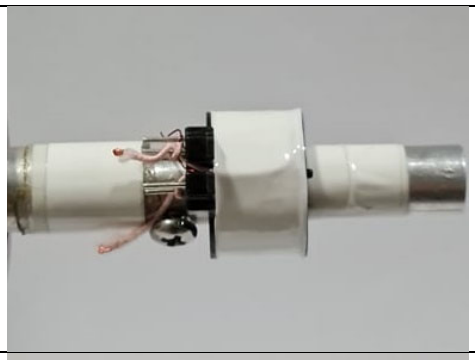
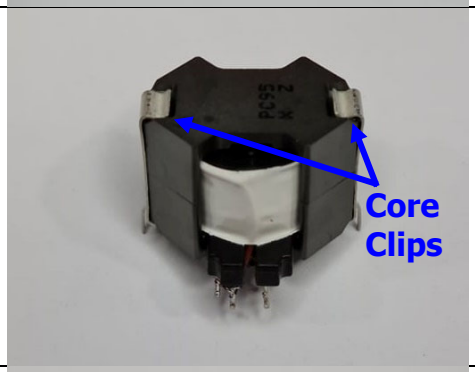
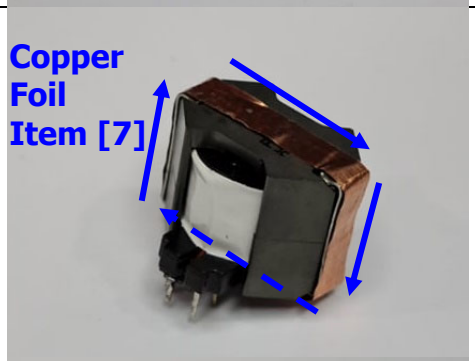
8.4 *Material List*

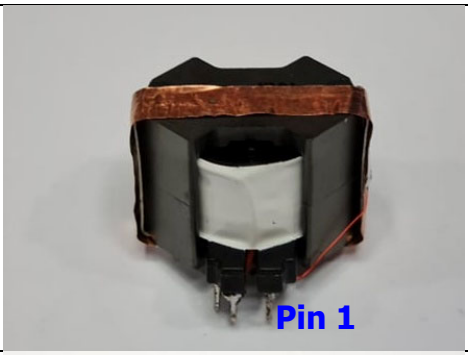
Item	Description
[1]	Core: TDK Core: RM8 PC95
[2]	Bobbin: RM8, 6 pins (6/0). PI #: 25-01147-00
[3]	Litz Wire: 75 #42 AWG Single Coated Solderable, Served.
[4]	Magnet Wire: 1 x #34 AWG, Double Coated.
[5]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 10 mm Width.
[6]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 13 mm Width.
[7]	Foil, Copper. 5 mm Width.
[8]	RM8 Core Clip.
[9]	Varnish: Dolph BC-359, or equivalent.

8.5 *Winding Instructions*

	Assign Pins 1, 3, 4, 5, and 6. Cut unused Pin 2.
	Position the bobbin on the mandrel such that the pin side of the bobbin is on the left side. Rotation of the mandrel is clock-wise.
 	Start at Pin 3, wind 59 turns of litz wire Item [3]. Wind going from left to right in the first layer, then right to left the next layer, and continue until 59 turns is completed within 5 layers.

	At the end of last turn, exit the wire to the right and leave ~2″ floating.
 	Use wire Item [4], start at Pin 4, and wind 5 turns from left to right. Ensure to wind it between the grooves of the Main Winding. Exit the wire to the right and leave ~2″ floating.
	Apply 1 layer of tape Item [5].
	Bring the 2 wires back to the left and terminate them to their respective pins: Terminate Main Winding (WDG #1) to Pin 6. Terminate Auxiliary Winding (WDG #2) to Pin 5.

		Apply 2 layers of tape Item [5].
		Solder the wires to their respective bobbin pins (Pin 3, 4, 5, and 6). Add gap to the middle leg of core Item [1] to get 276 µH ±5% inductance. Use RM8 core clips Item [8] to fix the 2 cores into the bobbin. Cut the 2 terminals of the clips.
	 	Wrap 1 turn of copper foil Item [7] around the core, and solder wire Item [4] onto the copper foil on the right side. Terminate and solder it to Pin 1.

		
		Secure core halves by wrapping 2 layers of tape Item [6] along the inductor bottom, sides, and top. Ensure inductance is still 276 μH ±5%. Varnish with Item [9] to complete the inductor.

9 Transformer Specification (T2)

9.1 *Electrical Diagram*

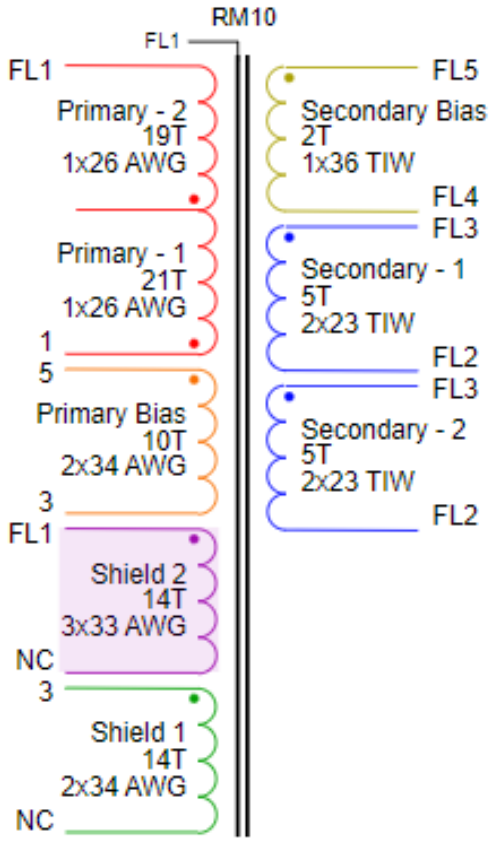


Figure 15 – Transformer Electrical Diagram.

9.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Across pin 1 to FL1, with all other windings open LCR meter Ls measurement, 100 kHz, 1.0 V test level	486 µH ±5%
Primary Leakage Inductance	Across pin 1 to FL1, with FL2 and FL3 shorted LCR meter Ls measurement, 100 kHz, 1.0 V test level	7.3 µH ±0.3 µH
Resonant Frequency	Across pin 1 to FL1, with all other windings open	1,200 kHz (Min.)
Electrical Strength (Primary to Secondary)	Across shorted primary windings (pins 1, FL1, 3, 5) to shorted secondary windings (FL2, FL3, FL4, FL5)	3000 VAC, 200 V / s ramp rate, 60 s soak

9.3 *Transformer Build Diagram*

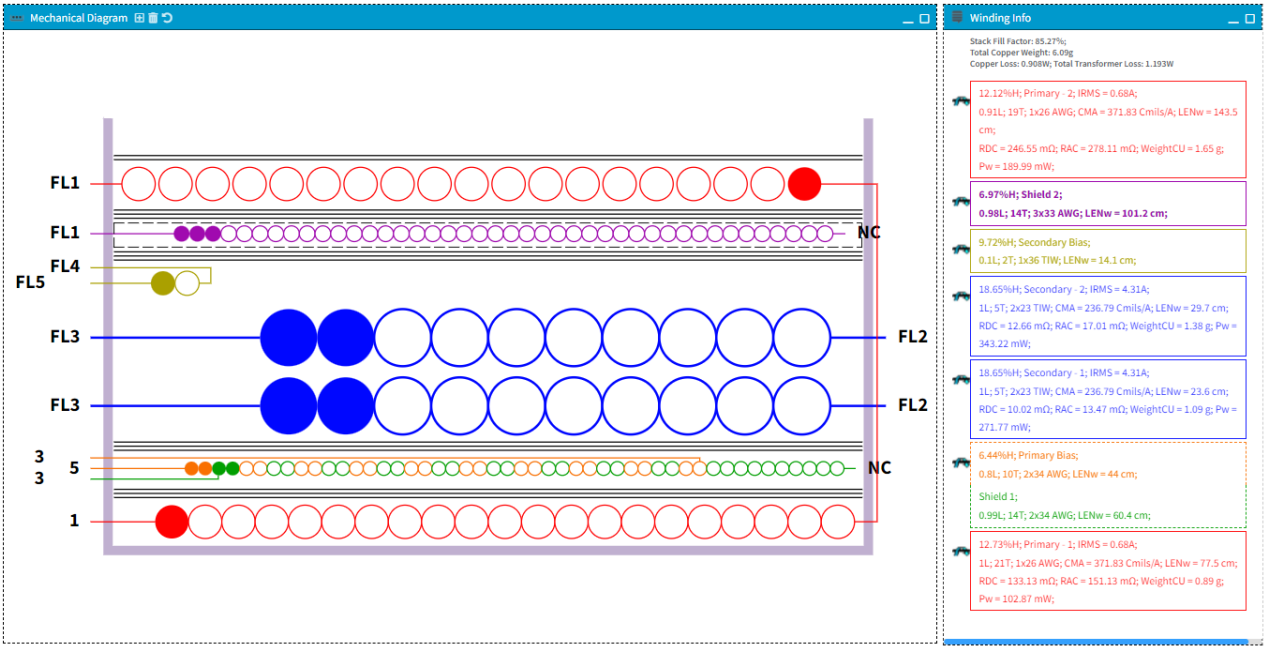
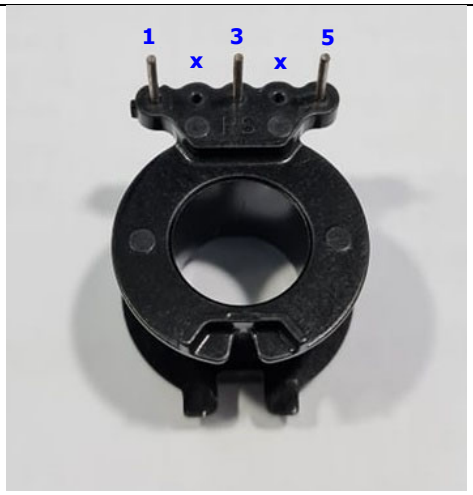
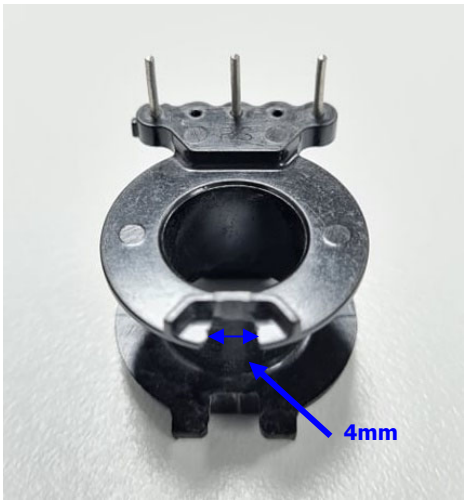
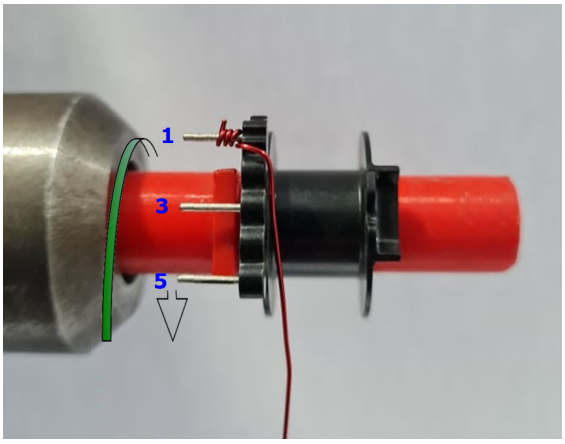


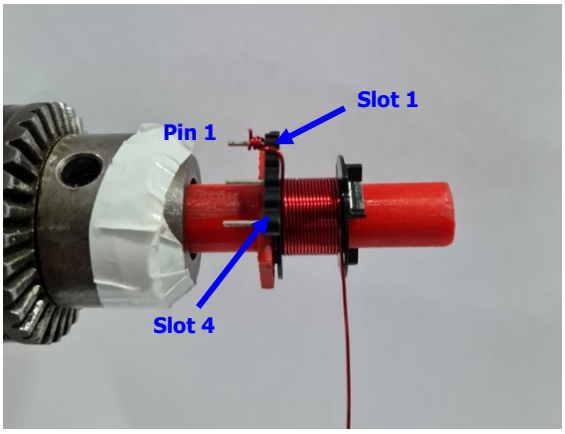
Figure 16 – Transformer Build Diagram.

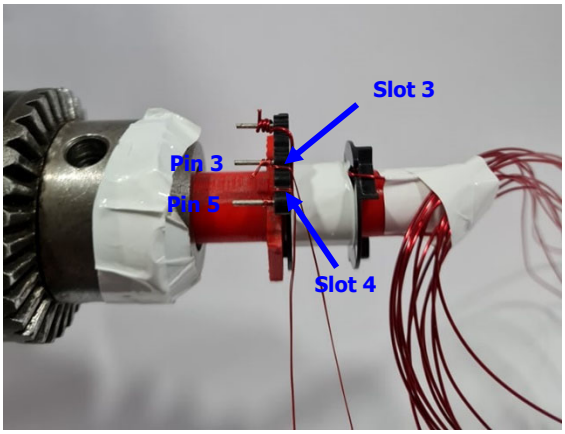
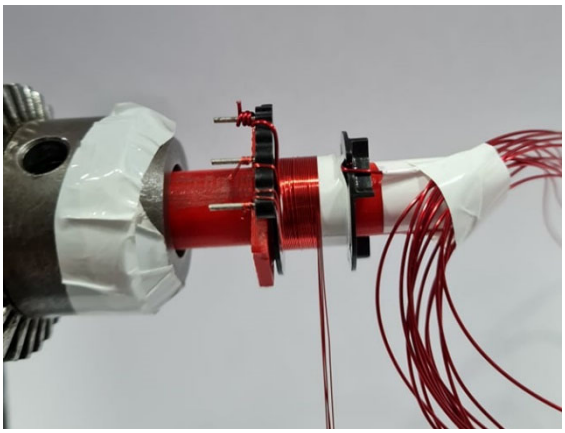
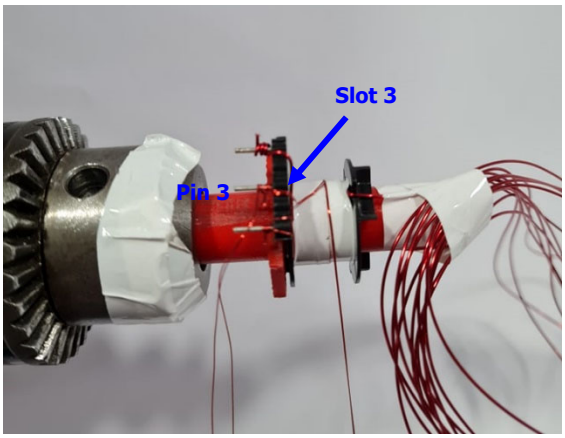
9.4 *Material List*

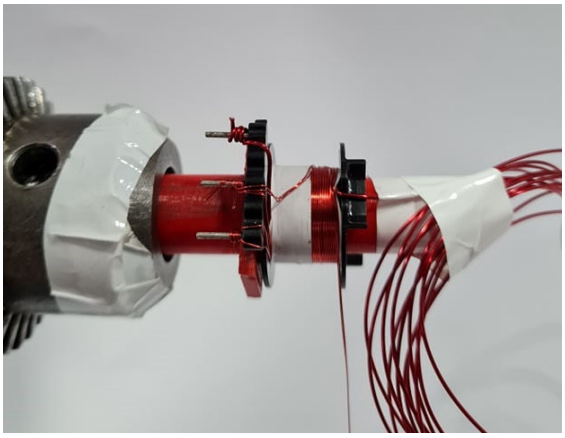
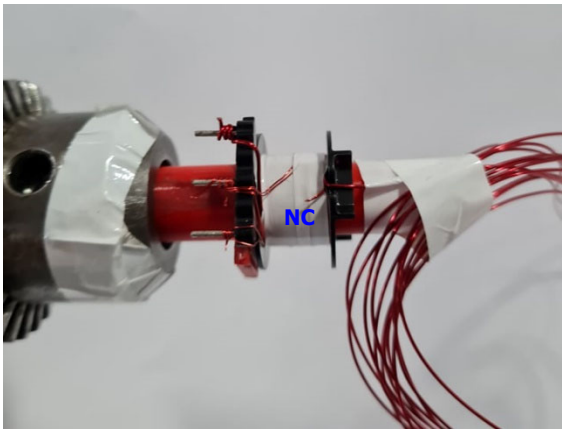
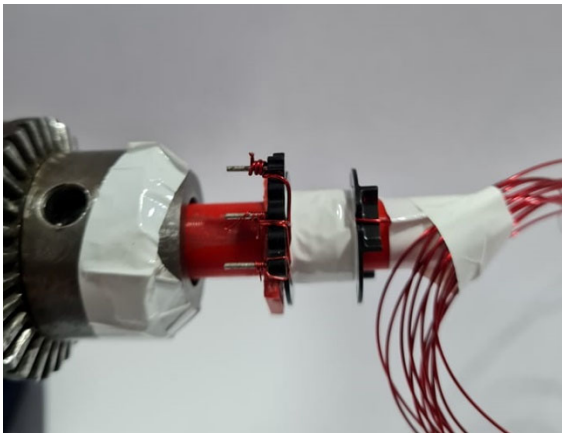
Item	Description
[1]	Core: RM10. Material: PC95 or equivalent
[2]	Bobbin: RM10 vertical 5 pins (5/0). P-1031. PI #: 25-00921-00.
[3]	Magnet Wire: #26 AWG, Double Coated.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #33 AWG, Double Coated.
[6]	Magnet Wire: #23 AWG, Triple Insulated Wire.
[7]	Magnet Wire: #36 AWG, Triple Insulated Wire.
[8]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 3 mm Width.
[9]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 5 mm Width.
[10]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 8 mm Width.
[11]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 10.5 mm Width.
[12]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 11.2 mm Width.
[13]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 21.5 mm Width.
[14]	Foil: Copper Foil, 5 mm Width.
[15]	RM10 Core Clip
[16]	Varnish: Dolph BC-359.

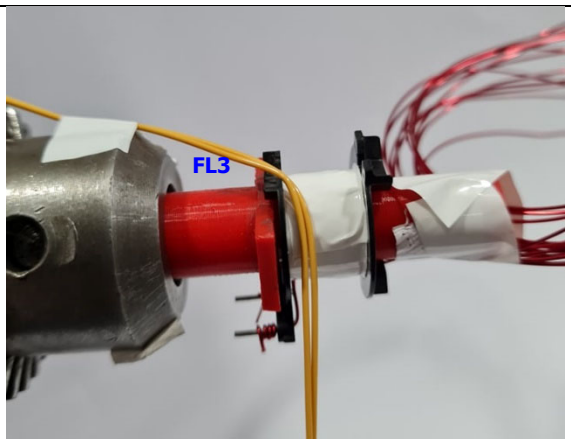
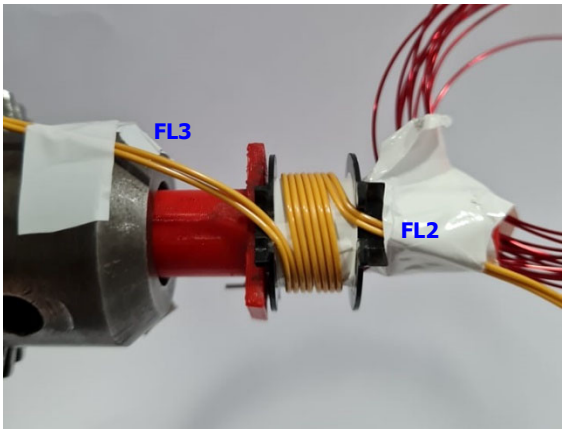
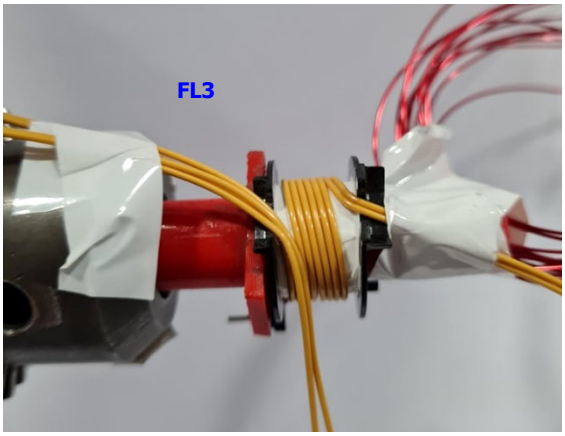
9.5 *Winding Instructions*

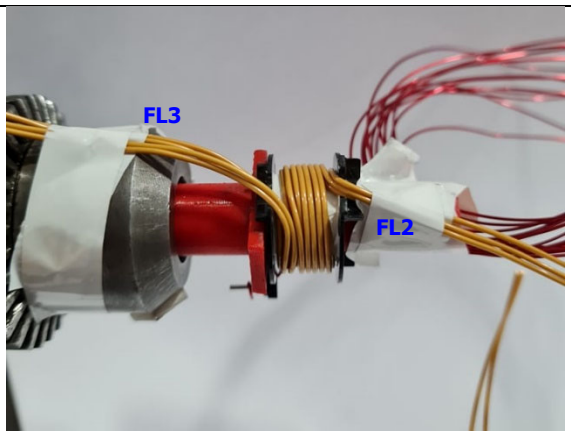
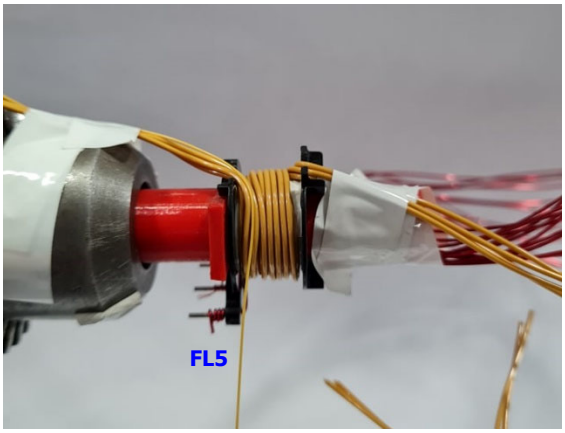
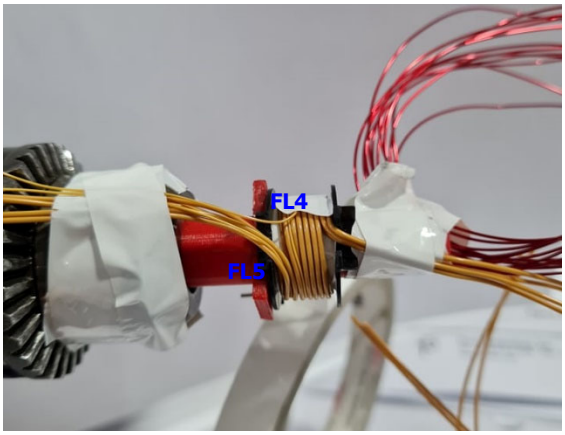
Bobbin and Winding Preparation		Start by cutting pins 2 and 4 of the bobbin Item [2].
		Widen the slot on the flange of the secondary side of the bobbin's bottom side to ~4 mm.
		Place the bobbin on the mandrel with pin side of the bobbin on the left side. Winding direction is clock-wise.

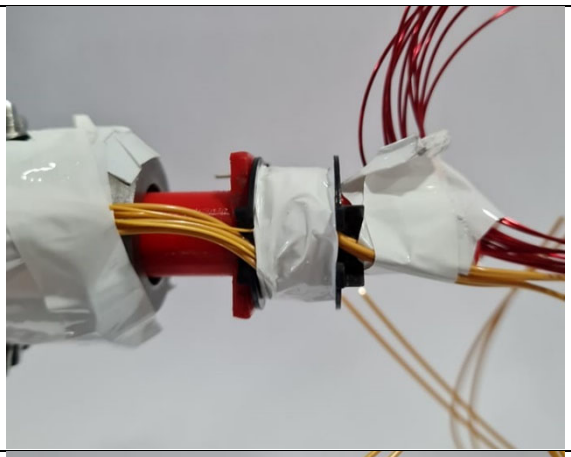
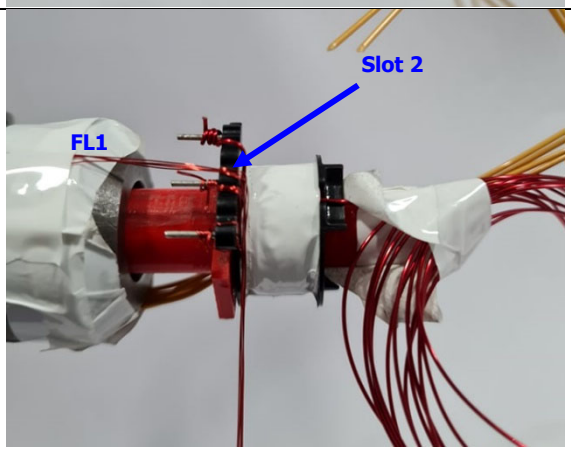
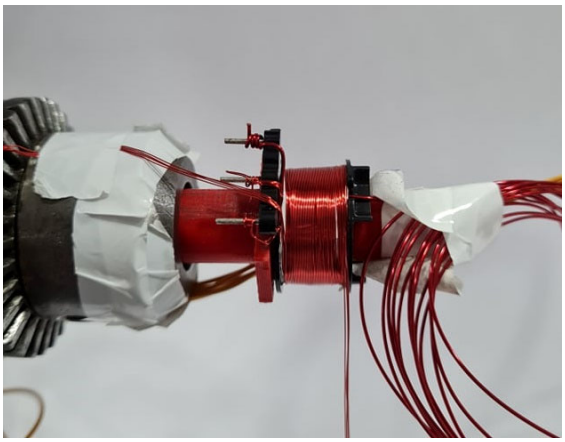
1st Primary (Primary 1)		Start at Pin 1, enter wire to bobbin Slot 1, and wind 1st primary 21 turns of wire Item [3] in 1 layer, from left to right.
Insulation	 	At the end of **Primary 1**, exit wire to the right and leave enough length of this wire for **Primary 2** (19 turns) to be wound later. Apply 3 layers of tape Item [11].

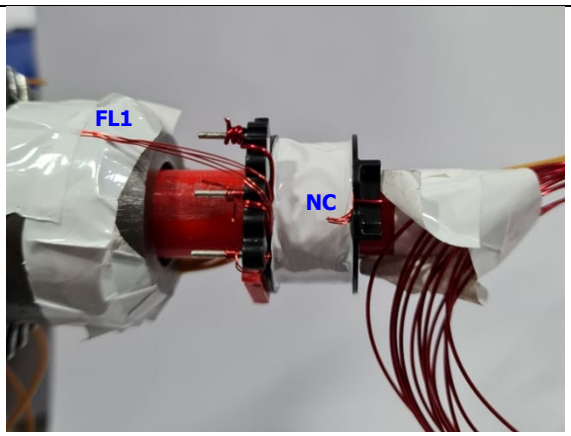
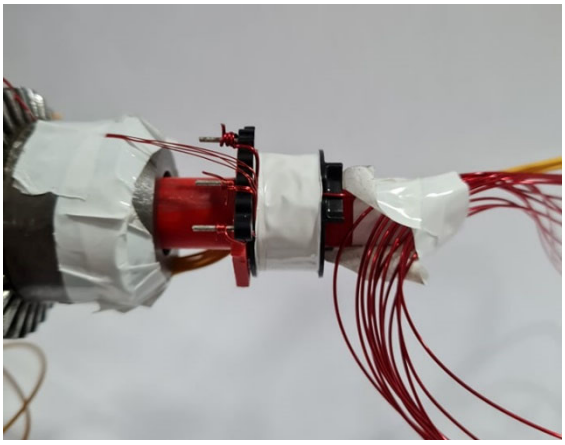
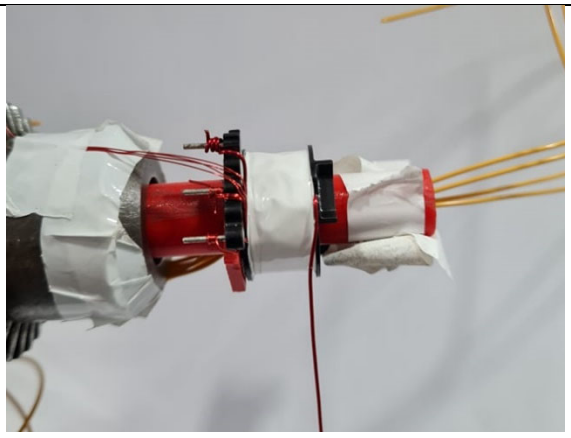
Primary Bias & Shield 1		Use 2 wires Item [4] for **Primary Bias**. Start at Pin 5 and enter to bobbin Slot 4. Use another 2 wires Item [4] for **Shield 1**. Start at Pin 3 and enter to bobbin Slot 3.
Primary Bias Termination	 	At the end of 10th turn, put 1 layer of tape Item [10] over the windings. Next, bring the wires for Primary Bias back to the left of bobbin Slot 3 and terminate it at Pin 3.

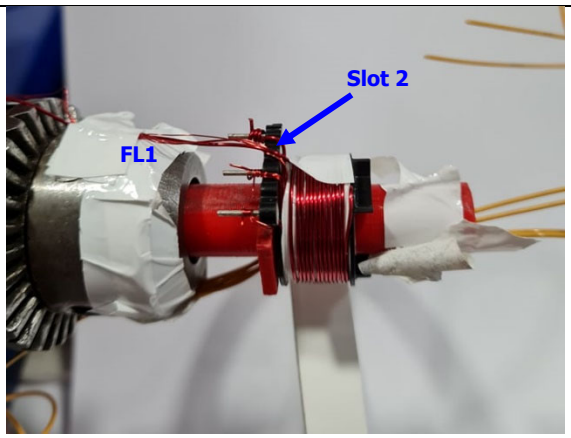
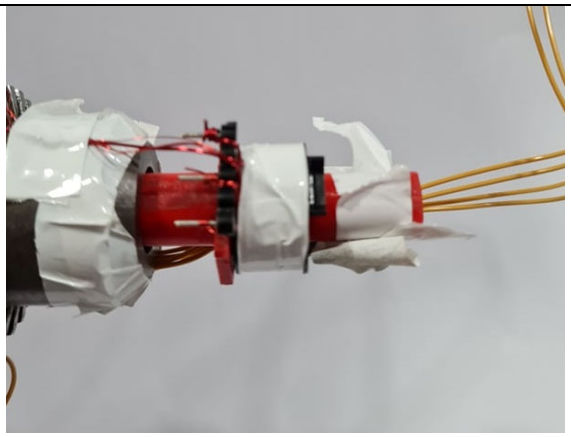
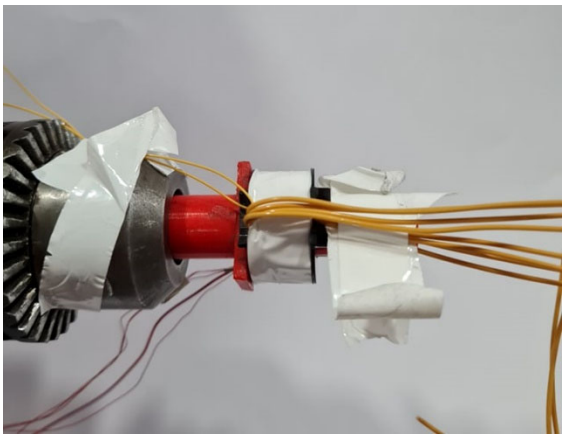
Shield Winding 1 Termination	 	Continue winding 4 more turns of Shield 1 to complete 14 turns. At the end of the turns, apply 1 layer of tape Item [8] to secure the winding. Cut short 2 wires of **Shield 1** to approximately 1/3 of bobbin width and leave as No-Connect (NC).
Insulation		Apply 3 layers of tape Item [11].

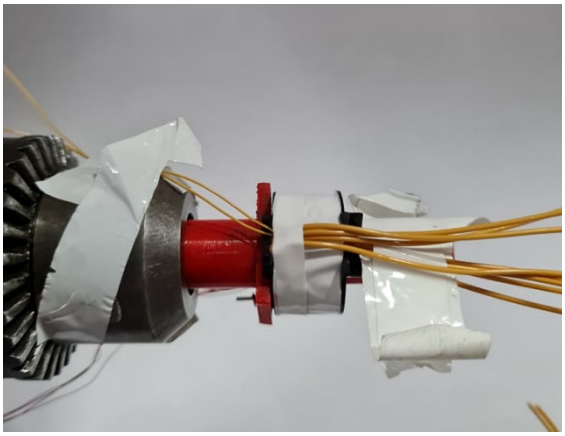
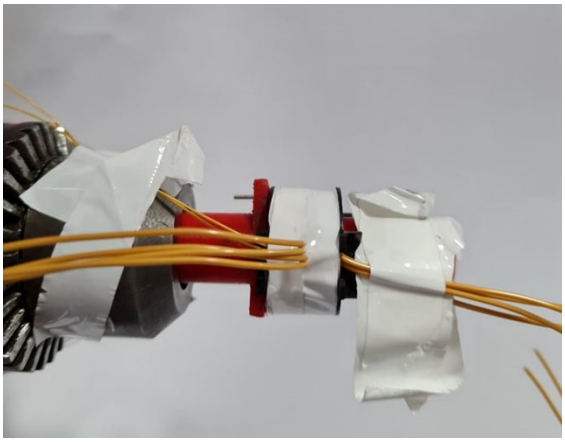
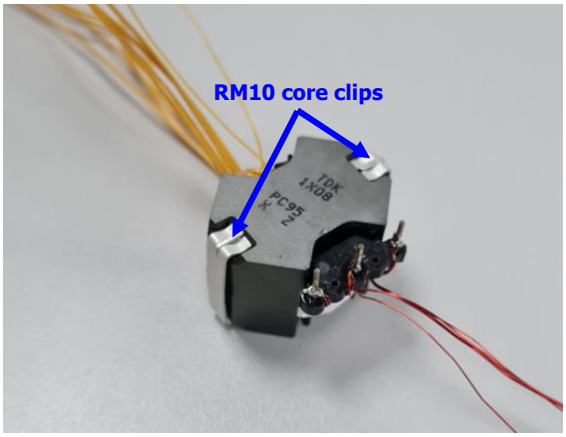
Secondary 1 and Secondary 2		Start at the secondary left slot of the bobbin. Use 2 wires Item [6], leave ~4" floating, and mark as FL3.
		Wind 5 turns in 1 layer. At the end of last turn, exit the wires at the right slot, leave ~2" floating and mark as FL2 for 1st half of secondary (**Secondary 1**)
		Repeat another winding same as above for 2nd half of secondary (**Secondary 2**), which is parallel with 1st half secondary (**Secondary 1**).

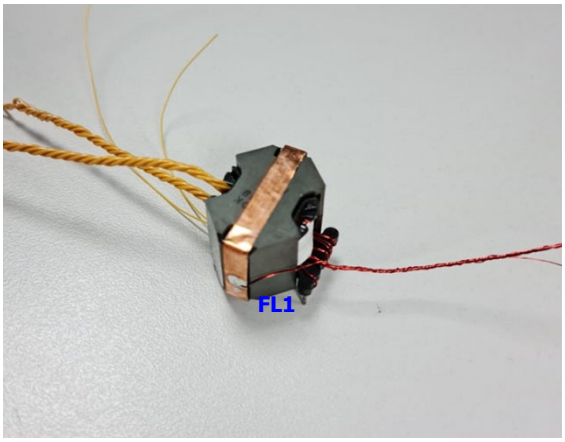
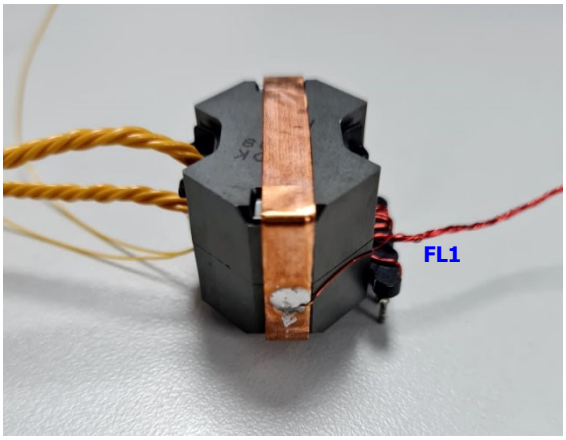
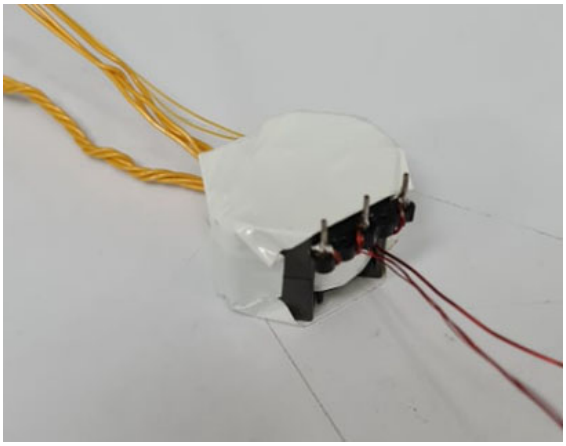
		
Secondary Bias	 	Use wire Item [7], start from the left and on the secondary side of bobbin, leaving ~2" and mark as FL5. Wind 2 turns and exit the wire also on the left leaving ~2" and mark as FL4. *(Ensure to wind the secondary bias in between grooves of Secondary 2 winding and not make any bumps)*

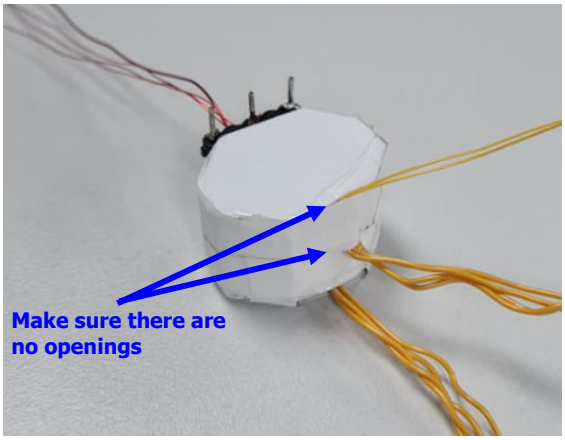
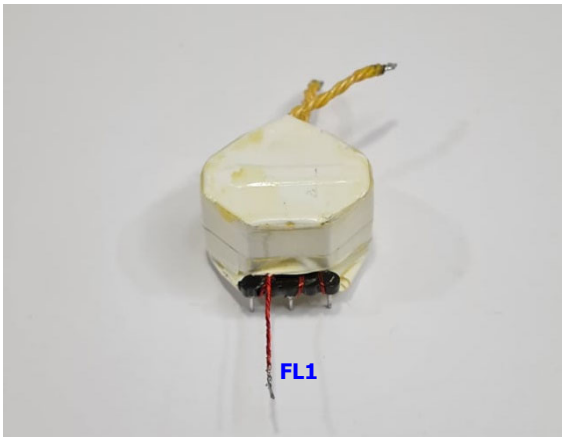
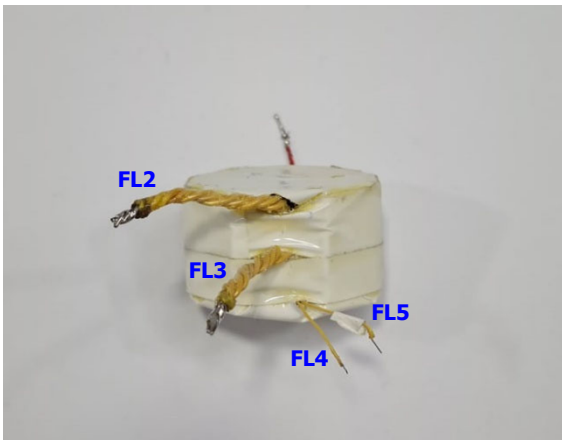
Insulation		Apply 3 layers of tape Item [12]. (*It is important to apply the tapes so that the layer next to it will be as flat as possible)*
Shield 2	 	Use 3 wires Item [5] for Shield 2. Leave ~2" floating and mark it as FL1 and enter to bobbin Slot 2. Wind 14 turns in parallel. (*It is important that the shield winding is as flat as possible so that there will be no gaps in between the windings)* At the end of last turn, place tape Item [11] to secure the winding, then cut short the 4 wires to approximately 1/3 of bobbin width and leave as No-Connect (NC).

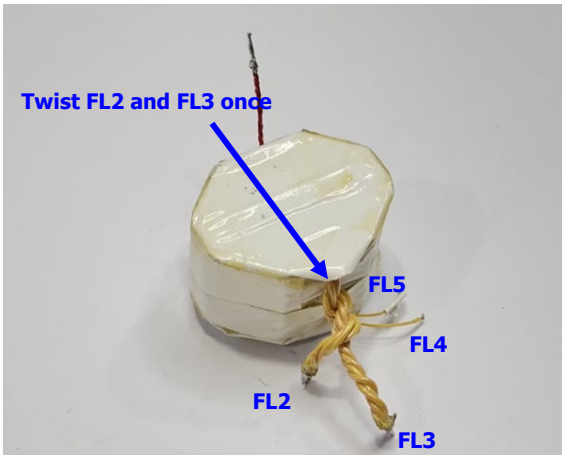
		
Insulation		Apply 3 layers of tape Item [11].
2nd Primary (Primary 2)		Using wire remaining from **Primary 1**, wind 19 turns of **Primary 2**, right to left. Spread the windings evenly. At the last turn, bring the wire out to the left of bobbin Slot 2, leave ~2" floating and mark it as FL1.

		
Insulation		Apply 2 layers of tape Item [11].
Secondary		Bring all 4 wires of Secondary Winding FL3 from left slot to exit to the right slot.

Insulation	 	Apply 2 layers of tape Item [9] that covers one half of FL3.
Gap, Core Clips, and Tape Insulation		Solder the wires to their respective bobbin pins (Pin 1, 3, 5). Add gap to the middle left of core Item [1] to get 486 µH ± 5% primary inductance. Use RM10 core clips Item [15] to fix the 2 cores into the bobbin. Cut the 2 terminals of the clips.

Core Grounding	 	Wrap 1 turn of copper foil Item [14] and solder wire Item [5] onto the copper foil. Label the termination as FL1 and twist the wire together with other FL1 terminations.
Tape for Core Insulation		Secure core halves by wrapping 2 layers of tape Item [13] along the transformer top, bottom, and sides. Ensure primary inductance is still 486 μH ± 5%.

		Use tape Item [11] for 2 horizontal wraps on upper and lower section of the transformer for improved ESD performance. *(It is important to make sure that there are no openings on the bottom and secondary side of transformer which can be exposed for improved ESD performance)*
Finish Assembly	 	Twist wires of FL1. Twist together the 4 wires of FL2. Also twist together the 4 wires of FL3.

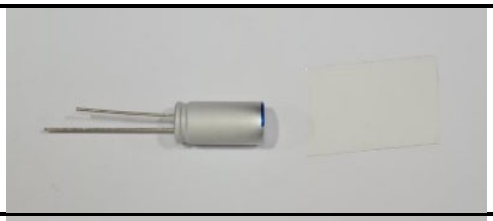
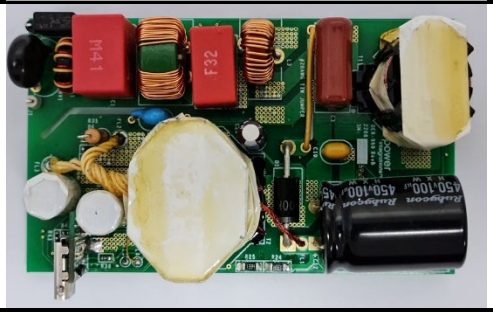
		Lastly, twist FL2 and FL3 together once to minimize the secondary loop for improved EMI performance. Cut FL2 and FL3 as short as possible such that it is just enough to terminate them on the board. Varnish with Item [16] to complete the transformer. Cut excess fly lead wire after soldering the transformer into the PCB.

10 PCB Assembly Instructions

10.1 *Material List*

Item	Description
[1]	Capacitor C27 on DER-960 Schematic.
[2]	Capacitor C28 on DER-960 Schematic.
[3]	Tape: 3M 1350F-1, Polyester Film, 1 mil Thickness, 17 mm Width.

10.2 *Output Capacitor Assembly Instructions*

	
	Cover the top of C27 and C28 with tape Item [3]. After which, wrap 2 layers of Item [3] around the capacitors to insulate the capacitor from transformer core.
	Finished assembly.

Note: Cut all the TH pins to <0.5 mm on the bottom side of the board after completing the assembly.

11 PFC Inductor Design Spreadsheet

1	Hiper_PFS-5_Boost_031722; Rev.1.0; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	Discontinuous Mode Boost Converter Design Spreadsheet
2	**Enter Application Variables**					
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN	90		90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX	265		265	VAC	Maximum AC input voltage
6	VBROWNIN			82	VAC	Expected Typical Brown-in Voltage per IC specifications; Line impedance not accounted for.
7	VBROWNOUT			71	VAC	Expected Typical Brown-out voltage per IC specifications; Line impedance not accounted for.
8	VO	400		400	VDC	Nominal load voltage
9	PO	105		105	W	Nominal Output power
10	fL	60		60	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate	0.9500		0.9500		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			380	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
15	T_HOLDUP			20	ms	Holdup time
16	VHOLDUP_MIN			320	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	No		No		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
20	**KP and INDUCTANCE**					
21	LPFC_MIN (0 bias)			262	uH	Minimum PFC inductance value
22	LPFC_TYP (0 bias)	276		276	uH	LPFC value used for calculations. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation.
23	LPFC_MAX (0 bias)			290	uH	Maximum PFC inductance value
24	LP_TOL			5.0	%	Tolerance of PFC Inductor Value (ferrite only)
25	LPFC_PEAK			276	uH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
26	KP_ACTUAL			1.25		Actual KP calculated from LPFC_DESIRED
28	**Basic Current Parameters**					
29	IAC_RMS			1.23	A	AC input RMS current at VACMIN and Full Power load
30	IL_RMS			1.58	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
31	IO_DC			0.26	A	Output average current/Average diode current
34	**PFS Parameters**					
35	PFS Package			F		HiperPFS package selection
36	PFS Part Number	PFS5274F		PFS5274F		If examining brownout operation, over-ride autopick with desired device size
37	Self-Supply Feature	No		No		Device self-supply feature. Select "Yes" to select device with self-supply feature or "No" for device without self-supply
38	PS_FACTOR	1.0		1.0		Programmable output power selection factor
39	PO_MAX_DEV			115	W	Maximum output power of the device
40	IOCP min			3.60	A	Minimum Current limit
41	IOCP typ			4.40	A	Typical current limit
42	IOCP max			5.20	A	Maximum current limit
43	IP			3.60	A	MOSFET peak current
44	IRMS			1.37	A	PFS MOSFET RMS current
45	RDSON			0.52	Ohms	Typical RDSon at 100 'C

46	FS_PK			80.6	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
47	FS_AVG			71.1	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
48	PCOND_LOSS_PFS			0.973	W	Estimated PFS Switch conduction losses
49	PSW_LOSS_PFS			0.008	W	Estimated PFS Switch switching losses
50	PFS_TOTAL			0.981	W	Total Estimated PFS Switch losses
51	TJ Max			100	deg C	Maximum steady-state junction temperature
52	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
53	HEATSINK Theta-CA			58.34	°C/W	Maximum thermal resistance of heatsink
56	**INDUCTOR DESIGN**					
57	**Material and Dimensions**					
58	Core Type	Ferrite		Ferrite		Enter "Sendust", "Iron Powder" or "Ferrite"
59	Core Material	Auto		PC44/PC95		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
60	Core Geometry	RM		RM		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
61	Core	RM8		RM8		Core part number
62	Ae			64.00	mm^2	Core cross sectional area
63	Le			38.00	mm	Core mean path length
64	AL			5290.00	nH/t^2	Core AL value
65	Ve			2.43	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)	3.38		3.38	mm	Core height/Height of window; ID if toroid
67	MLT			42.0	mm	Mean length per turn
68	BW	9.37		9.37	mm	Bobbin width
69	LG			0.96	mm	Gap length (Ferrite cores only)
70	**Flux and MMF Calculations**					
71	BP_TARGET (ferrite only)	4000	Info	4000	Gauss	Info: Peak flux density is too high. Check for Inductor saturation during line transient operation
72	B_OCP (or BP)			3991	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			2631	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance,minimum IOCP
74	µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
75	µ_MAX (powder only)			N/A	%	actual µ at peak current divided by µ at zero current, at VACMIN, full load (powder only)
76	µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
77	I_TEST			4.4	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			3377	Gauss	Flux density at I_TEST and maximum tolerance inductance
79	µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCPtyp
80	**Wire**					
81	TURNS			59		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
82	ILRMS			1.58	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	42		42	AWG	Inductor wire gauge
85	Filar	75		75		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
86	OD (per strand)			0.064	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			0.77	mm	Will be different than OD if Litz
88	DCR			0.233	ohm	Choke DC Resistance
89	P AC Resistance Ratio			0.36		Ratio of total copper loss, including HF AC, to the DC component of the loss

90	J		Warning	6.64	A/mm^2	Current density is high, if copper loss is high use thicker wire, more strands, or larger core
91	Layers			5.11		Estimated layers in winding
92	Auxiliary Winding					
93	N_AUX	5		5		Recommended auxiliary winding number of turns to ensure the supply to the VS pin
94	V_VS_MAX			1.29	V	Maximum voltage across the auxiliary winding
95	V_VS_MIN			-31.76	V	Minimum voltage across the auxiliary winding
96	RVS			10.00	kohm	Recommended series resistor to the VS pin. Place as close as possible to the VS pin of Hiper-PFS5
97	**Loss Calculations**					
98	BAC-p-p			2761	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
99	LPFC_CORE_LOSS			0.119	W	Estimated Inductor core Loss
100	LPFC_COPPER_LOSS			0.603	W	Estimated Inductor copper losses
101	LPFC_TOTAL_LOSS			0.722	W	Total estimated Inductor Losses
104	**PFC Diode**					
105	PFC Diode Part Number	STTH3R06		STTH3R06		PFS Diode Part Number
106	Type / Part Number			ULTRAFAST		PFC Diode Type / Part Number
107	Manufacturer			ST		Diode Manufacturer
108	VRRM			600.0	V	Diode rated reverse voltage
109	IF			3.00	A	Diode rated forward current
110	Qrr		Info	190.0	nC	Qrr too high: Will result in high diode loss
111	VF			1.25	V	Diode rated forward voltage drop
112	PCOND_DIODE			0.356	W	Estimated Diode conduction losses
113	PSW_DIODE			0.000	W	Estimated Diode switching losses
114	P_DIODE			0.356	W	Total estimated Diode losses
115	TJ Max			100.0	deg C	Maximum steady-state operating temperature
116	Rth-JS		Info	20.00	degC/W	Rth too high. Will result in high diode loss
117	HEATSINK Theta-CA			147.95	degC/W	Maximum thermal resistance of heatsink
118	IFSM			55.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
121	**Output Capacitor**					
122	COUT	100		100	uF	Minimum value of Output capacitance
123	VO_RIPPLE_EXPECTED			7.3	V	Expected ripple voltage on Output with selected Output capacitor
124	T_HOLDUP_EXPECTED			27.4	ms	Expected holdup time with selected Output capacitor
125	ESR_LF			2.02	ohms	Low Frequency Capacitor ESR
126	ESR_HF			0.81	ohms	High Frequency Capacitor ESR
127	IC_RMS_LF			0.18	A	Low Frequency Capacitor RMS current
128	IC_RMS_HF			0.71	A	High Frequency Capacitor RMS current
129	CO_LF_LOSS			0.066	W	Estimated Low Frequency ESR loss in Output capacitor
130	CO_HF_LOSS			0.406	W	Estimated High frequency ESR loss in Output capacitor
131	Total CO LOSS			0.472	W	Total estimated losses in Output Capacitor
134	**Input Bridge (BR1) and Fuse (F1)**					
135	I^2t Rating			7.02	A^2*s	Minimum I^2t rating for fuse
136	Fuse Current rating			1.88	A	Minimum Current rating of fuse
137	VF			0.90	V	Input bridge Diode forward Diode drop
138	IAVG			1.17	A	Input average current at VBROWNOUT.
139	PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
140	PCOND_LOSS_BRIDGE			1.990	W	Estimated Bridge Diode conduction loss
141	CIN			0.33	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
142	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
143	CIN_PLOSS			0.007	W	Input Capacitor Loss
144	RT1			9.37	ohms	Input Thermistor value
145	D_Precharge			1N5407		Recommended precharge Diode
148	**PFS5 Small Signal Components**					
149	RVS			10.0	kOhms	VS pin resistor for valley sensing. This resistor should be optimized such that proper delay is introduced from the instant the voltage on the sense winding goes below the Vvs2 threshold to the instant when the cascode turns-on (valley sensing). Must be tested on the bench

150	RPS			> 400	kOhms	Power programmability resistor. Leaving PS pin open is acceptable
151	RV1			4.0	MOhms	Line sense resistor 1
152	RV2			6.0	MOhms	Line sense resistor 2
153	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
154	RV4			155.5	kOhms	Description pending, could be modified based on feedback chain R1-R4
155	C_V			0.514	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
156	C_VCC			1.0	uF	Supply decoupling capacitor
157	C_C			100	nF	Feedback C pin decoupling capacitor
158	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
159	PGT set resistor			320.5	kohm	Power good threshold setting resistor
162	**Feedback Components**					
163	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
164	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
165	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
166	RFB_4			155.5	kohms	Feedback network, lower divider resistor
167	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
168	RFB_5			39.2	kohms	Feedback network: zero setting resistor
169	CFB_2			1000	nF	Feedback component- noise suppression capacitor
172	**Loss Budget (Estimated at VACMIN)**					
173	PFS Losses			0.981	W	Total estimated losses in PFS
174	Boost diode Losses			0.356	W	Total estimated losses in Output Diode
175	Input Bridge losses			1.990	W	Total estimated losses in input bridge module
176	Input Capacitor Losses			0.007	W	Total estimated losses in input capacitor
177	Inductor losses			0.722	W	Total estimated losses in PFC choke
178	Output Capacitor Loss			0.472	W	Total estimated losses in Output capacitor
179	EMI choke copper loss			0.151	W	Total estimated losses in EMI choke copper
180	Total losses			4.680	W	Overall loss estimate
181	Efficiency			95.73	%	Estimated efficiency at VACMIN, full load.
184	**HiperPFS-5 Integrated CAPZero Function**					
185	Total Series Resistance (Rcapzero1+Rcapzero2)			0.864	MOhms	Maximum total series resistor value to discharge X-capacitors with time constant of 1 second. Resistors must be connected to D1 and D2 pins of the HiperPFS-5 part for integrated CAPZero function
188	**EMI Filter Components Recommendation**					
189	CX2	330		330	nF	X-capacitor after differential mode choke and before bridge, ratio with Po
190	LDM_calc			384	uH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
191	CX1			470	nF	X-capacitor before common mode choke, ratio with Po
192	LCM			10.0	mH	Typical common mode choke value
193	LCM_leakage			30	uH	Estimated leakage inductance of CM choke, typical from 30~60uH
194	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
195	LDM_Actual			354	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
196	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
197	DCR_LDM			0.030	Ohms	Total DCR of DM choke(or CM #2) for estimating copper loss
199	**Note: CX2 can be placed between CM choke and DM choke depending on EMI design requirement.**					

Note: The warnings on the spreadsheet have been verified to not be an issue for this design. For line 90 (J), high system efficiency is still achieved.

12 Transformer Design Spreadsheet

Two transformer design spreadsheets are presented in this section

- Flyback stage with PFC ON (100 W output operation)
- Flyback stage with PFC OFF (65 W output operation)

12.1 *Flyback Stage with PFC ON*

1	ACDC_InnoSwitch4-Pro_Flyback_040622; Rev.0.3; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4-Pro Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	DC		DC		Input Type
4	VIN_MIN	395		395	V	Minimum DC input voltage
5	VIN_MAX	405		405	V	Maximum DC input voltage
6	VIN_RANGE			PFC INPUT		Input voltage range
7	FLINE				Hz	AC Input voltage frequency
8	CAP_INPUT				uF	Input capacitance
10	**SET-POINT 1**					
11	VOUT1	21.00		21.00	V	Output voltage 1, should be the highest output voltage required
12	IOUT1	4.761		4.761	A	Output current 1
13	POUT1			99.98	W	Output power 1
14	EFFICIENCY1	0.94		0.94		Converter efficiency for output 1
15	Z_FACTOR1	0.60		0.60		Z-factor for output 1
16	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
18	**SET-POINT 2**					
19	VOUT2	20.00		20.00	V	Output voltage 2
20	IOUT2	5.000		5.000	A	Output current 2
21	POUT2			100.00	W	Output power 2
22	EFFICIENCY2	0.94		0.94		Converter efficiency for output 2
23	Z_FACTOR2	0.60		0.60		Z-factor for output 2
24	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
26	**SET-POINT 3**					
27	VOUT3	15.00		15.00	V	Output voltage 3
28	IOUT3	5.000		5.000	A	Output current 3
29	POUT3			75.00	W	Output power 3
30	EFFICIENCY3	0.93		0.93		Converter efficiency for output 3
31	Z_FACTOR3	0.60		0.60		Z-factor for output 3
32	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
82	VOLTAGE_CDC	0.000		0.000	V	Cable drop compensation desired at full load
86	**PRIMARY CONTROLLER SELECTION**					
87	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
88	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
89	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
90	DEVICE_GENERIC	AUTO		INN4375		Device selection
91	DEVICE_CODE			INN4375F		Device code
92	PDEVICE_MAX			100	W	Device maximum power capability
93	RDSON_100DEG			0.54	Ω	Primary switch on-time resistance at 100°C
94	ILIMIT_MIN			2.374	A	Primary switch minimum current limit
95	ILIMIT_TYP			2.580	A	Primary switch typical current limit
96	ILIMIT_MAX			2.786	A	Primary switch maximum current limit
97	VDRAIN_ON_PRSW			0.14	V	Primary switch on-time voltage drop

98	VDRAIN_OFF_PRSW			620	V	Peak drain voltage on the primary switch during turn-off
102	**WORST CASE ELECTRICAL PARAMETERS**					
103	FSWITCHING_MAX	83000		83000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
104	VOR	165.0		165.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
105	VMIN			395.00	V	Minimum DC input voltage at full load
106	KP			1.347		Measure of continuous/discontinuous mode of operation
107	MODE_OPERATION			DCM		Mode of operation
108	DUTYCYCLE			0.228		Primary switch duty cycle
109	TIME_ON			3.37	us	Primary switch on-time
110	TIME_OFF			8.83	us	Primary switch off-time
111	LPRIMARY_MIN			461.7	uH	Minimum primary magnetizing inductance
112	LPRIMARY_TYP			486.0	uH	Typical primary magnetizing inductance
113	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
114	LPRIMARY_MAX			510.3	uH	Maximum primary magnetizing inductance
116	**PRIMARY CURRENT**					
117	IAVG_PRIMARY			0.263	A	Primary switch average current
118	IPEAK_PRIMARY			2.641	A	Primary switch peak current
119	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
120	IRIPPLE_PRIMARY			2.641	A	Primary switch ripple current
121	IRMS_PRIMARY			0.680	A	Primary switch RMS current
123	**SECONDARY CURRENT**					
124	IPEAK_SECONDARY			21.125	A	Secondary winding peak current
125	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
126	IRMS_SECONDARY			8.627	A	Secondary winding RMS current
127	IRIPPLE_CAP_OUT			7.030	A	Output capacitor ripple current
131	**TRANSFORMER CONSTRUCTION PARAMETERS**					
132	**CORE SELECTION**					
133	CORE	RM10		RM10		Core selection. Refer to the "Transformer Construction" tab for the detailed report.
134	CORE NAME			B65813-J-R97		Core code
135	AE			98.0	mm^2	Core cross sectional area
136	LE			44.0	mm	Core magnetic path length
137	AL			4200	nH	Ungapped core effective inductance per turns squared
138	VE			4310	mm^3	Core volume
139	BOBBIN NAME			B65814-N1012-D1		Bobbin name
140	AW			41.5	mm^2	Bobbin window area
141	BW	10.00		10.00	mm	Bobbin width
142	MARGIN			0.0	mm	Bobbin safety margin
144	**PRIMARY WINDING**					
145	NPRIMARY			40		Primary winding number of turns
146	BPEAK			3783	Gauss	Peak flux density
147	BMAX			3395	Gauss	Maximum flux density
148	BAC			1698	Gauss	AC flux density (0.5 x Peak to Peak)
149	ALG			304	nH	Typical gapped core effective inductance per turns squared
150	LG			0.376	mm	Core gap length
152	**PRIMARY BIAS WINDING**					
153	NBIAS_PRIMARY			10		Primary bias winding number of turns
155	**SECONDARY WINDING**					
156	NSECONDARY	5		5		Secondary winding number of turns
158	**SECONDARY BIAS WINDING**					
159	NBIAS_SECONDARY			2		Secondary bias winding number of turns
162	**PRIMARY COMPONENTS SELECTION**					
163	**CLAMPZERO**					

164	LLEAK			4.86	uH	Primary winding leakage inductance
165	CCLAMP			100.0	nF	Primary clamp capacitor
166	RD_CLAMPZERO	30		30	kΩ	HSD resistor
167	TLLDL/THLDL			430.0	ns	HSD resistor programmed delay
168	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			375.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
169	TIME_VDS_VALLEY			45.4	ns	Time taken by the VDS ring to reach its first valley
170	IPEAK_CLAMPZERO			2.589	A	Active clamp peak current
172	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
173	BROWN-IN REQURED	115.00		115.00	V	Required AC RMS/DC line brown-in threshold
174	RLS			4.10	MΩ	Connect two 2.05 MOhm resistors to the V-pin for the required UV/OV threshold
175	BROWN-IN ACTUAL			116.19	V	Actual AC RMS/DC brown-in threshold using standard resistors
176	BROWN-OUT ACTUAL			105.08	V	Actual AC RMS/DC brown-out threshold using standard resistors
177	OVERVOLTAGE_LINE		Warning	484.45	V	The device voltage stress will be higher than 650V when overvoltage is triggered
179	**PRIMARY BIAS WINDING**					
180	VBIAS_PRIMARY			9.00	V	Rectified primary bias voltage at the cable-disconnect (5V) set-point
181	VF_BIAS_PRIMARY			0.70	V	Primary bias winding diode forward drop
182	VREVERSE_BIASDIODE_PRIMARY			184.82	V	Primary bias diode reverse voltage (not accounting parasitic voltage ring)
183	CBIAS_PRIMARY			22	uF	Primary bias winding rectification capacitor
184	CBPP			4.70	uF	BPP pin capacitor
188	**SECONDARY COMPONENTS SELECTION**					
189	**RECTIFIER**					
190	VDRAIN_OFF_SRFET			71.63	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
191	SRFET	SIR804DP	Info	SIR804DP		The voltage stress (including the parasitic ring) on the secondary MOSFET selected may exceed the device BVDSS: pick a MOSFET with a higher BVDSS
192	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
193	RDSON_SRFET			10.3	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
195	**SECONDARY BIAS WINDING**					
196	USE_SECONDARYBIAS	AUTO		YES		Select to use secondary bias winding or not
197	VBIAS_SECONDARY			6.00	V	Rectified secondary bias voltage at full load
198	VF_BIAS_SECONDARY			0.70	V	Secondary bias winding diode forward drop
199	VREVERSE_BIASDIODE_SECONDARY			48.85	V	Secondary bias diode reverse voltage (not accounting parasitic voltage ring)
200	CBIAS_SECONDARY			10	uF	Secondary bias winding rectification capacitor
201	CBPS			2.20	uF	BPS pin capacitor

Note: The warnings on the spreadsheet have been verified to not be an issue for this design. For line 177 (OVERVOLTAGE_LINE), the InnoSwitch4-Pro INN4375F is a 750 V device.

12.2 *Flyback Stage with PFC OFF*

1	ACDC_InnoSwitch4-Pro_Flyback_040622; Rev.0.3; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	InnoSwitch4-Pro Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	INPUT_TYPE	AC		AC		Input Type
4	VIN_MIN	90		90	V	Minimum AC input voltage
5	VIN_MAX	265		265	V	Maximum AC input voltage
6	VIN_RANGE			UNIVERSAL		Input voltage range
7	FLINE			60	Hz	AC Input voltage frequency
8	CAP_INPUT	100.0		100.0	uF	Input capacitance
10	**SET-POINT 1**					
11	VOUT1	21.00		21.00	V	Output voltage 1, should be the highest output voltage required
12	IOUT1	3.100		3.100	A	Output current 1
13	POUT1			65.10	W	Output power 1
14	EFFICIENCY1	0.93		0.93		Converter efficiency for output 1
15	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
18	**SET-POINT 2**					
19	VOUT2	20.00		20.00	V	Output voltage 2
20	IOUT2	3.250		3.250	A	Output current 2
21	POUT2			65.00	W	Output power 2
22	EFFICIENCY2	0.93		0.93		Converter efficiency for output 2
23	Z_FACTOR2	0.50		0.50		Z-factor for output 2
24	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
26	**SET-POINT 3**					
27	VOUT3	15.00		15.00	V	Output voltage 3
28	IOUT3	4.330		4.330	A	Output current 3
29	POUT3			64.95	W	Output power 3
30	EFFICIENCY3	0.93		0.93		Converter efficiency for output 3
31	Z_FACTOR3	0.50		0.50		Z-factor for output 3
32	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
34	**SET-POINT 4**					
35	VOUT4	12.00		12.00	V	Output voltage 4
36	IOUT4	5.000		5.000	A	Output current 4
37	POUT4			60.00	W	Output power 4
38	EFFICIENCY4	0.93		0.93		Converter efficiency for output 4
39	Z_FACTOR4	0.50		0.50		Z-factor for output 4
40	TYPE	PDO	Info	PDO		The voltage entered is not a standard PDO(Power Delivery Object)
42	**SET-POINT 5**					
43	VOUT5	9.00		9.00	V	Output voltage 5
44	IOUT5	5.000		5.000	A	Output current 5
45	POUT5			45.00	W	Output power 5
46	EFFICIENCY5	0.92		0.92		Converter efficiency for output 5
47	Z_FACTOR5	0.50		0.50		Z-factor for output 5
48	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
50	**SET-POINT 6**					
51	VOUT6	5.00		5.00	V	Output voltage 6
52	IOUT6	5.000		5.000	A	Output current 6
53	POUT6			25.00	W	Output power 6

54	EFFICIENCY6	0.92		0.92		Converter efficiency for output 6
55	Z_FACTOR6	0.50		0.50		Z-factor for output 6
56	TYPE	PDO		PDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
58	**SET-POINT 7**					
59	VOUT7	3.30		3.30	V	Output voltage 7
60	IOUT7	5.000		5.000	A	Output current 7
61	POUT7			16.50	W	Output power 7
62	EFFICIENCY7	0.90		0.90		Converter efficiency for output 7
63	Z_FACTOR7	0.50		0.50		Z-factor for output 7
64	TYPE	APDO		APDO		Select whether this set-point is a PDO(Power Delivery Object) or APDO(Augmented Power Data Object)
82	VOLTAGE_CDC	0.000		0.000	V	Cable drop compensation desired at full load
86	**PRIMARY CONTROLLER SELECTION**					
87	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
88	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
89	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
90	DEVICE_GENERIC	INN4375		INN4375		Device selection
91	DEVICE_CODE			INN4375F		Device code
92	PDEVICE_MAX			80	W	Device maximum power capability
93	RDSON_100DEG			0.54	Ω	Primary switch on-time resistance at 100°C
94	ILIMIT_MIN			2.374	A	Primary switch minimum current limit
95	ILIMIT_TYP			2.580	A	Primary switch typical current limit
96	ILIMIT_MAX			2.786	A	Primary switch maximum current limit
97	VDRAIN_ON_PRSW			0.42	V	Primary switch on-time voltage drop
98	VDRAIN_OFF_PRSW			588.31	V	Peak drain voltage on the primary switch during turn-off
102	**WORST CASE ELECTRICAL PARAMETERS**					
103	FSWITCHING_MAX	61283	Info	61283	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
104	VOR	165.0		165.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
105	VMIN			87.22	V	Valley of the rectified minimum input AC voltage at full load
106	KP			0.763		Measure of continuous/discontinuous mode of operation
107	MODE_OPERATION			CCM		Mode of operation
108	DUTYCYCLE			0.655		Primary switch duty cycle
109	TIME_ON		Info	14.40	us	Primary switch on-time is greater than 12.4us: Increase the controller switching frequency or increase the VOR
110	TIME_OFF			5.28	us	Primary switch off-time
111	LPRIMARY_MIN			461.7	uH	Minimum primary magnetizing inductance
112	LPRIMARY_TYP			486.0	uH	Typical primary magnetizing inductance
113	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
114	LPRIMARY_MAX			510.3	uH	Maximum primary magnetizing inductance
116	**PRIMARY CURRENT**					
117	IAVG_PRIMARY			0.778	A	Primary switch average current
118	IPEAK_PRIMARY			2.491	A	Primary switch peak current
119	IPEDESTAL_PRIMARY			0.517	A	Primary switch current pedestal
120	IRIPPLE_PRIMARY			2.489	A	Primary switch ripple current
121	IRMS_PRIMARY			1.138	A	Primary switch RMS current
123	**SECONDARY CURRENT**					
124	IPEAK_SECONDARY			19.928	A	Secondary winding peak current
125	IPEDESTAL_SECONDARY			4.132	A	Secondary winding pedestal current
126	IRMS_SECONDARY			8.347	A	Secondary winding RMS current
127	IRIPPLE_CAP_OUT			6.684	A	Output capacitor ripple current
131	**TRANSFORMER CONSTRUCTION PARAMETERS**					

132	**CORE SELECTION**					
133	CORE	RM10		RM10		Core selection. Refer to the "Transformer Construction" tab for the detailed report.
134	CORE NAME			B65813-J-R97		Core code
135	AE			98.0	mm^2	Core cross sectional area
136	LE			44.0	mm	Core magnetic path length
137	AL			4200	nH	Ungapped core effective inductance per turns squared
138	VE			4310	mm^3	Core volume
139	BOBBIN NAME			B65814-N1012-D1		Bobbin name
140	AW			41.5	mm^2	Bobbin window area
141	BW	10.00		10.00	mm	Bobbin width
142	MARGIN			0.0	mm	Bobbin safety margin
144	PRIMARY WINDING					
145	NPRIMARY			40		Primary winding number of turns
146	BPEAK			3783	Gauss	Peak flux density
147	BMAX			3193	Gauss	Maximum flux density
148	BAC			1594	Gauss	AC flux density (0.5 x Peak to Peak)
149	ALG			304	nH	Typical gapped core effective inductance per turns squared
150	LG			0.376	mm	Core gap length
152	**PRIMARY BIAS WINDING**					
153	NBIAS_PRIMARY			10		Primary bias winding number of turns
155	**SECONDARY WINDING**					
156	NSECONDARY	5		5		Secondary winding number of turns
158	**SECONDARY BIAS WINDING**					
159	NBIAS_SECONDARY			2		Secondary bias winding number of turns
162	**PRIMARY COMPONENTS SELECTION**					
163	**CLAMPZERO**					
164	LLEAK			4.86	uH	Primary winding leakage inductance
165	CCLAMP			100.0	nF	Primary clamp capacitor
166	RD_CLAMPZERO	30		30	kΩ	HSD resistor
167	TLLDL/THLDL			120.0	ns	HSD resistor programmed delay
168	TIME_CLAMPZERO_OFF_TO_PRIMARY_ON			65.0	ns	Time between the ClampZero FET turn off and the primary FET turns on based on the HSD resistor selection
169	TIME_VDS_VALLEY			45.4	ns	Time taken by the VDS ring to reach its first valley
170	IPEAK_CLAMPZERO			2.442	A	Active clamp peak current
172	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
173	BROWN-IN REQURED	82.00		82.00	V	Required AC RMS/DC line brown-in threshold
174	RLS			4.10	MΩ	Connect two 2.05 MOhm resistors to the V-pin for the required UV/OV threshold
175	BROWN-IN ACTUAL			82.16	V	Actual AC RMS/DC brown-in threshold using standard resistors
176	BROWN-OUT ACTUAL			74.30	V	Actual AC RMS/DC brown-out threshold using standard resistors
177	OVERVOLTAGE_LINE		Warning	342.56	V	The device voltage stress will be higher than 650V when overvoltage is trigerred
179	**PRIMARY BIAS WINDING**					
180	VBIAS_PRIMARY			9.00	V	Rectified primary bias voltage at the cable-disconnect (5V) set-point
181	VF_BIAS_PRIMARY			0.70	V	Primary bias winding diode forward drop
182	VREVERSE_BIASDIODE_PRIMARY			135.33	V	Primary bias diode reverse voltage (not accounting parasitic voltage ring)
183	CBIAS_PRIMARY			22	uF	Primary bias winding rectification capacitor
184	CBPP			4.70	uF	BPP pin capacitor
188	**SECONDARY COMPONENTS SELECTION**					
189	**RECTIFIER**					

190	VDRAIN_OFF_SRFET			67.85	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
191	SRFET	SIR804DP		SIR804DP		Secondary rectifier (Logic MOSFET)
192	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
193	RDSON_SRFET			10.3	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
195	**SECONDARY BIAS WINDING**					
196	USE_SECONDARYBIAS	AUTO		YES		Select to use secondary bias winding or not
197	VBIAS_SECONDARY			6.00	V	Rectified secondary bias voltage at full load
198	VF_BIAS_SECONDARY			0.70	V	Secondary bias winding diode forward drop
199	VREVERSE_BIASDIODE_SECONDARY			99.33	V	Secondary bias diode reverse voltage (not accounting parasitic voltage ring)
200	CBIAS_SECONDARY			10	uF	Secondary bias winding rectification capacitor
201	CBPS			2.20	uF	BPS pin capacitor

Note: The warnings on the spreadsheet have been verified to not be an issue for this design. For line 177 (OVERVOLTAGE_LINE), the InnoSwitch4-Pro INN4375F is a 750 V device.

13 Performance Data

Note: 1. Output voltage measured on the PCB unless otherwise specified.
2. For data points showing performance across varying input line voltage and output load current, measurements were taken from full load to no load, with input line voltage from low-line to high-line, at room temperature ambient (approximately 25 °C) unless otherwise specified.

13.1 *No-Load Input Power*

13.1.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 230 VAC, 265 VAC
Output Load Condition	0% (Unit tested without Type-C cable connected to output)
Soak Time per Line	15 minutes
Integration time	5 minutes

13.1.2 Test Results

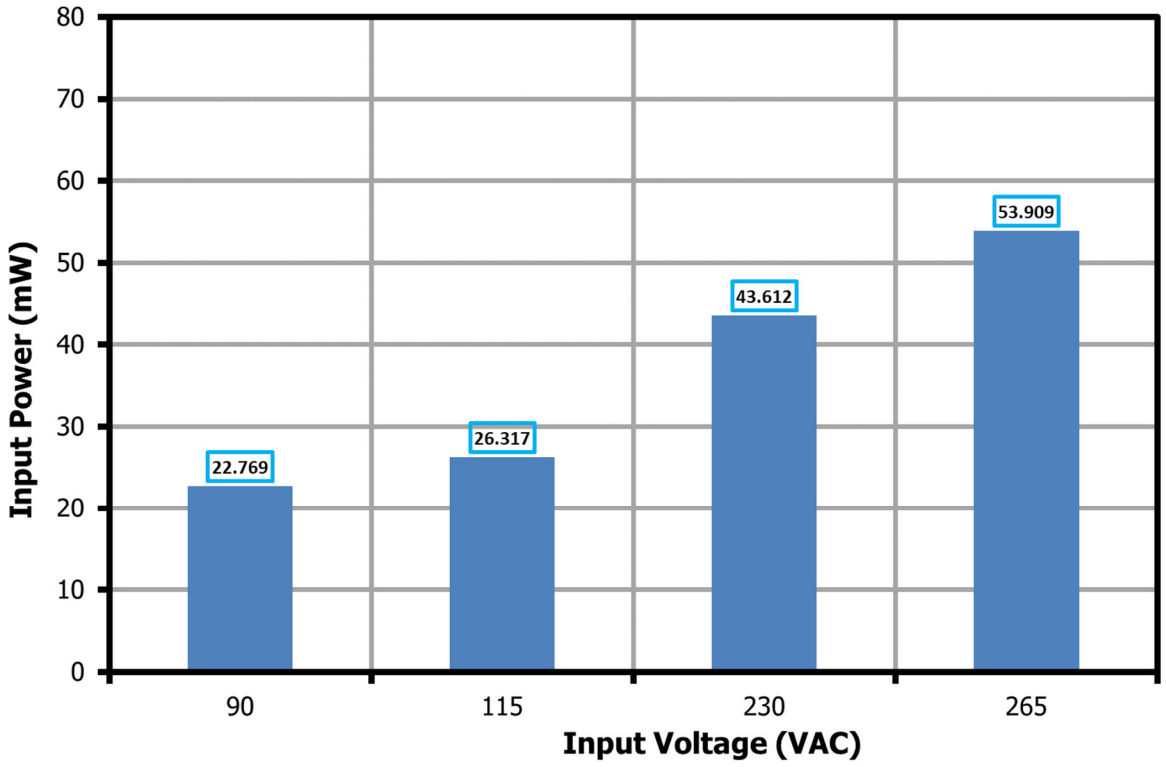


Figure 17 – No-Load Input Power vs. Input Line Voltage.

13.2 *Full Load Efficiency (On-board)*

V_{OUT} (V)	Load (A)	Power (W)	Full Load Efficiency (%)			
			90 VAC	115 VAC	230 VAC	265 VAC
5	5	25	90.55	91.15	91.45	91.29
9	5	45	91.15	92.00	93.01	92.94
12	5	60	91.11	92.18	93.43	93.43
15	5	75	91.00	91.83	93.10	93.26
20	5	100	91.01	92.00	93.45	93.62

13.3 *Average and 10% Load Efficiency*

13.3.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 230 VAC, 265 VAC
Output Voltage	5 V, 9 V, 12 V, 15 V, 20 V
Output Load	100%, 75%, 50%, 25%, 10%
Soak Time per Line	30 minutes
Delay Time per Load	1 minute
Output Voltage Measurement	On-Board

13.3.2 Efficiency Requirements

		Test	Average Efficiency (%)		10% Load Efficiency (%)
		Effective	2016	Jan-16	Jan-16
V_{OUT} (V)	Model (V)	Power (W)	New EISA2007	CoC v5 Tier 2	CoC v5 Tier 2
5	<6	25	84.25	85.00	73.18
9	>6	45	87.73	88.85	78.43
12	>6	60	88.00	89.00	79.00
15	>6	75	88.00	89.00	79.00
20	>6	100	88.00	89.00	79.00

13.3.3 Efficiency Performance Summary (On Board)

V_{OUT} (V)	Power (W)	Average Efficiency (%)		10% Load Efficiency (%)	
		115 VAC	230 VAC	115 VAC	230 VAC
5	25	91.51	91.30	90.01	87.82
9	45	92.20	92.83	89.90	89.32
12	60	92.32	93.27	89.88	89.88
15	75	92.08	93.19	89.75	90.30
20	100	91.99	93.35	89.45	90.59

13.3.4 Average and 10% Load Efficiency Measurements

13.3.4.1 Output: 5 V / 5 A

Input (VAC)	Load (%)	Design Performance						Efficiency Standards		Remarks
		P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)	CoC v5 Tier 2 (%)	
115	100	27.97	5.094	4.999	25.47	91.05	**91.51**	84.25	85.00	**PASS**
	75	20.78	5.071	3.749	19.01	91.50				
	50	13.74	5.053	2.499	12.63	91.91				
	25	6.86	5.030	1.250	6.29	91.59				
	10	2.78	5.018	0.499	2.51	**90.01**			75.47	**PASS**
230	100	27.86	5.098	5.000	25.49	91.49	**91.30**	84.25	85.00	**PASS**
	75	20.77	5.080	3.749	19.05	91.70				
	50	13.80	5.058	2.500	12.64	91.61				
	25	6.96	5.036	1.250	6.29	90.40				
	10	2.86	5.023	0.499	2.51	**87.82**			75.47	**PASS**

13.3.4.2 Output: 9 V / 5 A

Input (VAC)	Load (%)	Design Performance						Efficiency Standards		Remarks
		P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)	CoC v5 Tier 2 (%)	
115	100	49.57	9.120	5.000	45.60	91.99	**92.20**	87.73	88.85	**PASS**
	75	36.97	9.095	3.749	34.10	92.24				
	50	24.55	9.078	2.500	22.69	92.42				
	25	12.28	9.055	1.250	11.31	92.13				
	10	5.02	9.038	0.499	4.51	**89.90**			78.85	**PASS**
230	100	49.08	9.127	4.999	45.63	92.97	**92.83**	87.73	88.85	**PASS**
	75	36.68	9.108	3.749	34.15	93.10				
	50	24.39	9.086	2.499	22.71	93.11				
	25	12.28	9.058	1.250	11.32	92.16				
	10	5.05	9.042	0.499	4.51	**89.32**			78.85	**PASS**

13.3.4.3 Output: 12 V / 5 A

Input (VAC)	Load (%)	Design Performance						Efficiency Standards		Remarks
		P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)	CoC v5 Tier 2 (%)	
115	100	65.13	12.001	4.999	60.00	92.12	**92.32**	88.00	89.00	**PASS**
	75	48.77	12.017	3.749	45.06	92.38				
	50	32.50	12.033	2.500	30.08	92.54				
	25	16.31	12.043	1.250	15.05	92.26				
	10	6.69	12.043	0.499	6.01	**89.88**			79.00	**PASS**
230	100	64.27	12.006	4.999	60.02	93.39	**93.27**	88.00	89.00	**PASS**
	75	48.21	12.023	3.749	45.08	93.50				
	50	32.17	12.035	2.499	30.08	93.51				
	25	16.23	12.043	1.249	15.05	92.70				
	10	6.69	12.044	0.499	6.01	**89.88**			79.00	**PASS**

13.3.4.4 Output: 15 V / 5 A

Input (VAC)	Load (%)	Design Performance						Efficiency Standards		Remarks
		P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)	CoC v5 Tier 2 (%)	
115	100	81.97	15.056	4.999	75.27	91.83	**92.08**	88.00	89.00	**PASS**
	75	61.55	15.069	3.749	56.50	91.79				
	50	40.71	15.072	2.500	37.67	92.54				
	25	20.44	15.080	1.250	18.84	92.18				
	10	8.39	15.078	0.499	7.53	**89.75**			79.00	**PASS**
230	100	80.82	15.059	4.999	75.29	93.15	**93.19**	88.00	89.00	**PASS**
	75	60.80	15.072	3.749	56.51	92.94				
	50	40.25	15.079	2.499	37.69	93.63				
	25	20.26	15.084	1.250	18.85	93.03				
	10	8.34	15.080	0.499	7.53	**90.30**			79.00	**PASS**

13.3.4.5 Output: 20 V / 5 A

Input (VAC)	Load (%)	Design Performance						Efficiency Standards		Remarks
		P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 (%)	CoC v5 Tier 2 (%)	
115	100	109.45	20.116	4.999	100.57	91.89	**91.99**	88.00	89.00	**PASS**
	75	82.16	20.122	3.749	75.44	91.82				
	50	54.48	20.120	2.500	50.29	92.31				
	25	27.34	20.118	1.250	25.14	91.95				
	10	11.23	20.109	0.500	10.05	**89.45**			79.00	**PASS**
230	100	107.68	20.103	4.999	100.50	93.33	**93.35**	88.00	89.00	**PASS**
	75	80.89	20.108	3.749	75.39	93.20				
	50	53.65	20.107	2.500	50.26	93.68				
	25	26.96	20.103	1.250	25.12	93.18				
	10	11.08	20.094	0.500	10.04	**90.59**			79.00	**PASS**

13.4 *Efficiency Across Line at 100% Load (On Board)*

13.4.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 132 VAC, 180 VAC, 230 VAC, 265 VAC
Output Voltage	5 V, 9 V, 12 V, 15 V, 20 V
Output Load	100%
Soak Time per Line	10 minutes
Output Voltage Measurement	On-Board

13.4.2 Test Results

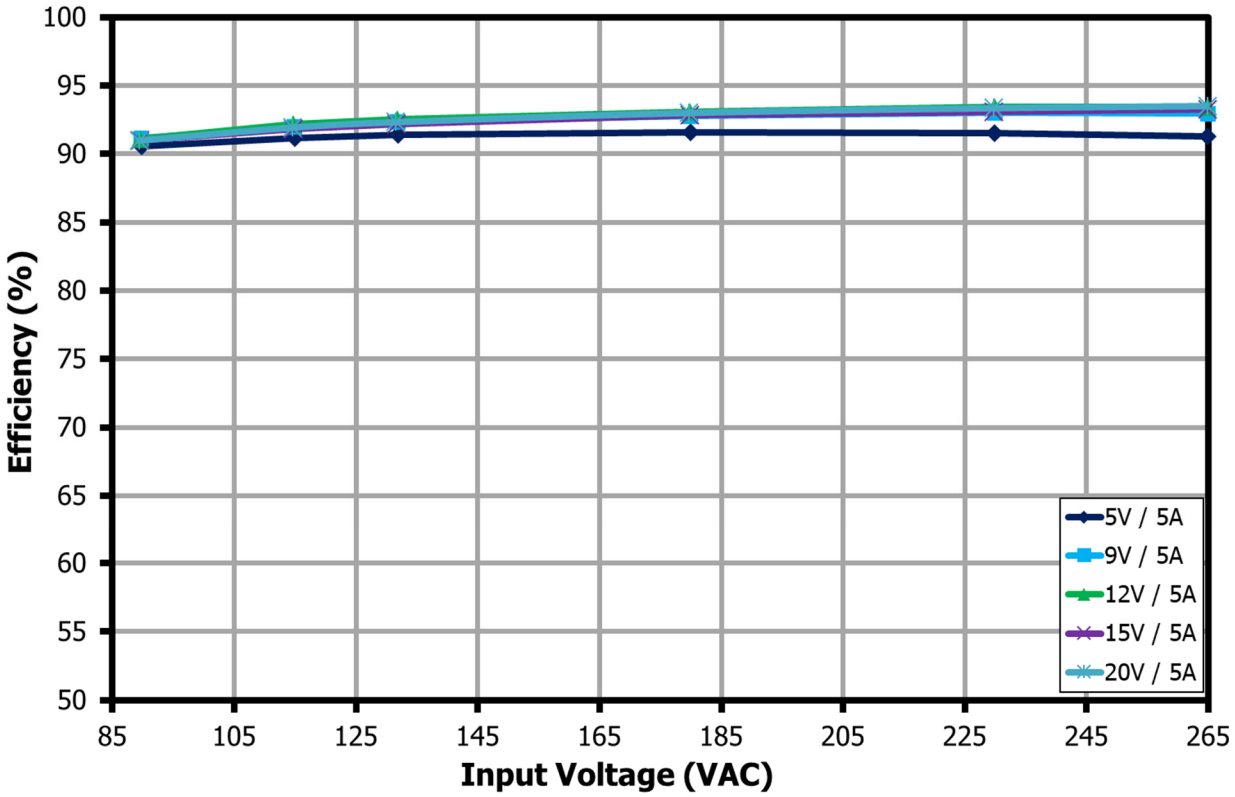


Figure 18 – Full Load Efficiency vs. Input Line for 5 V, 9 V, 12 V, 15 V, and 20 V Output, Room Temperature.

13.5 *Efficiency Across Load (On Board)*

Note: 1. The PFC bias circuit has been configured to operate as discussed in Section 4.2. Improvement in efficiency is expected for operating conditions wherein the PFC stage is disabled.

13.5.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 230 VAC, 265 VAC
Output Voltage	5 V, 9 V, 12 V, 15 V, 20 V
Output Load	10% - 100%
Soak Time per Line	10 minutes
Delay Time per Load	1 minute
Output Voltage Measurement	On-Board

13.5.2 Test Results

13.5.2.1 Output: 5 V / 5 A

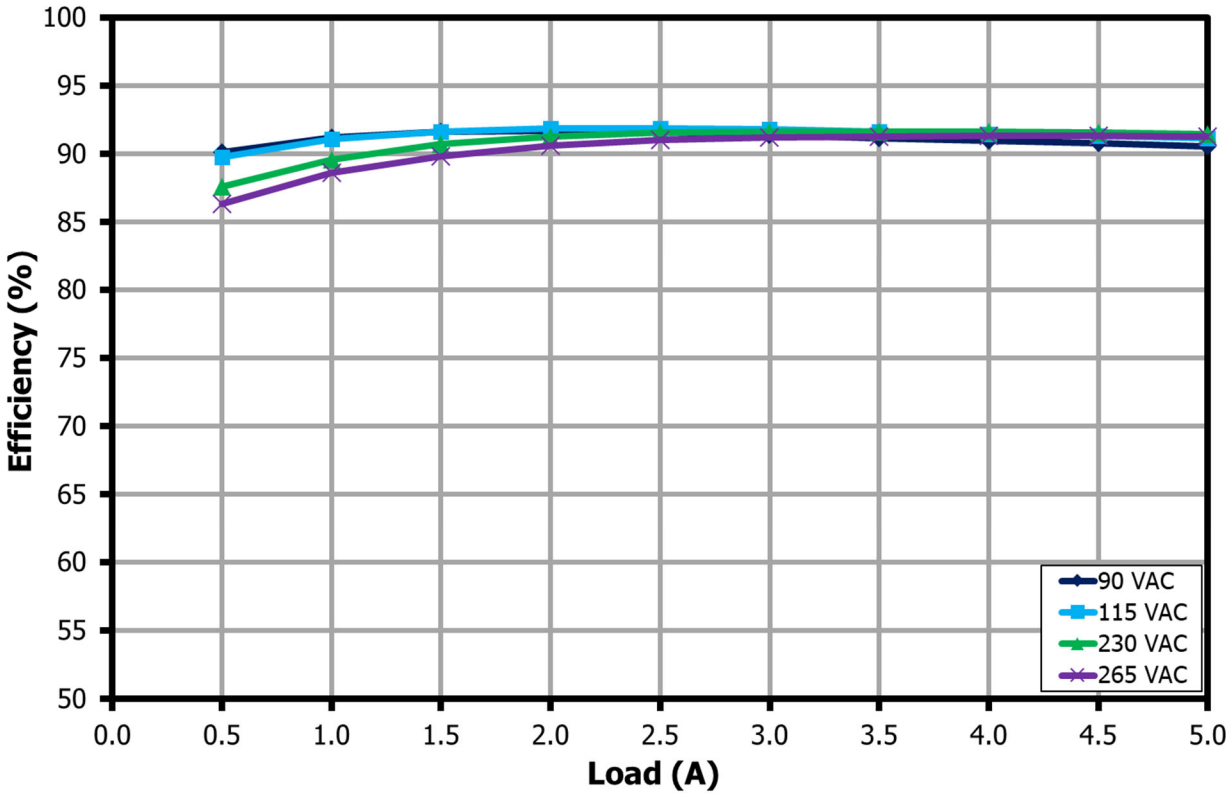


Figure 19 – Efficiency vs. Load for 5 V Output, Room Temperature.

13.5.2.2 Output: 9 V / 5 A

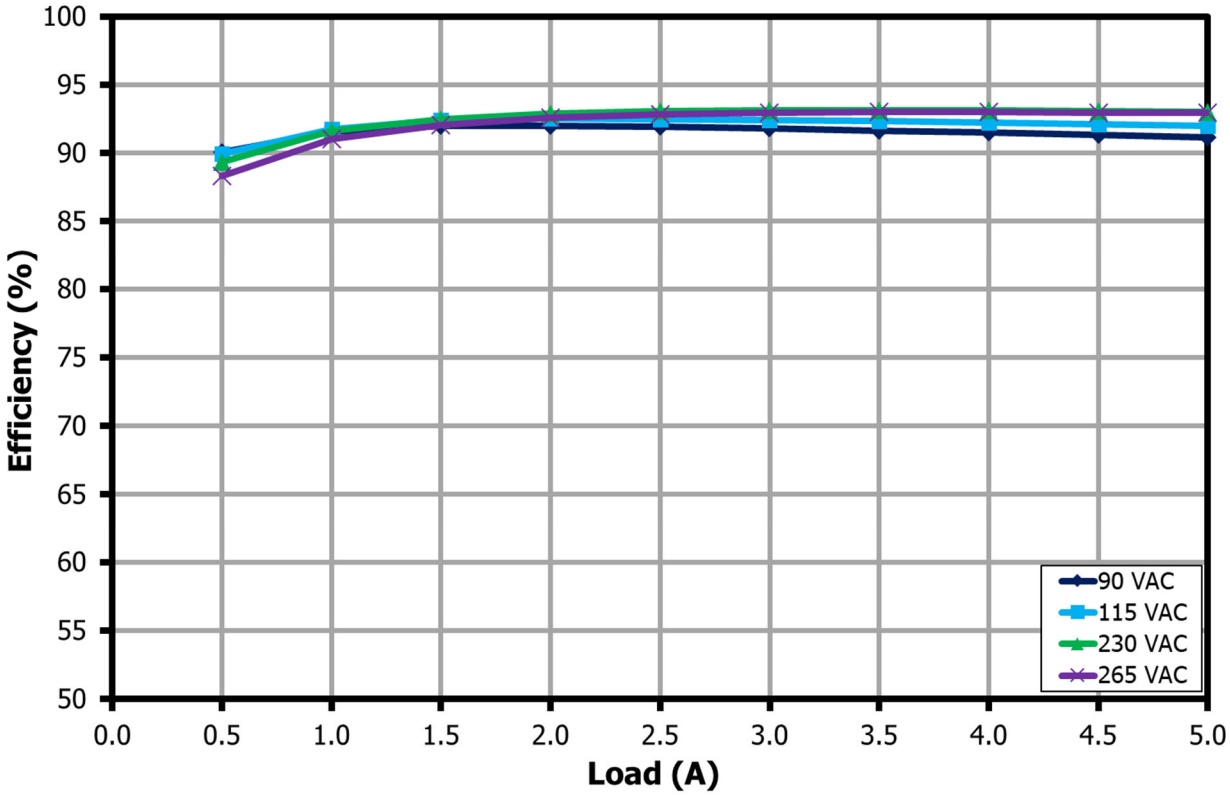


Figure 20 – Efficiency vs. Load for 9 V Output, Room Temperature.

13.5.2.3 Output: 12 V / 5 A

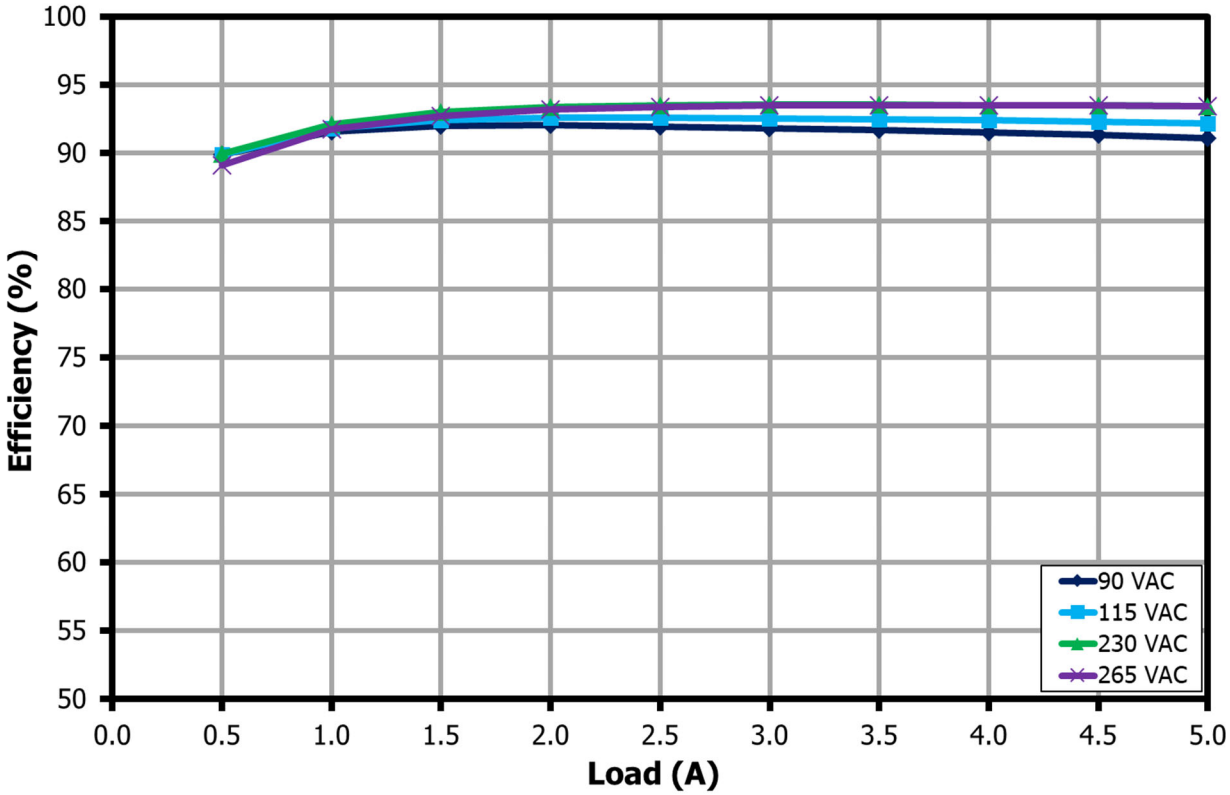


Figure 21 – Efficiency vs. Load for 12 V Output, Room Temperature.

13.5.2.4 Output: 15 V / 5 A

13.5.2.4.1 Output: 15 V / 5 A (90 VAC)

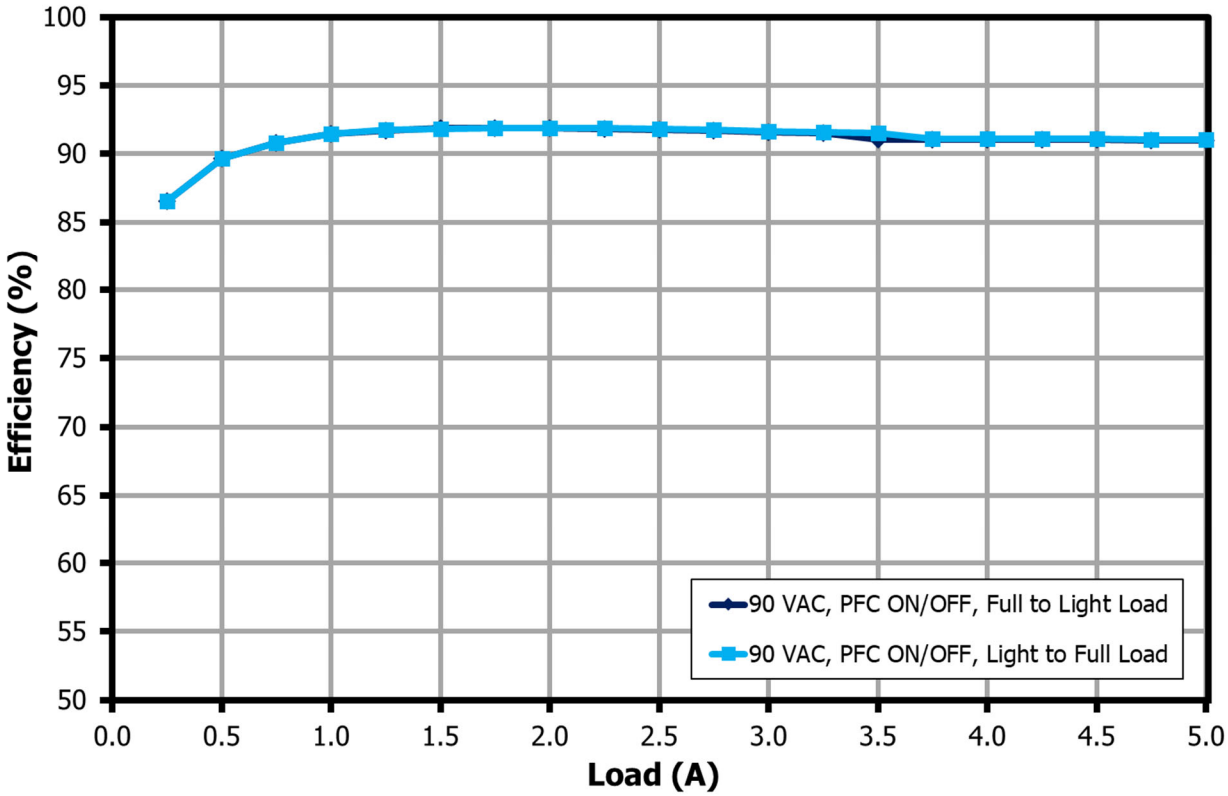


Figure 22 – Efficiency vs. Load for 15 V Output, 90 VAC, Room Temperature.

13.5.2.4.2 Output: 15 V / 5 A (115 VAC)

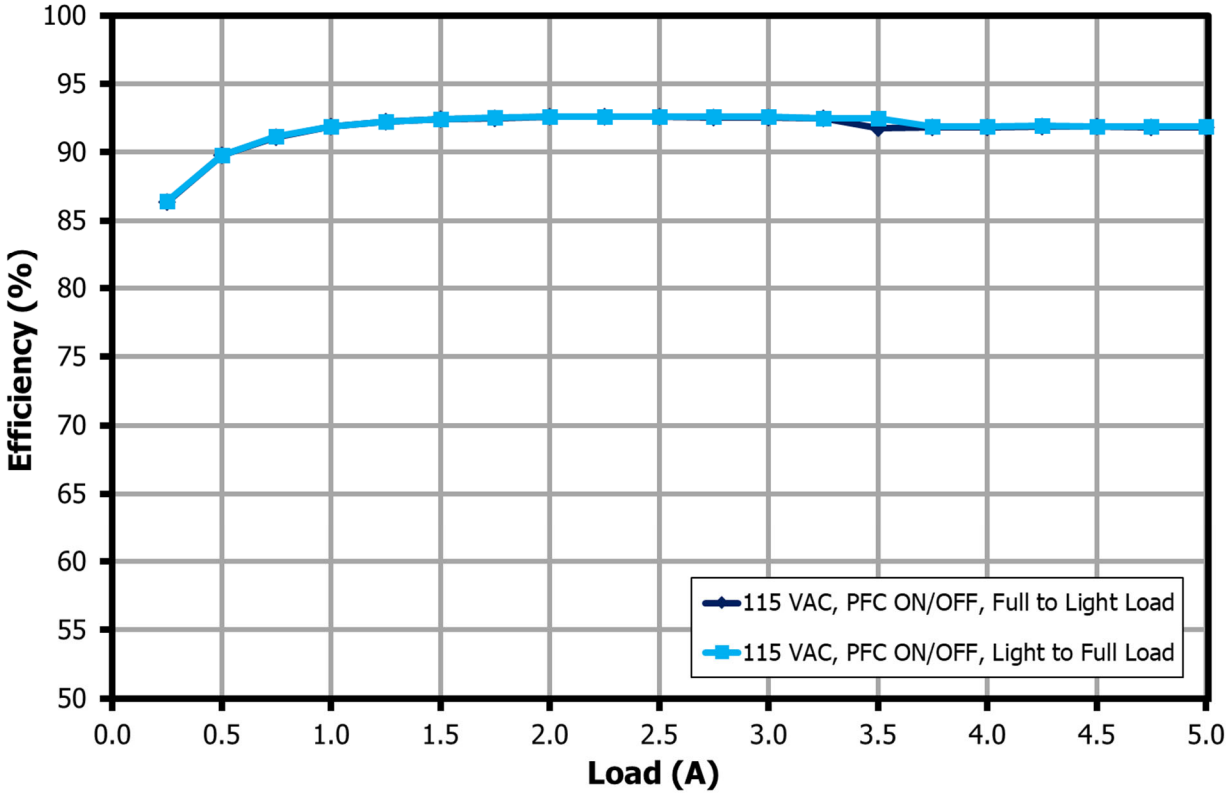


Figure 23 – Efficiency vs. Load for 15 V Output, 115 VAC, Room Temperature.

13.5.2.4.3 Output: 15 V / 5 A (230 VAC)

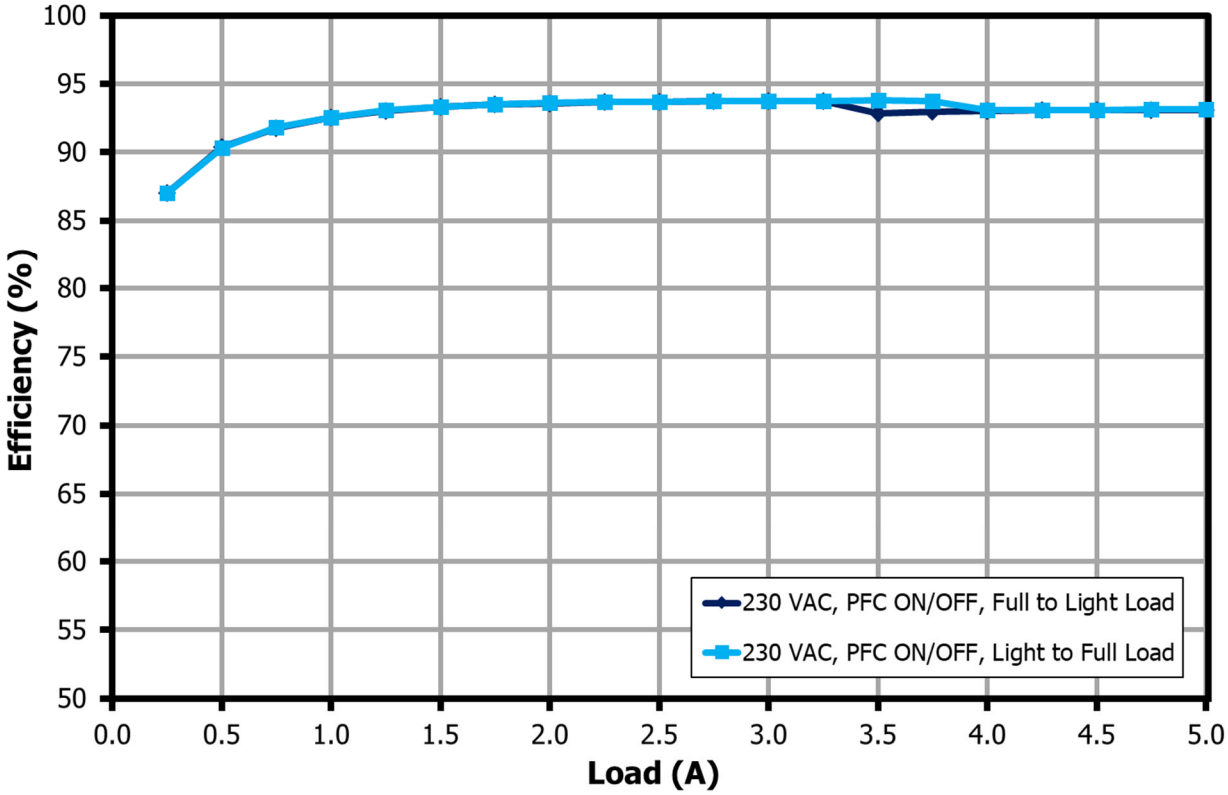


Figure 24 – Efficiency vs. Load for 15 V Output, 230 VAC, Room Temperature.

13.5.2.4.4 Output: 15 V / 5 A (265 VAC)

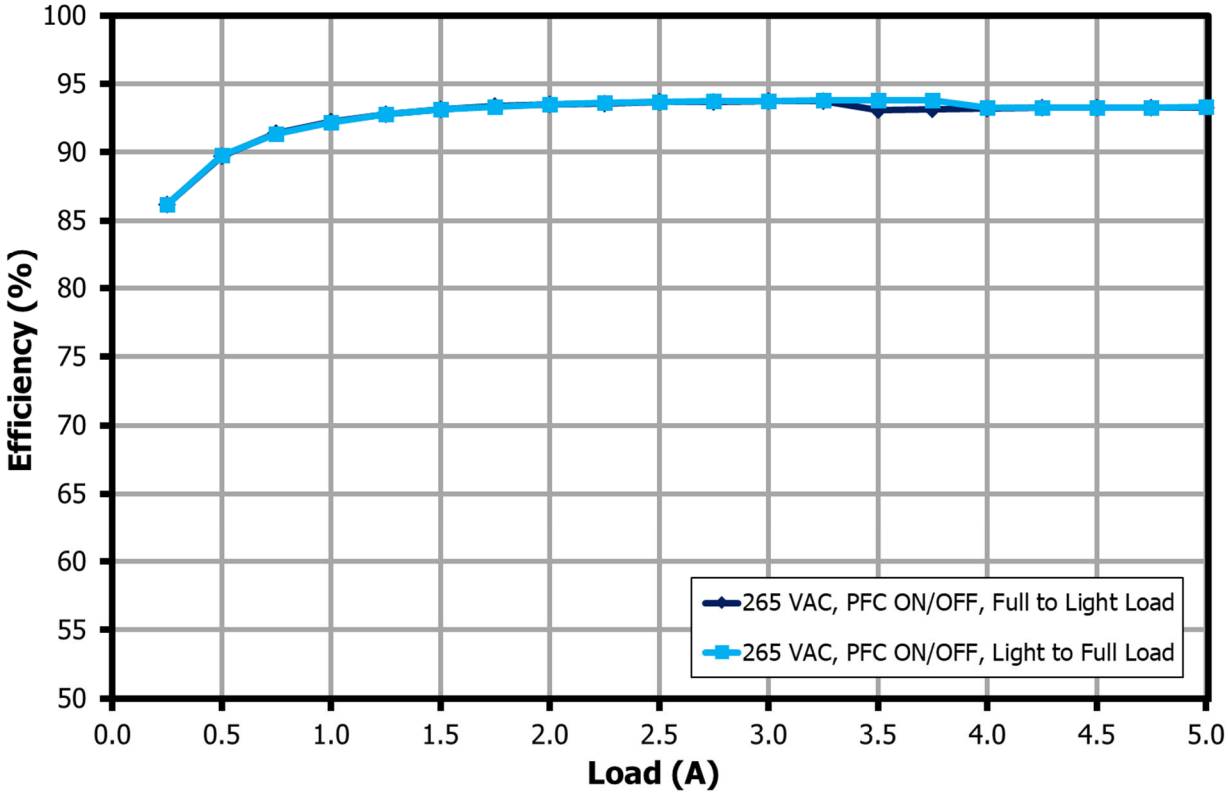


Figure 25 – Efficiency vs. Load for 15 V Output, 265 VAC, Room Temperature.

13.5.2.5 Output: 20 V / 5 A

13.5.2.5.1 Output: 20 V / 5 A (90 VAC)

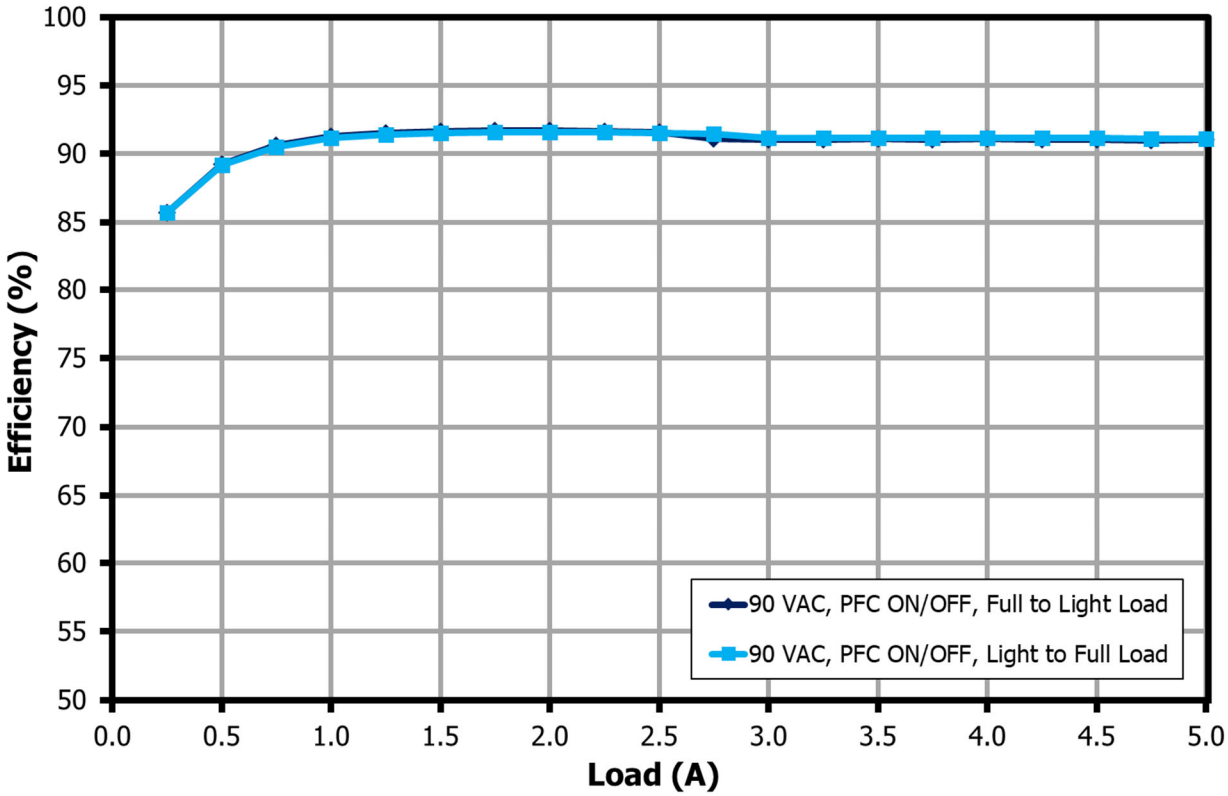


Figure 26 – Efficiency vs. Load for 20 V Output, 90 VAC, Room Temperature.

13.5.2.5.2 Output: 20 V / 5 A (115 VAC)

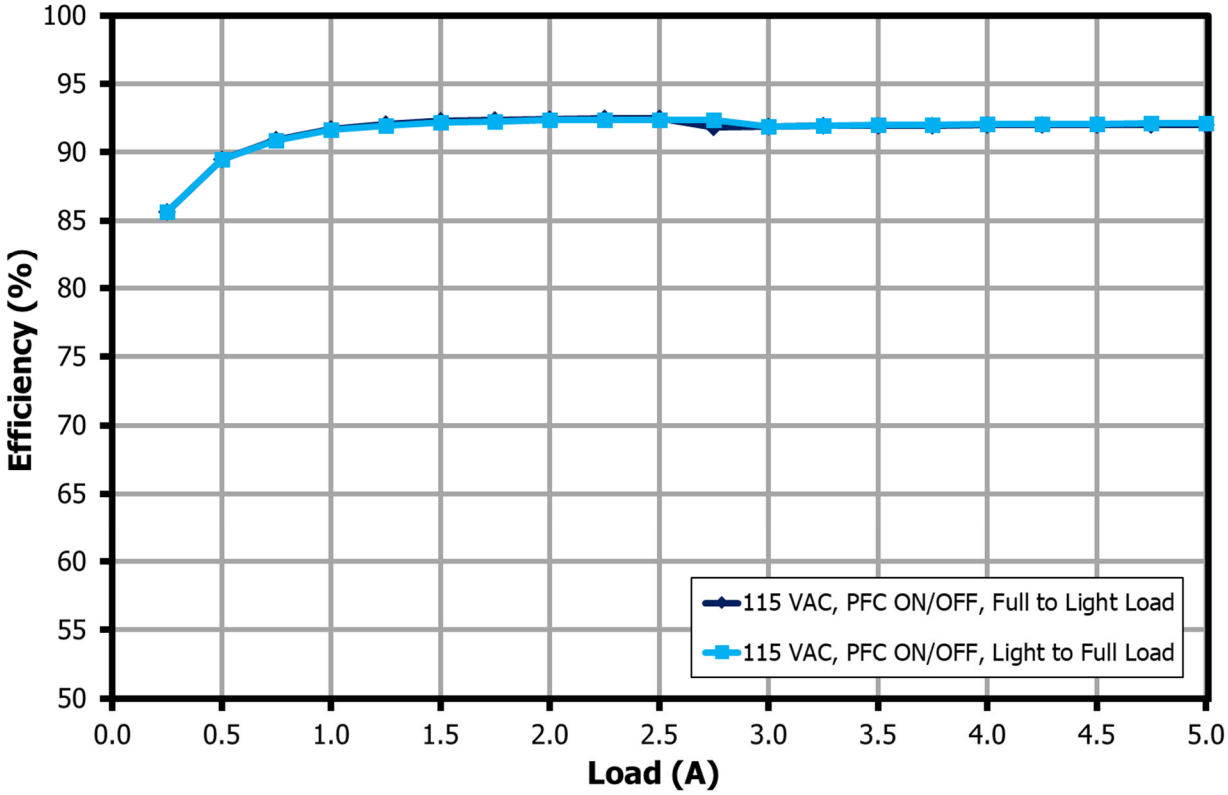


Figure 27 – Efficiency vs. Load for 20 V Output, 115 VAC, Room Temperature.

13.5.2.5.3 Output: 20 V / 5 A (230 VAC)

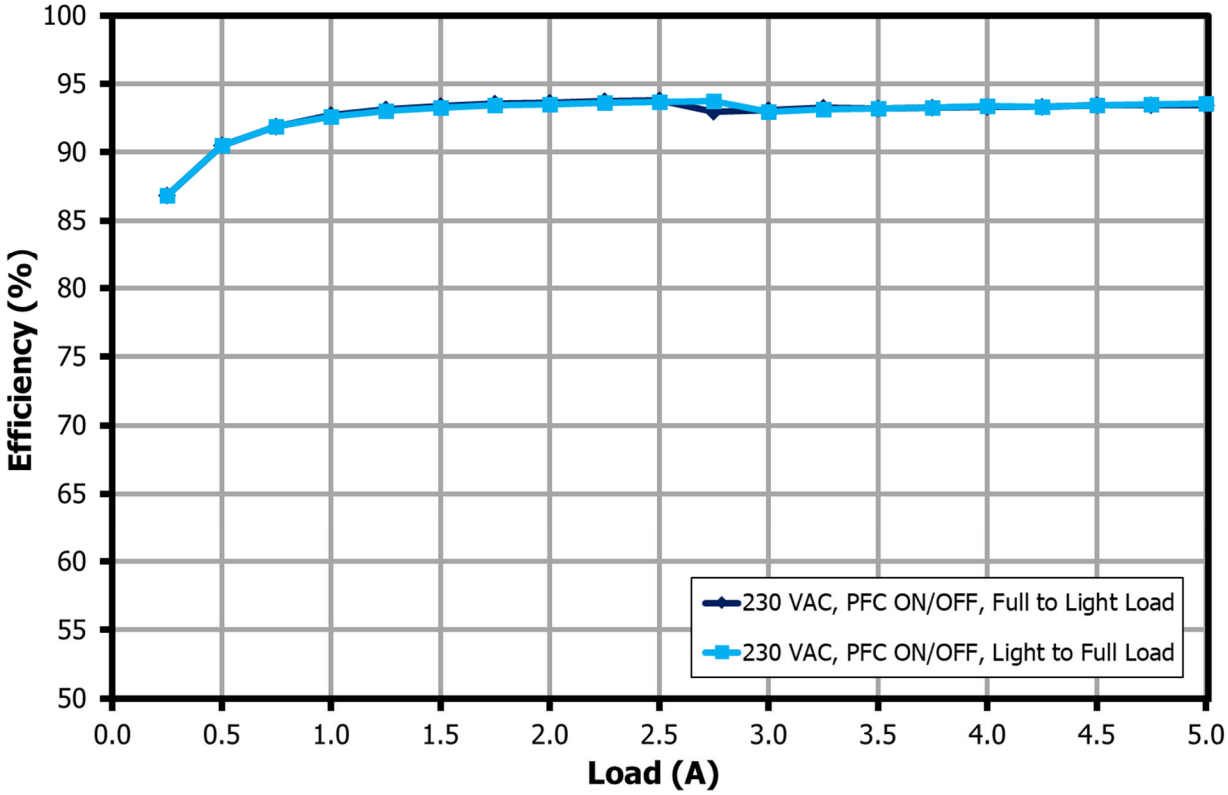


Figure 28 – Efficiency vs. Load for 20 V Output, 230 VAC, Room Temperature.

13.5.2.5.4 Output: 20 V / 5 A (265 VAC)

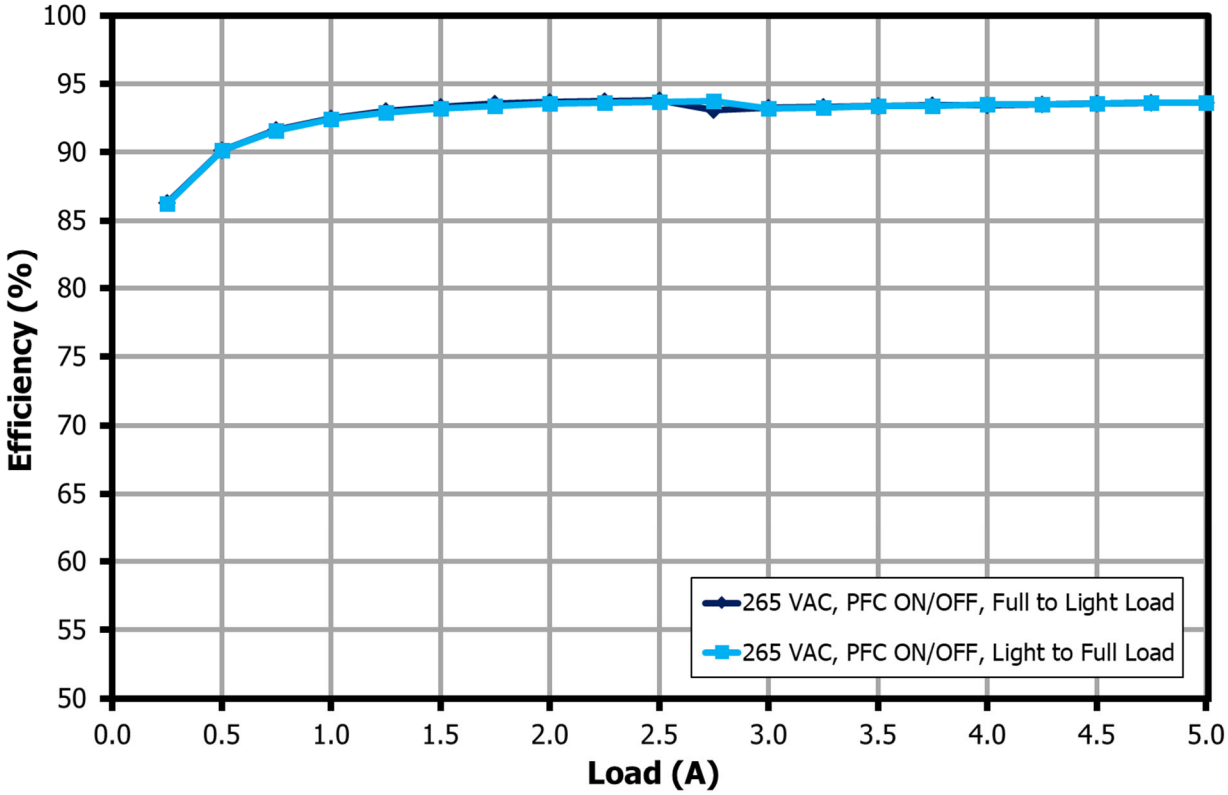


Figure 29 – Efficiency vs. Load for 20 V Output, 265 VAC, Room Temperature.

13.6 *Load Regulation (On Board)*

13.6.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 230 VAC, 265 VAC
Output Voltage	5 V, 9 V, 12 V, 15 V, 20 V
Output Load	0% - 100%
Soak Time per Line	10 minutes
Delay Time per Load	1 minute
Output Voltage Measurement	On-Board

13.6.2 Test Results

13.6.2.1 Output: 5 V / 5 A

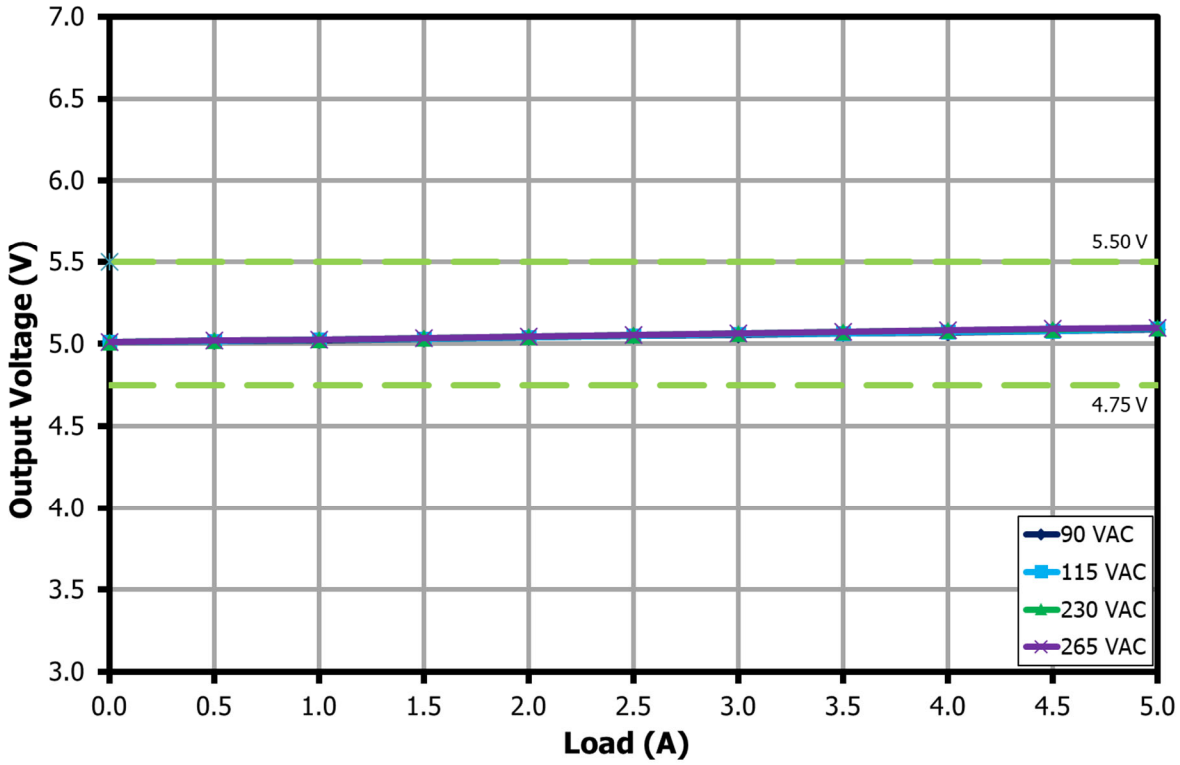


Figure 30 – Output Voltage vs. Output Load for 5 V Output, Room Temperature.

Note: USB PD Specification defines vSafe5V (4.75 V to 5.5 V, measured on-board) as the allowable VBUS Voltage range at 5 V operation.

13.6.2.2 Output: 9 V / 5 A

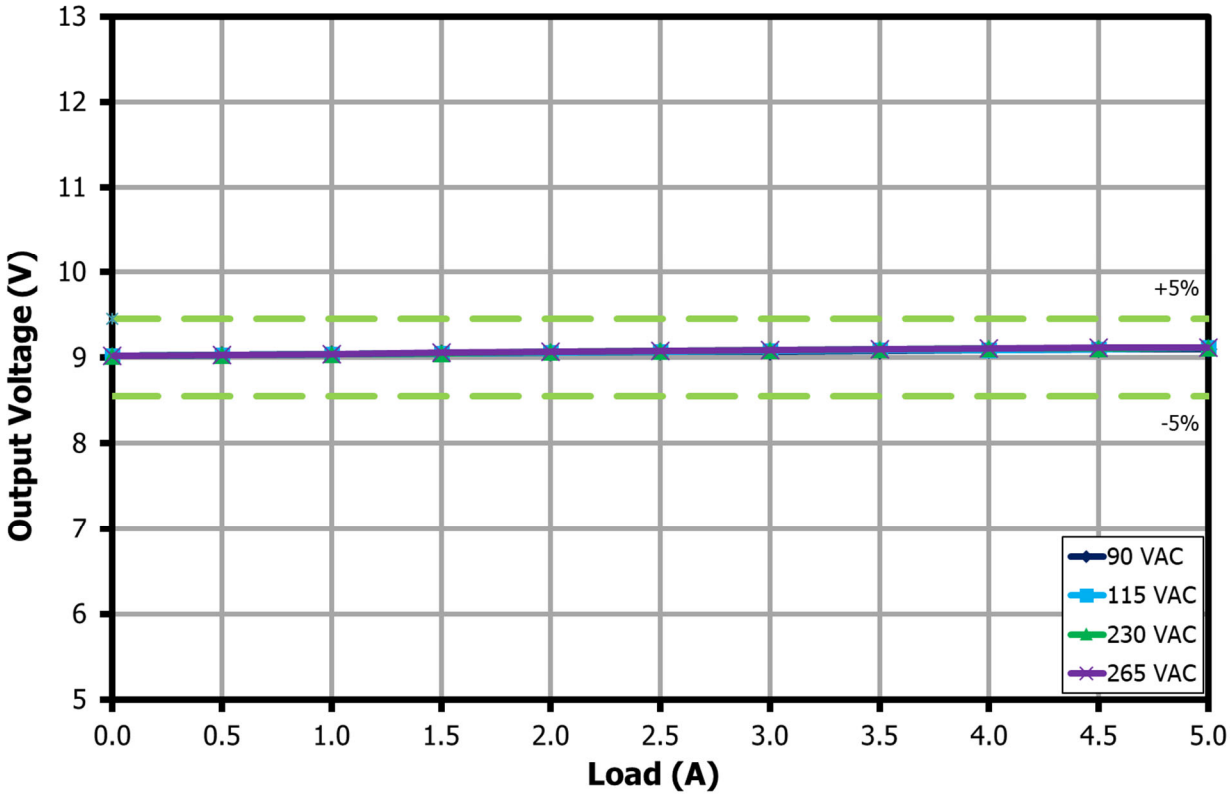


Figure 31 – Output Voltage vs. Output Load for 9 V Output, Room Temperature.

13.6.2.3 Output: 12 V / 5 A

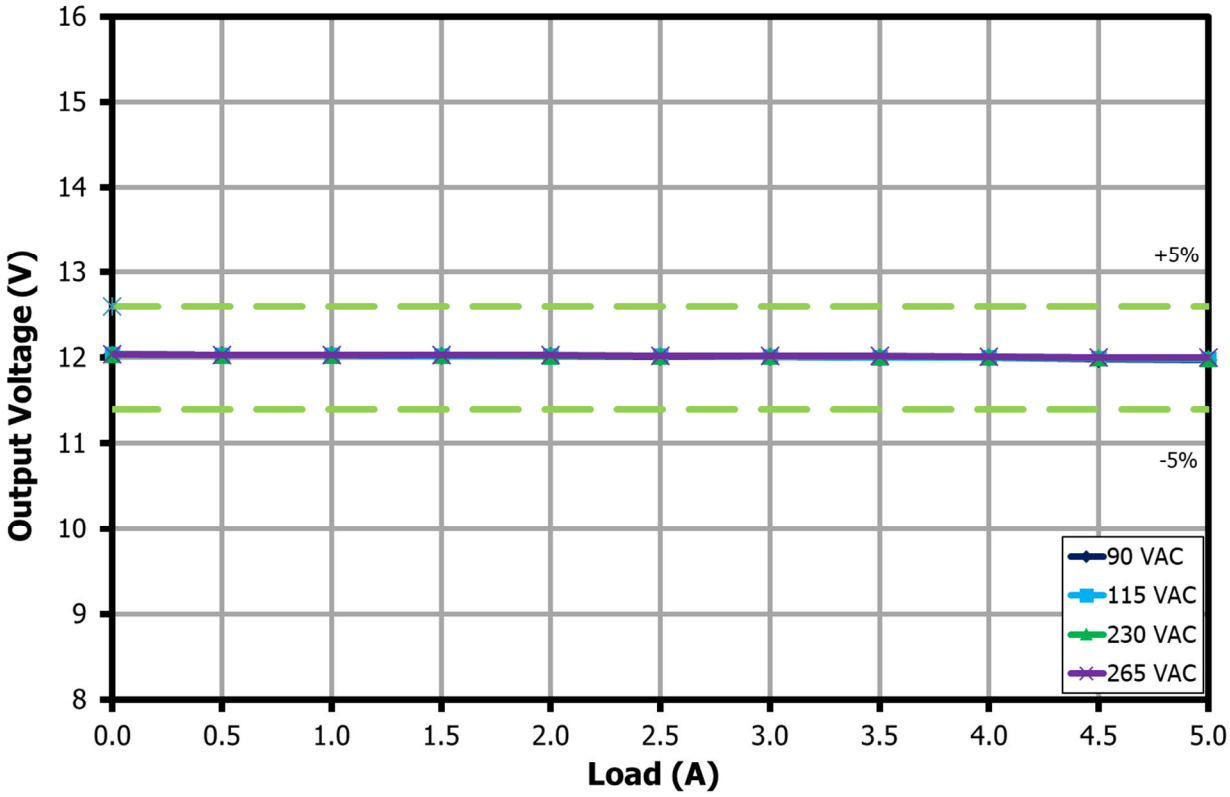


Figure 32 – Output Voltage vs. Output Load for 12 V Output, Room Temperature.

13.6.2.4 Output: 15 V / 5 A

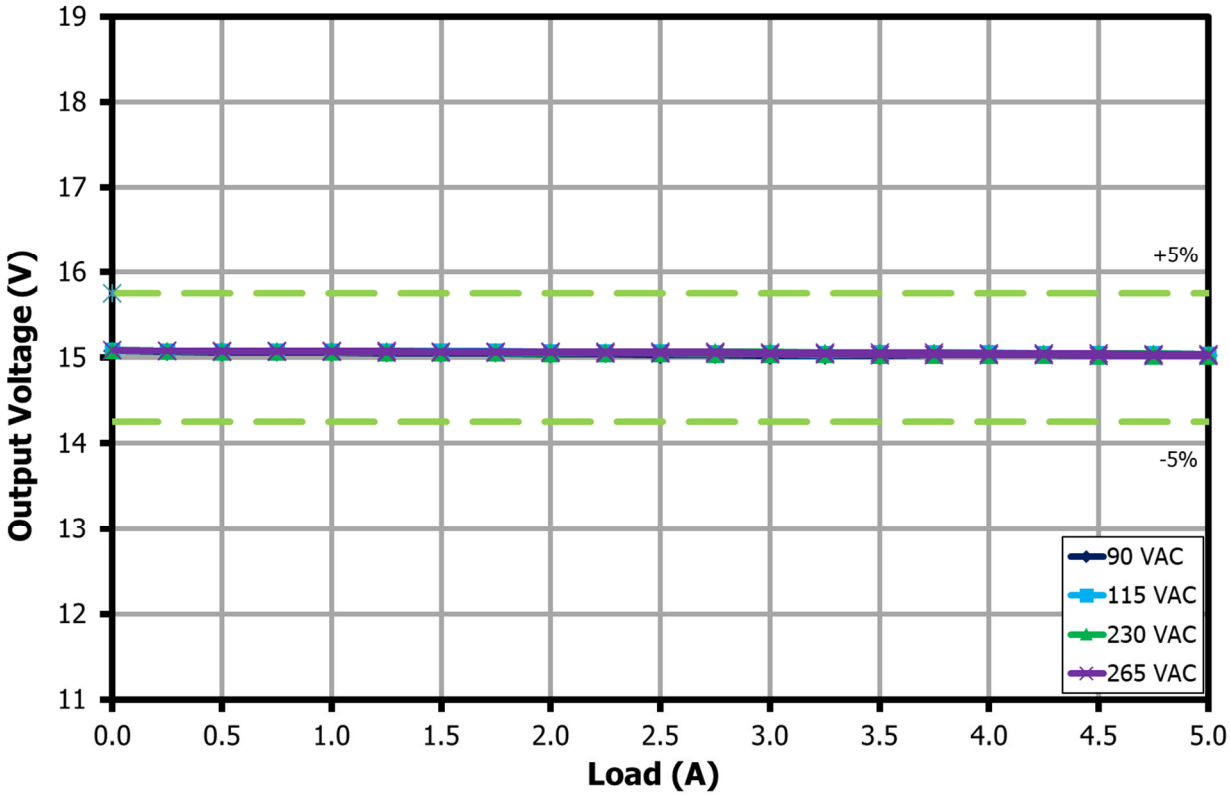


Figure 33 – Output Voltage vs. Output Load for 15 V Output, Room Temperature.

13.6.2.5 Output: 20 V / 5 A

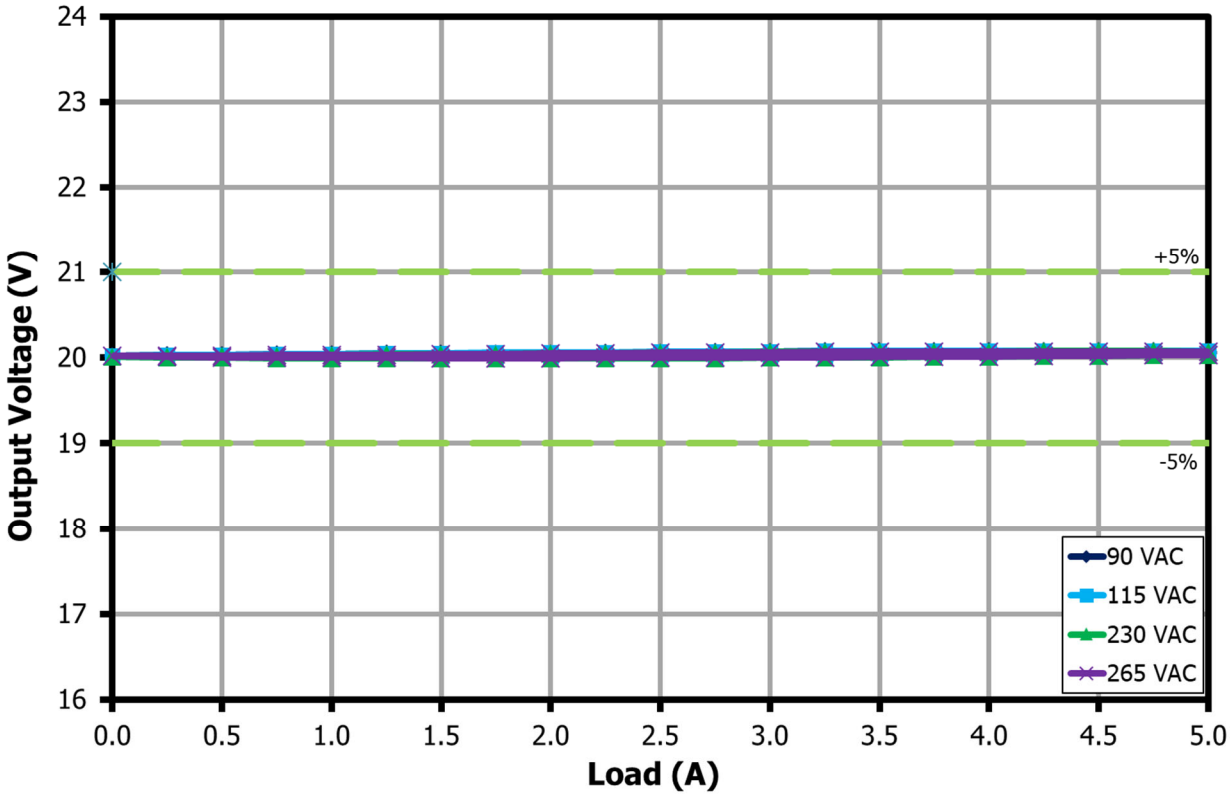


Figure 34 – Output Voltage vs. Output Load for 20 V Output, Room Temperature.

13.7 *Line Regulation (On Board)*

13.7.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 132 VAC, 180 VAC, 230 VAC, 265 VAC
Output Voltage	5 V, 9 V, 12 V, 15 V, 20 V
Output Load	50%, 100%
Soak Time per Line	10 minutes
Output Voltage Measurement	On-Board

13.7.2 Test Results

13.7.2.1 Output: 5 V / 5 A

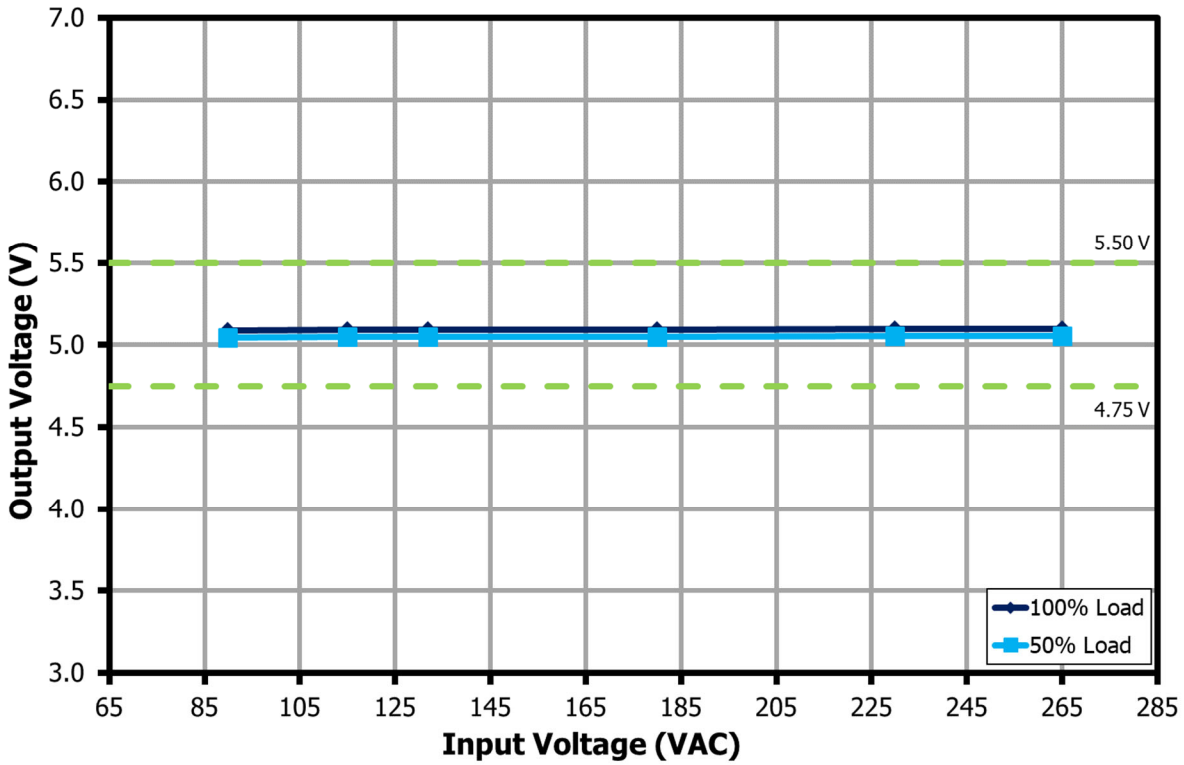


Figure 35 – Output Voltage vs. Input Line Voltage for 5 V Output, Room Temperature.

Note: USB PD Specification defines vSafe5V (4.75 V to 5.5 V, measured on-board) as the allowable VBUS Voltage range at 5 V operation.

13.7.2.2 Output: 9 V / 5 A

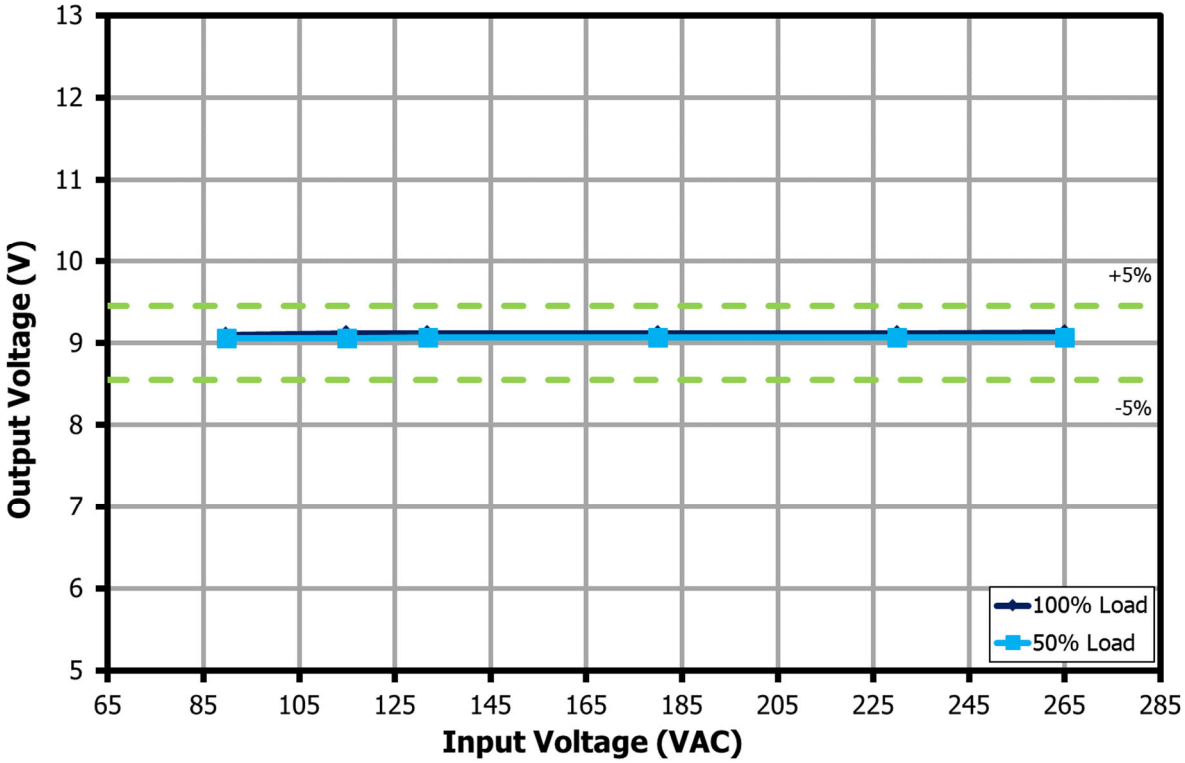


Figure 36 – Output Voltage vs. Input Line Voltage for 9 V Output, Room Temperature.

13.7.2.3 Output: 12 V / 5 A

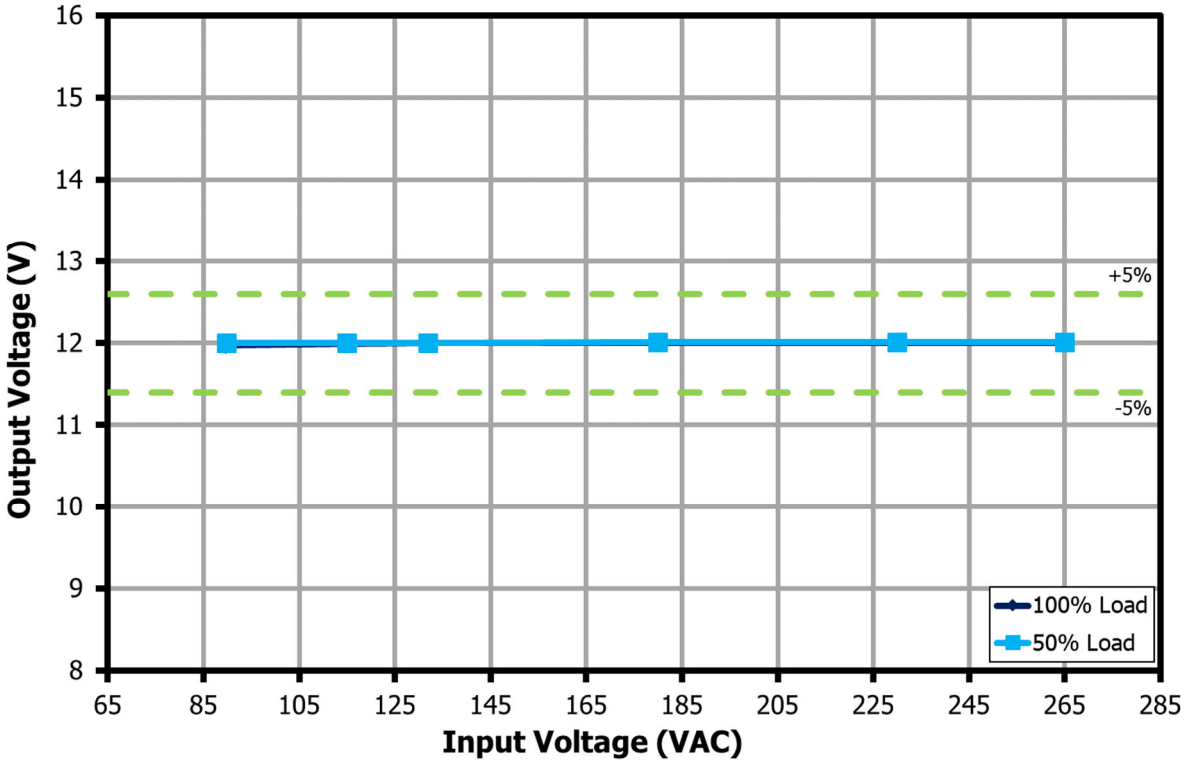


Figure 37 – Output Voltage vs. Input Line Voltage for 12 V Output, Room Temperature.

13.7.2.4 Output: 15 V / 5 A

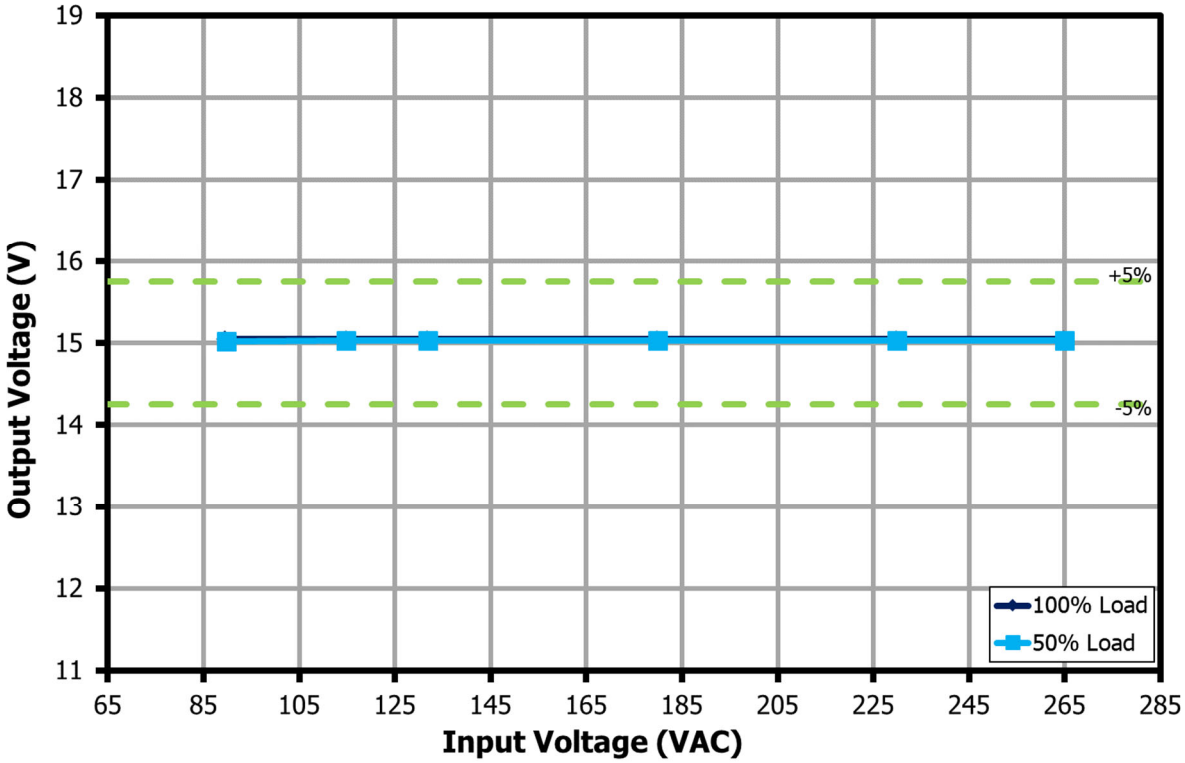


Figure 38 – Output Voltage vs. Input Line Voltage for 15 V Output, Room Temperature.

13.7.2.5 Output: 20 V / 5 A

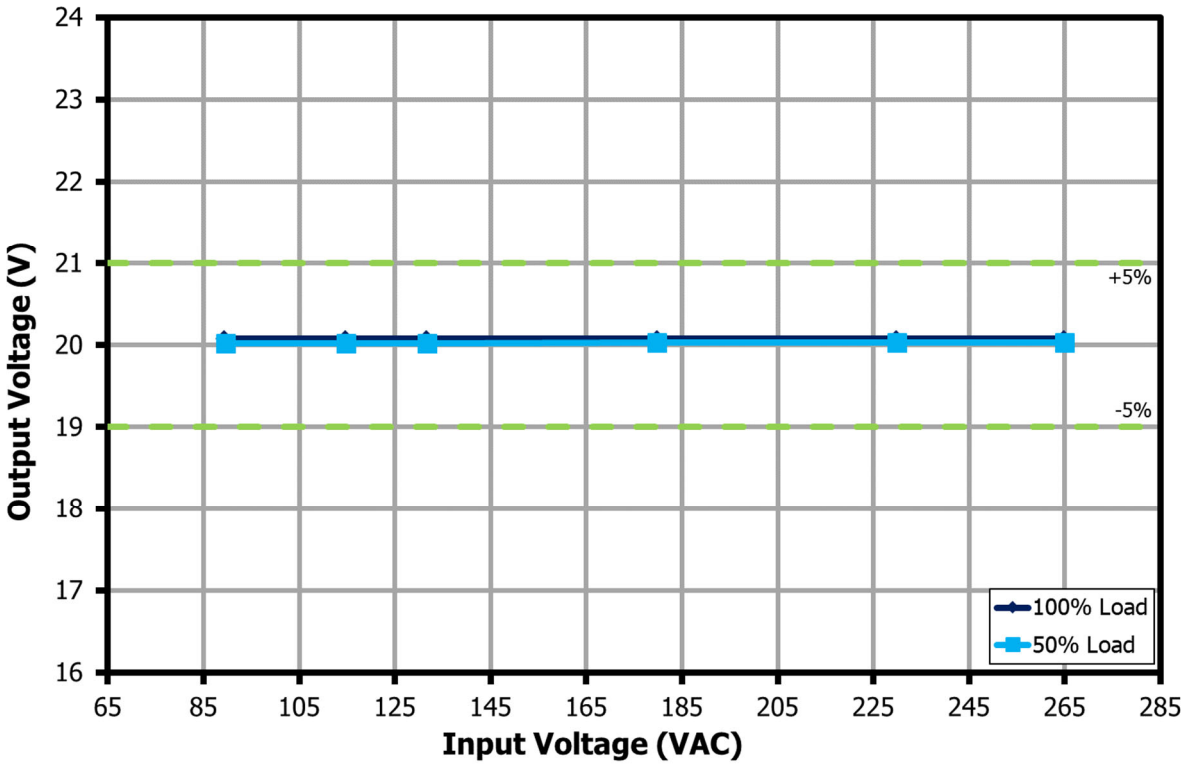


Figure 39 – Output Voltage vs. Input Line Voltage for 20 V Output, Room Temperature.

13.8 *Input Current Harmonics*

13.8.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 115 VAC, 230 VAC, 265 VAC
Output Voltage	15 V, 20 V
Output Load	100%
Soak Time per Line	10 minutes
Output Voltage Measurement	On-Board

Note: Input current harmonics are checked for 15 V and 20 V at ≥ 75W operation in compliance with IEC/EN61000-3-2

13.8.2 Test Results

13.8.2.1 Output: 15 V / 5 A (90 VAC)

Input		Input Measurement					Output Measurement				
$VAC_{(RMS)}$	**Freq (Hz)**	**$V_{IN(RMS)}$**	**I_{IN} (mA)**	**P_{IN} (W)**	**PF**	**% THD**	**V_{OUT} (V)**	**I_{OUT} (mA)**	**P_{OUT} (W)**	**%V Reg**	**Efficiency (%)**
90	60	89.45	944.50	82.58	0.98	15.38	15.04	5000.00	75.21	0.28	91.07

Harmonic Order	Harmonic Content (mA)	Class D Limit (mA/W)	Class D Limit (mA)	Remarks
1	923.90			
3	121.10	3.40	281.25	Pass
5	59.70	1.90	157.17	Pass
7	38.90	1.00	82.72	Pass
9	19.60	0.50	41.36	Pass
11	19.70	0.35	28.95	Pass
13	8.70	0.30	24.50	Pass
15	8.40	0.26	21.23	Pass
17	6.10	0.23	18.73	Pass
19	6.00	0.20	16.76	Pass
21	1.40	0.18	15.17	Pass
23	1.80	0.17	13.85	Pass
25	2.40	0.15	12.74	Pass
27	3.50	0.14	11.80	Pass
29	4.20	0.12	10.98	Pass
31	4.00	0.12	10.27	Pass
33	4.50	0.12	9.65	Pass
35	3.70	0.11	9.10	Pass
37	4.20	0.10	8.61	Pass
39	4.50	0.10	8.17	Pass

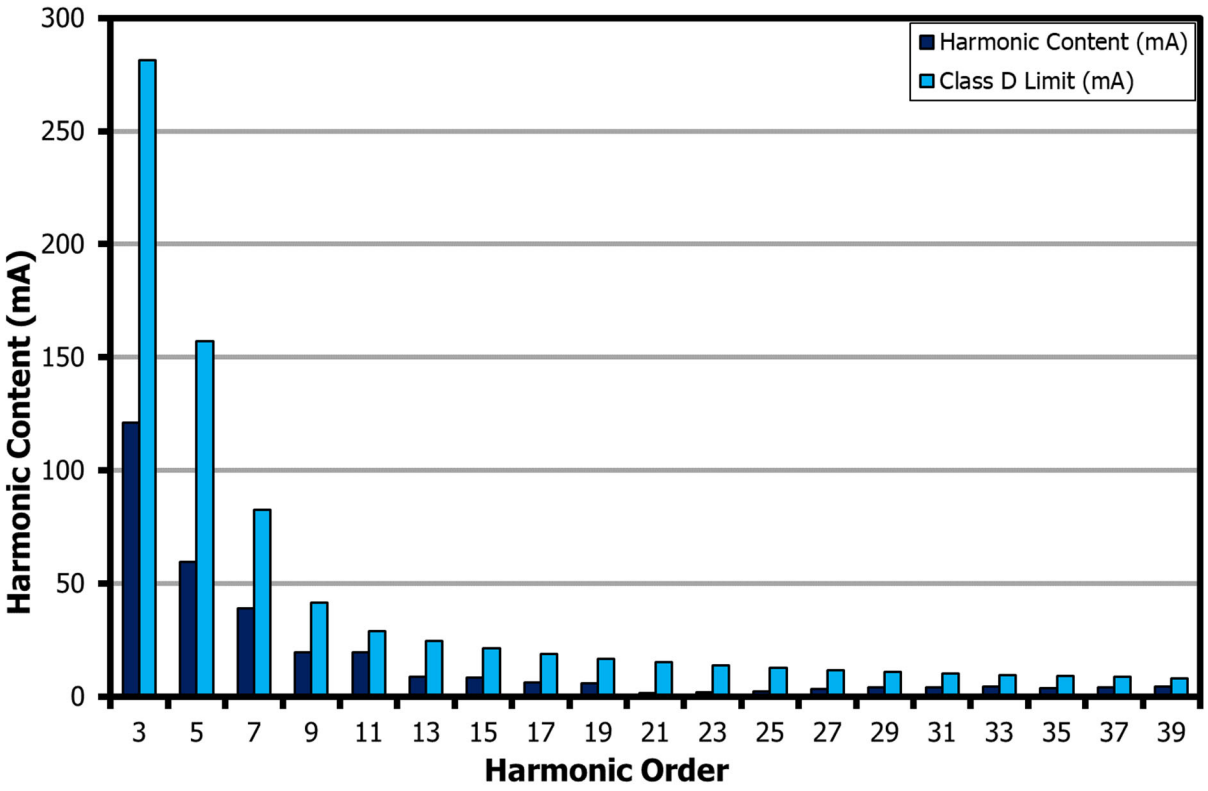


Figure 40 – Input Current Harmonics for 15 V Output, 5 A Load, 90 VAC, Room Temperature.

13.8.2.2 Output: 15 V / 5 A (115 VAC)

Input		Input Measurement					Output Measurement				
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN(RMS)}$	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
115	60	114.64	734.40	82.08	0.97	17.09	15.05	4999.90	75.27	0.35	91.70

Harmonic Order	Harmonic Content (mA)	Class D Limit (mA/W)	Class D Limit (mA)	Remarks
1	720.6			
3	100.80	3.40	279.07	Pass
5	51.10	1.90	155.95	Pass
7	28.50	1.00	82.08	Pass
9	22.10	0.50	41.04	Pass
11	14.80	0.35	28.73	Pass
13	10.60	0.30	24.31	Pass
15	8.80	0.26	21.07	Pass
17	8.50	0.23	18.59	Pass
19	7.30	0.20	16.63	Pass
21	5.30	0.18	15.05	Pass
23	3.90	0.17	13.74	Pass
25	2.70	0.15	12.64	Pass
27	3.00	0.14	11.70	Pass
29	2.30	0.12	10.90	Pass
31	1.20	0.12	10.19	Pass
33	2.30	0.12	9.58	Pass
35	1.20	0.11	9.03	Pass
37	2.00	0.10	8.54	Pass
39	7.60	0.10	8.10	Pass

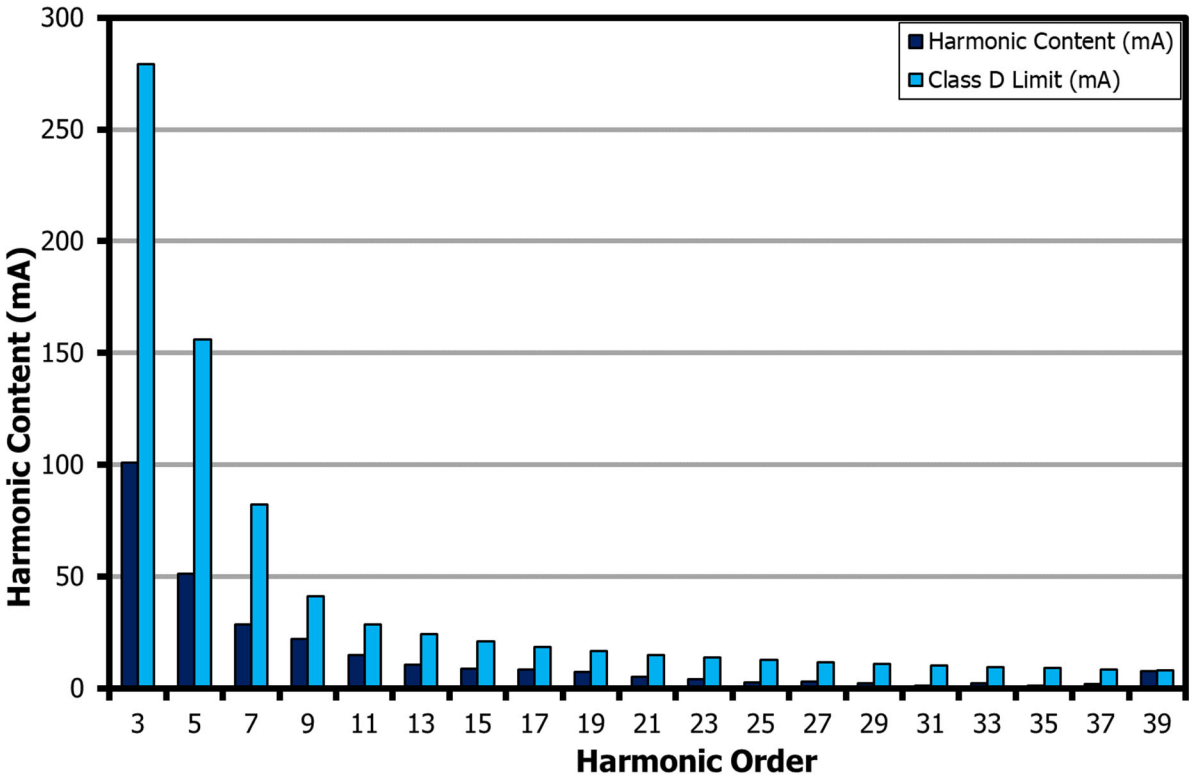


Figure 41 – Input Current Harmonics for 15 V Output, 5 A Load, 115 VAC, Room Temperature.

13.8.2.3 Output: 15 V / 5 A (230 VAC)

Input		Input Measurement					Output Measurement				
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN(RMS)}$	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
230	50	229.77	370.88	80.96	0.95	14.92	15.05	4999.90	75.27	0.35	92.97

Harmonic Order	Harmonic Content (mA)	Class D Limit (mA/W)	Class D Limit (mA)	Remarks
1	349.58			
3	45.18	3.40	275.26	Pass
5	11.88	1.90	153.82	Pass
7	5.57	1.00	80.96	Pass
9	1.26	0.50	40.48	Pass
11	2.79	0.35	28.34	Pass
13	2.80	0.30	23.98	Pass
15	5.05	0.26	20.78	Pass
17	4.89	0.23	18.34	Pass
19	4.84	0.20	16.41	Pass
21	4.05	0.18	14.84	Pass
23	4.47	0.17	13.55	Pass
25	2.78	0.15	12.47	Pass
27	2.22	0.14	11.54	Pass
29	0.06	0.12	10.75	Pass
31	3.29	0.12	10.05	Pass
33	0.95	0.12	9.45	Pass
35	3.12	0.11	8.91	Pass
37	1.44	0.10	8.42	Pass
39	2.39	0.10	7.99	Pass

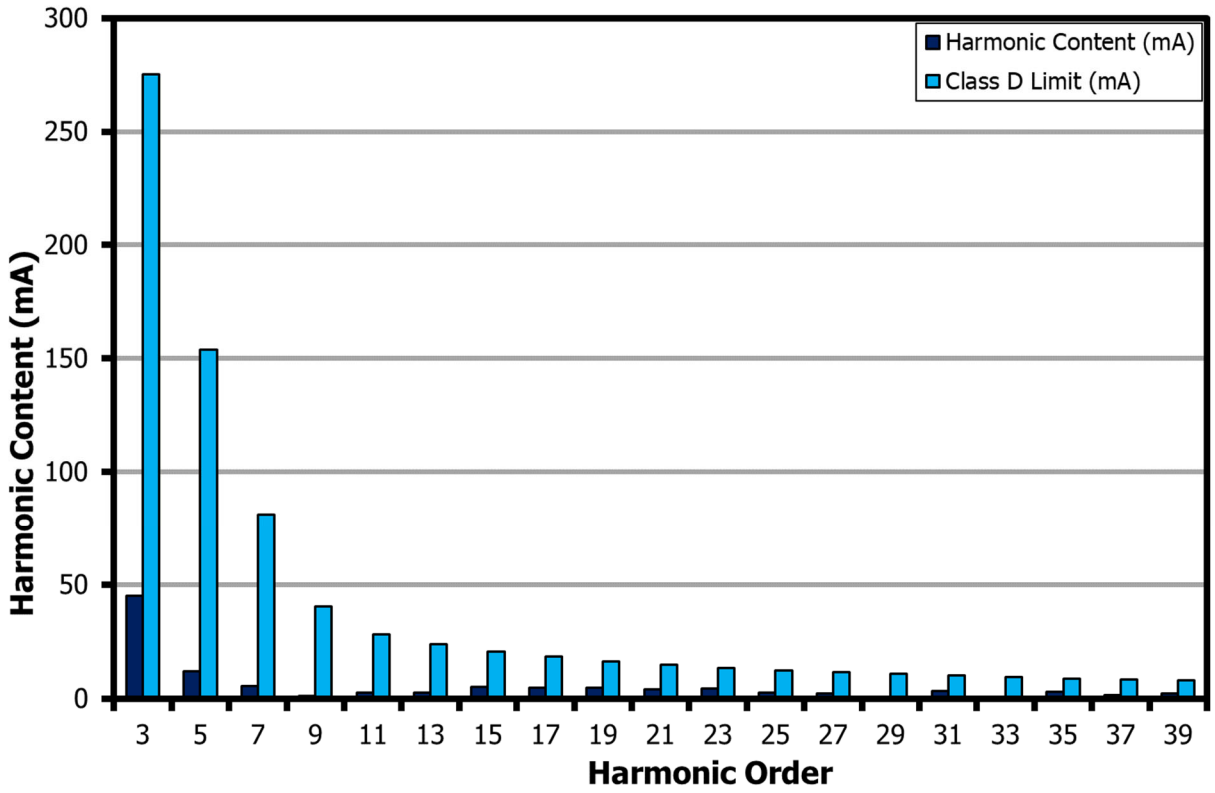


Figure 42 – Input Current Harmonics for 15 V Output, 5 A Load, 230 VAC, Room Temperature.

13.8.2.4 Output: 15 V / 5 A (265 VAC)

Input		Input Measurement					Output Measurement				
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN(RMS)}$	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
265	50	264.82	350.85	80.79	0.87	18.56	15.05	5000.40	75.25	0.33	93.15

Harmonic Order	Harmonic Content (mA)	Class D Limit (mA/W)	Class D Limit (mA)	Remarks
1	309.58			
3	40.09	3.40	274.69	Pass
5	23.53	1.90	153.50	Pass
7	16.18	1.00	80.79	Pass
9	22.22	0.50	40.40	Pass
11	14.10	0.35	28.28	Pass
13	6.55	0.30	23.93	Pass
15	4.11	0.26	20.74	Pass
17	4.69	0.23	18.30	Pass
19	3.22	0.20	16.37	Pass
21	4.44	0.18	14.81	Pass
23	5.39	0.17	13.52	Pass
25	2.65	0.15	12.44	Pass
27	3.85	0.14	11.52	Pass
29	4.03	0.12	10.73	Pass
31	3.21	0.12	10.03	Pass
33	2.03	0.12	9.43	Pass
35	1.84	0.11	8.89	Pass
37	2.69	0.10	8.41	Pass
39	1.58	0.10	7.98	Pass

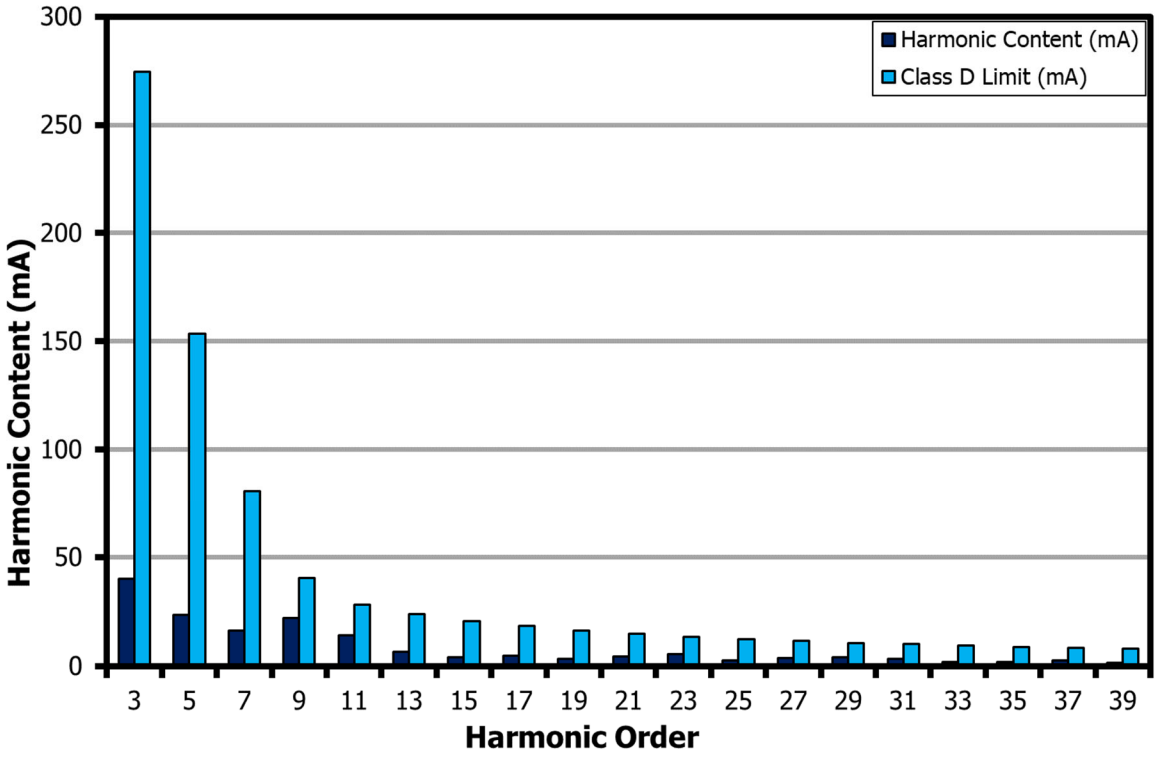


Figure 43 – Input Current Harmonics for 15 V Output, 5 A Load, 265 VAC, Room Temperature.

13.8.2.5 Output: 20 V / 5 A (90 VAC)

Input		Input Measurement					Output Measurement				
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN(RMS)}$	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
90	60	89.30	1248.40	110.02	0.99	11.35	20.07	5000.00	100.36	0.36	91.22

Harmonic Order	Harmonic Content (mA)	Class D Limit (mA/W)	Class D Limit (mA)	Remarks
1	1241.8			
3	116.50	3.40	375.80	Pass
5	64.70	1.90	210.01	Pass
7	35.40	1.00	110.53	Pass
9	21.50	0.50	55.27	Pass
11	13.00	0.35	38.69	Pass
13	11.70	0.30	32.73	Pass
15	7.90	0.26	28.37	Pass
17	6.00	0.23	25.03	Pass
19	3.00	0.20	22.40	Pass
21	1.80	0.18	20.26	Pass
23	3.70	0.17	18.50	Pass
25	3.80	0.15	17.02	Pass
27	4.80	0.14	15.76	Pass
29	3.40	0.12	14.67	Pass
31	5.60	0.12	13.73	Pass
33	5.50	0.12	12.90	Pass
35	4.30	0.11	12.16	Pass
37	4.80	0.10	11.50	Pass
39	4.20	0.10	10.91	Pass

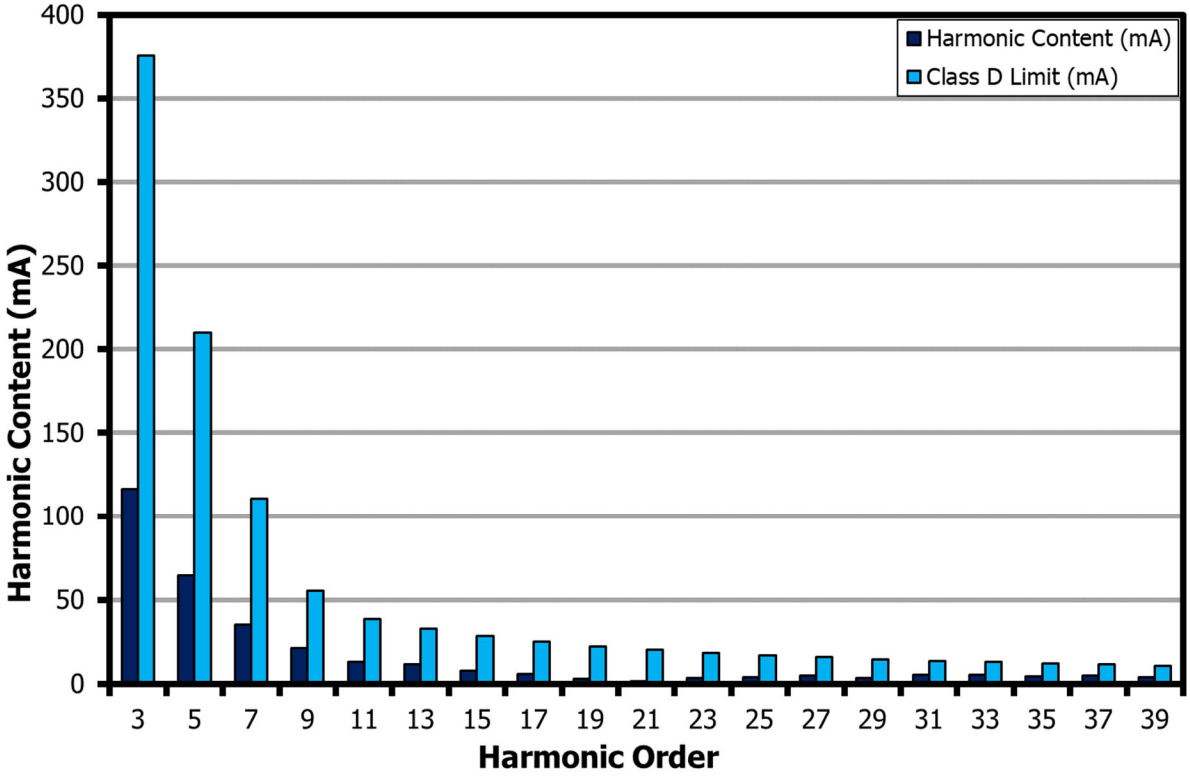


Figure 44 – Input Current Harmonics for 20 V Output, 5 A Load, 90 VAC, Room Temperature.

13.8.2.6 Output: 20 V / 5 A (115 VAC)

Input		Input Measurement					Output Measurement				
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN(RMS)}$	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
115	60	114.52	969.50	109.29	0.98	13.64	20.10	4999.80	100.49	0.49	91.95

Harmonic Order	Harmonic Content (mA)	Class D Limit (mA/W)	Class D Limit (mA)	Remarks
1	957.70			
3	106.70	3.40	371.59	Pass
5	57.70	1.90	207.65	Pass
7	32.10	1.00	109.29	Pass
9	24.00	0.50	54.65	Pass
11	17.10	0.35	38.25	Pass
13	11.90	0.30	32.37	Pass
15	8.00	0.26	28.05	Pass
17	6.50	0.23	24.75	Pass
19	5.10	0.20	22.15	Pass
21	3.60	0.18	20.04	Pass
23	2.70	0.17	18.29	Pass
25	3.30	0.15	16.83	Pass
27	2.50	0.14	15.58	Pass
29	2.00	0.12	14.51	Pass
31	1.50	0.12	13.57	Pass
33	1.80	0.12	12.75	Pass
35	1.60	0.11	12.02	Pass
37	1.80	0.10	11.37	Pass
39	9.40	0.10	10.79	Pass

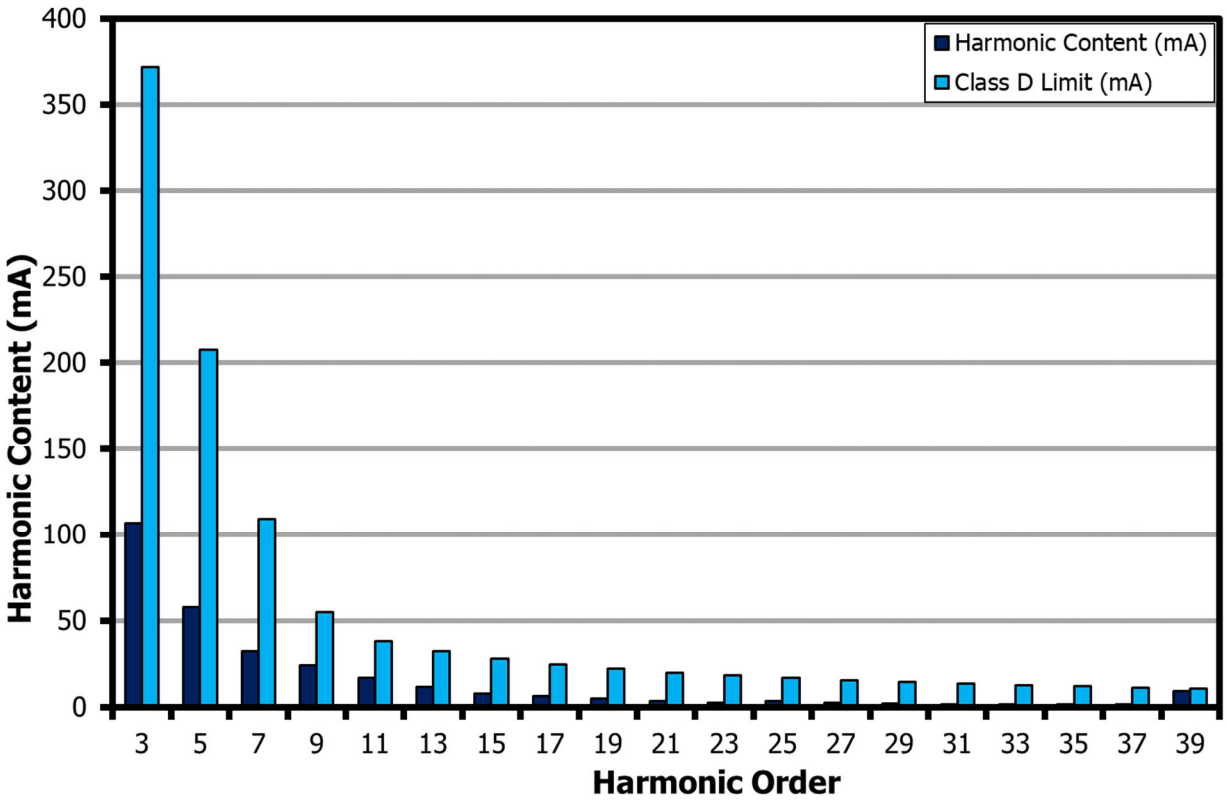


Figure 45 – Input Current Harmonics for 20 V Output, 5 A Load, 115 VAC, Room Temperature.

13.8.2.7 Output: 20 V / 5 A (230 VAC)

Input		Input Measurement					Output Measurement				
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN(RMS)}$	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
230	50	229.72	485.39	107.55	0.96	15.72	20.09	4999.80	100.46	0.46	93.41

Harmonic Order	Harmonic Content (mA)	Class D Limit (mA/W)	Class D Limit (mA)	Remarks
1	470.12			
3	66.28	3.40	365.67	Pass
5	20.35	1.90	204.35	Pass
7	11.00	1.00	107.55	Pass
9	5.67	0.50	53.78	Pass
11	6.76	0.35	37.64	Pass
13	6.11	0.30	31.85	Pass
15	8.37	0.26	27.60	Pass
17	8.48	0.23	24.36	Pass
19	7.33	0.20	21.79	Pass
21	8.88	0.18	19.72	Pass
23	4.35	0.17	18.00	Pass
25	8.89	0.15	16.56	Pass
27	3.75	0.14	15.34	Pass
29	8.19	0.12	14.28	Pass
31	4.66	0.12	13.36	Pass
33	3.67	0.12	12.55	Pass
35	5.83	0.11	11.83	Pass
37	4.81	0.10	11.19	Pass
39	2.77	0.10	10.62	Pass

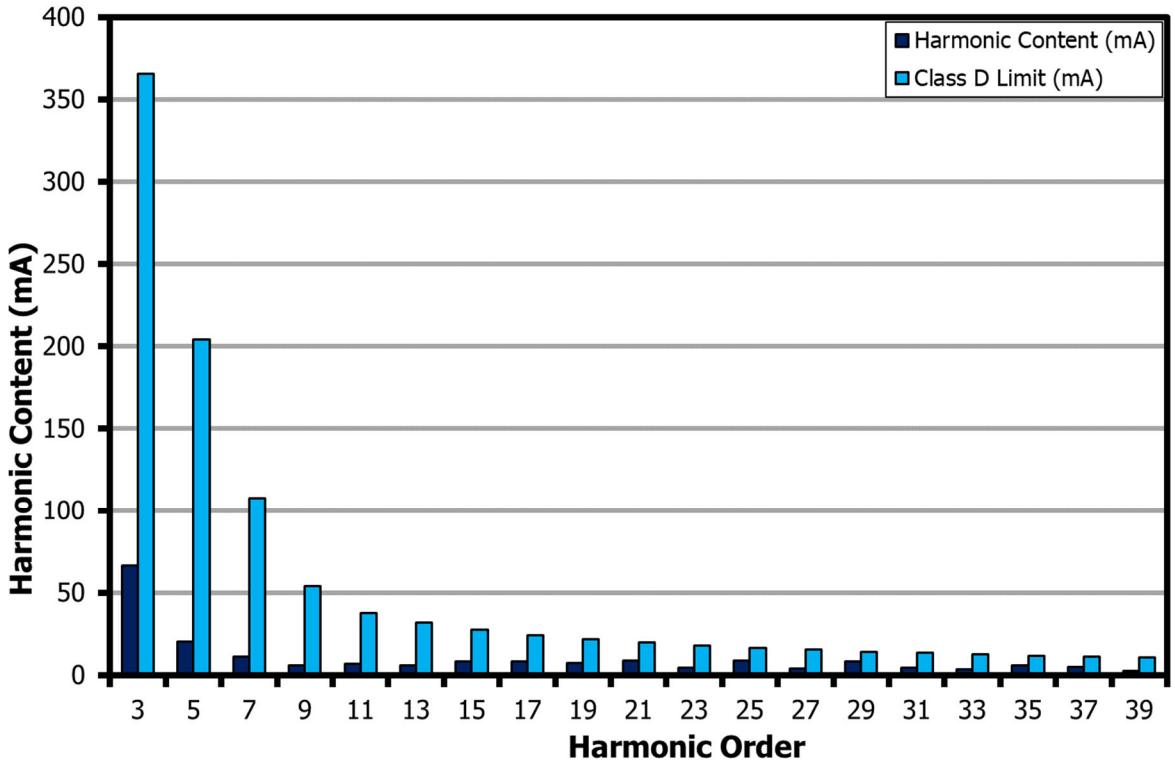


Figure 46 – Input Current Harmonics for 20 V Output, 5 A Load, 230 VAC, Room Temperature.

13.8.2.8 Output: 20 V / 5 A (265 VAC)

Input		Input Measurement					Output Measurement				
$VAC_{(RMS)}$	Freq (Hz)	$V_{IN(RMS)}$	I_{IN} (mA)	P_{IN} (W)	PF	% THD	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	%V Reg	Efficiency (%)
265	50	264.77	452.20	107.41	0.90	20.10	20.09	5000.00	100.47	0.47	93.54

Harmonic Order	Harmonic Content (mA)	Class D Limit (mA/W)	Class D Limit (mA)	Remarks
1	413.32			
3	57.16	3.40	365.19	Pass
5	35.04	1.90	204.08	Pass
7	19.36	1.00	107.41	Pass
9	32.22	0.50	53.71	Pass
11	16.65	0.35	37.59	Pass
13	10.21	0.30	31.81	Pass
15	5.03	0.26	27.57	Pass
17	2.74	0.23	24.33	Pass
19	2.24	0.20	21.76	Pass
21	5.54	0.18	19.69	Pass
23	4.31	0.17	17.98	Pass
25	2.87	0.15	16.54	Pass
27	4.35	0.14	15.32	Pass
29	2.48	0.12	14.26	Pass
31	4.48	0.12	13.34	Pass
33	4.07	0.12	12.53	Pass
35	4.40	0.11	11.82	Pass
37	4.27	0.10	11.18	Pass
39	4.41	0.10	10.60	Pass

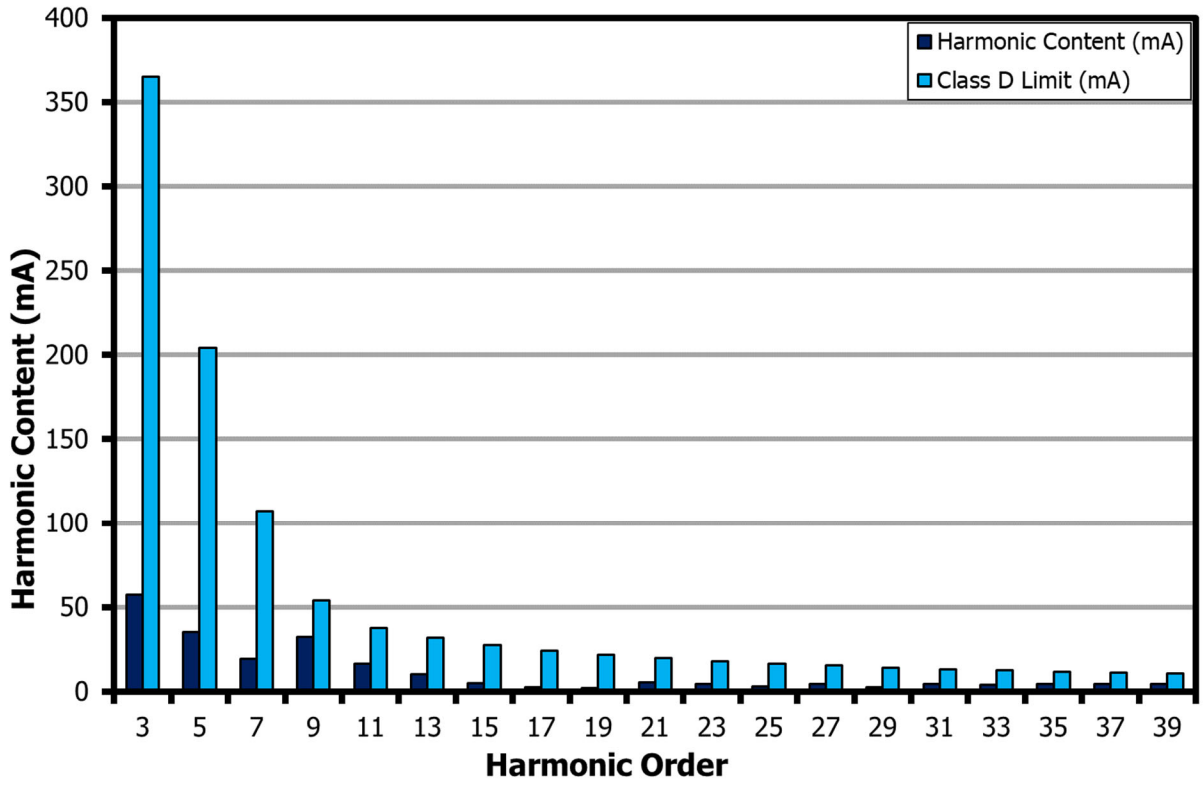


Figure 47 – Input Current Harmonics for 20 V Output, 5 A Load, 265 VAC, Room Temperature.

14 Thermal Performance

14.1 *Thermal Performance in Open Case, Room Temperature*

Note: For enclosed adapter application, this design requires use of metallic heat spreader and suitable thermally conductive insulator pads to ensure low temperature of the bridge rectifiers, HiperPFS-5, InnoSwitch4-Pro IC, and SR FETs. The performance data below is for open case operation and does not use heat spreader for cooling.

14.1.1 Test Set-up

Parameter	Value
Input Voltage	90 VAC, 265 VAC
Output Voltage	5 V, 9 V, 12 V, 15 V, 20 V
Output Load	100%
Soak Time per Line	60 minutes
Enclosure	Device is placed inside an acrylic box

14.1.2 Test Results

14.1.2.1 Output: 5 V / 5 A (90 VAC)

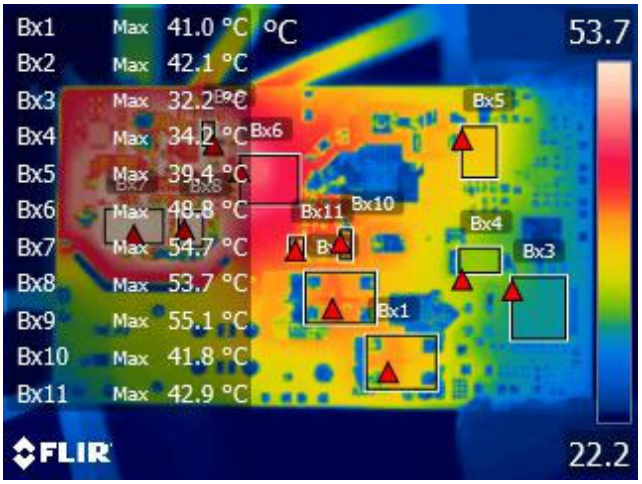


Figure 48 – Bottom Thermal Image, T_{AMB} = 22.6 ºC.
Bx1: Bridge Rectifier 1 = 41.0 ºC.
Bx2: Bridge Rectifier 2 = 42.1 ºC.
Bx3: HiperPFS-5 = 32.2 ºC.
Bx4: PFC Boost Diode = 34.2 ºC.
Bx5: ClampZero = 39.4 ºC.
Bx6: InnoSwitch4-Pro = 48.8 ºC.
Bx7: SR FET = 54.7 ºC.
Bx8: Schottky Diode = 53.7 ºC.
Bx9: IS Pin Resistor = 55.1 ºC.
Bx10: Primary Bias Diode = 41.8 ºC.
Bx11: BPP Linear Regulator BJT = 42.9 ºC.

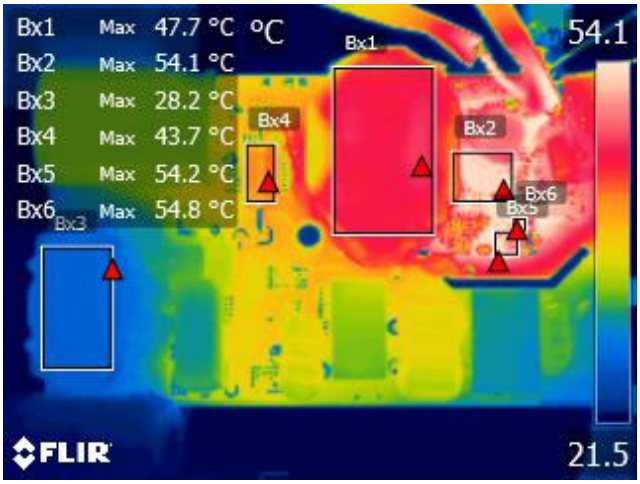


Figure 49 – Top Thermal Image, T_{AMB} = 22.6 ºC.
Bx1: Transformer Core = 47.7 ºC.
Bx2: Transformer Wire = 54.1 ºC.
Bx3: PFC Inductor Core = 28.2 ºC.
Bx4: Boost Pre-Charge Diode = 43.7 ºC.
Bx5: SR FET Snubber Resistor = 54.2 ºC.
Bx6: SR FET Snubber Diode = 54.8 ºC.

14.1.2.2 Output: 5 V / 5 A (265 VAC)

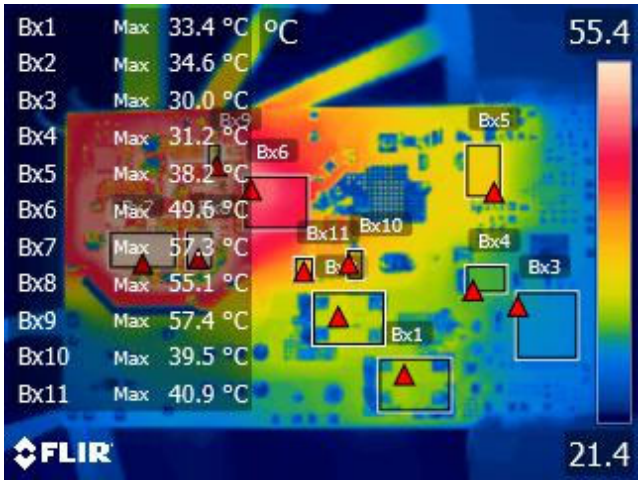


Figure 50 – Bottom Thermal Image, T_{AMB} = 22.4 ºC.
Bx1: Bridge Rectifier 1 = 33.4 ºC.
Bx2: Bridge Rectifier 2 = 34.6 ºC.
Bx3: HiperPFS-5 = 30.0 ºC.
Bx4: PFC Boost Diode = 31.2 ºC.
Bx5: ClampZero = 38.2 ºC.
Bx6: InnoSwitch4-Pro = 49.6 ºC.
Bx7: SR FET = 57.3 ºC.
Bx8: Schottky Diode = 55.1 ºC.
Bx9: IS Pin Resistor = 57.4 ºC.
Bx10: Primary Bias Diode = 39.5 ºC.
Bx11: BPP Linear Regulator BJT = 40.9 ºC.

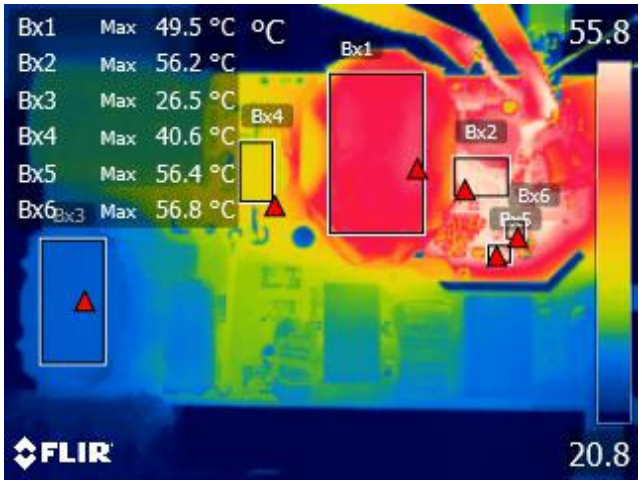


Figure 51 – Top Thermal Image, T_{AMB} = 22.4 ºC.
Bx1: Transformer Core = 49.5 ºC.
Bx2: Transformer Wire = 56.2 ºC.
Bx3: PFC Inductor Core = 26.5 ºC.
Bx4: Boost Pre-Charge Diode = 40.6 ºC.
Bx5: SR FET Snubber Resistor = 56.4 ºC.
Bx6: SR FET Snubber Diode = 56.8 ºC.

14.1.2.3 Output: 9 V / 5 A (90 VAC)

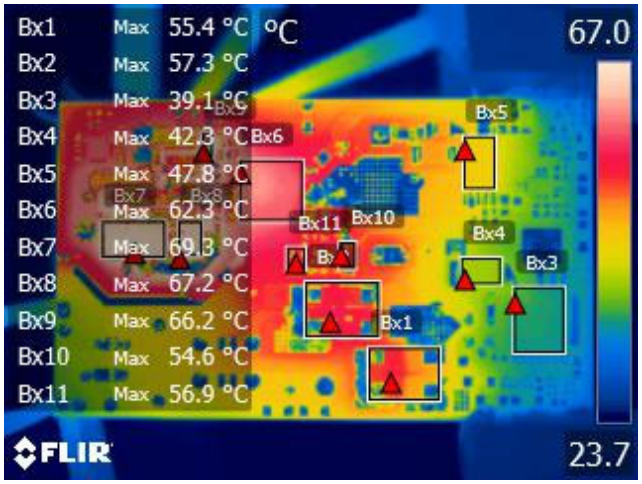


Figure 52 – Bottom Thermal Image, T_{AMB} = 24.6 ºC.
Bx1: Bridge Rectifier 1 = 55.4 ºC.
Bx2: Bridge Rectifier 2 = 57.3 ºC.
Bx3: HiperPFS-5 = 39.1 ºC.
Bx4: PFC Boost Diode = 42.3 ºC.
Bx5: ClampZero = 47.8 ºC.
Bx6: InnoSwitch4-Pro = 62.3 ºC.
Bx7: SR FET = 69.3 ºC.
Bx8: Schottky Diode = 67.2 ºC.
Bx9: IS Pin Resistor = 66.2 ºC.
Bx10: Primary Bias Diode = 54.6 ºC.
Bx11: BPP Linear Regulator BJT = 56.9 ºC.

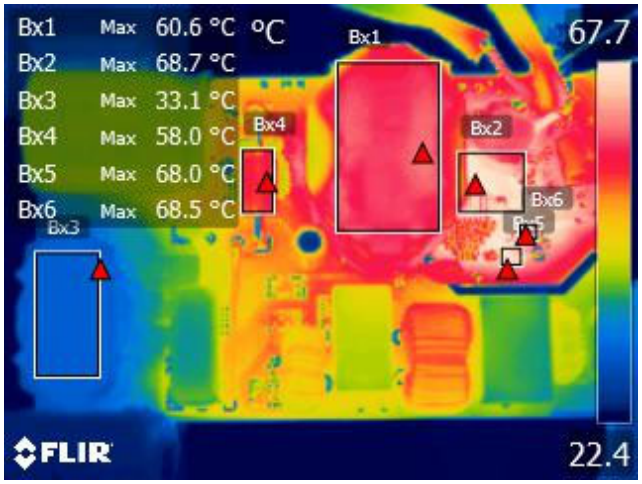


Figure 53 – Top Thermal Image, T_{AMB} = 24.6 ºC.
Bx1: Transformer Core = 60.6 ºC.
Bx2: Transformer Wire = 68.7 ºC.
Bx3: PFC Inductor Core = 33.1 ºC.
Bx4: Boost Pre-Charge Diode = 58.0 ºC.
Bx5: SR FET Snubber Resistor = 68.0 ºC.
Bx6: SR FET Snubber Diode = 68.5 ºC.

14.1.2.4 Output: 9 V / 5 A (265 VAC)

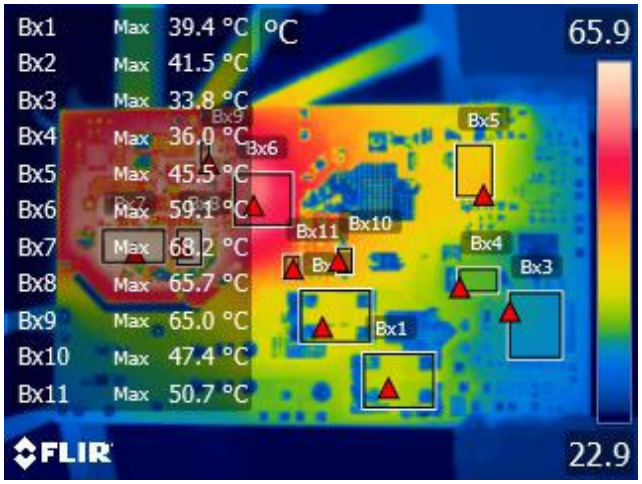


Figure 54 – Bottom Thermal Image, T_{AMB} = 23.6 ºC.
Bx1: Bridge Rectifier 1 = 39.4 ºC.
Bx2: Bridge Rectifier 2 = 41.5 ºC.
Bx3: HiperPFS-5 = 33.8 ºC.
Bx4: PFC Boost Diode = 36.0 ºC.
Bx5: ClampZero = 45.5 ºC.
Bx6: InnoSwitch4-Pro = 59.1 ºC.
Bx7: SR FET = 68.2 ºC.
Bx8: Schottky Diode = 65.7 ºC.
Bx9: IS Pin Resistor = 65.0 ºC.
Bx10: Primary Bias Diode = 47.4 ºC.
Bx11: BPP Linear Regulator BJT = 50.7 ºC.

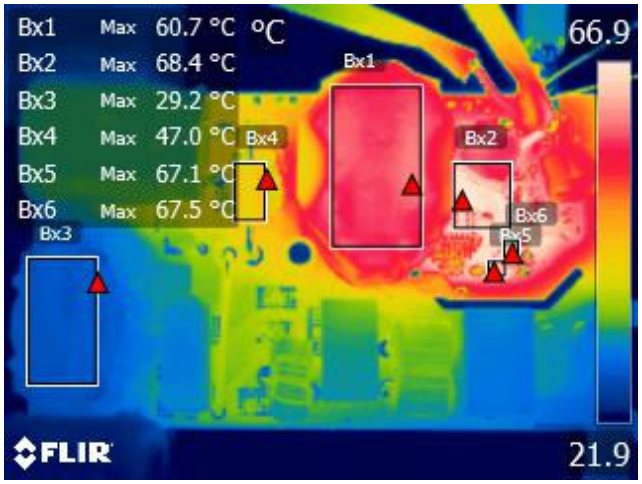


Figure 55 – Top Thermal Image, T_{AMB} = 23.6 ºC.
Bx1: Transformer Core = 60.7 ºC.
Bx2: Transformer Wire = 68.4 ºC.
Bx3: PFC Inductor Core = 29.2 ºC.
Bx4: Boost Pre-Charge Diode = 47.0 ºC.
Bx5: SR FET Snubber Resistor = 67.1 ºC.
Bx6: SR FET Snubber Diode = 67.5 ºC.

14.1.2.5 Output: 12 V / 5 A (90 VAC)

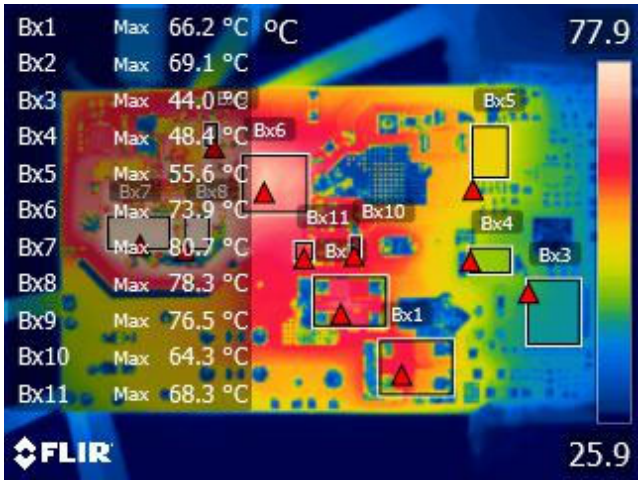


Figure 56 – Bottom Thermal Image, T_{AMB} = 25.4 ºC.
Bx1: Bridge Rectifier 1 = 66.2 ºC.
Bx2: Bridge Rectifier 2 = 69.1 ºC.
Bx3: HiperPFS-5 = 44.0 ºC.
Bx4: PFC Boost Diode = 48.4 ºC.
Bx5: ClampZero = 55.6 ºC.
Bx6: InnoSwitch4-Pro = 73.9 ºC.
Bx7: SR FET = 80.7 ºC.
Bx8: Schottky Diode = 78.3 ºC.
Bx9: IS Pin Resistor = 76.5 ºC.
Bx10: Primary Bias Diode = 64.3 ºC.
Bx11: BPP Linear Regulator BJT = 68.3 ºC.

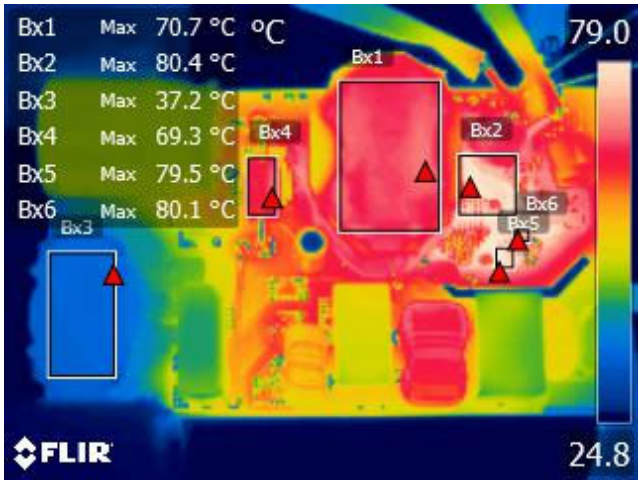


Figure 57 – Top Thermal Image, T_{AMB} = 25.4 ºC.
Bx1: Transformer Core = 70.7 ºC.
Bx2: Transformer Wire = 80.4 ºC.
Bx3: PFC Inductor Core = 37.2 ºC.
Bx4: Boost Pre-Charge Diode = 69.3 ºC.
Bx5: SR FET Snubber Resistor = 79.5 ºC.
Bx6: SR FET Snubber Diode = 80.1 ºC.

14.1.2.6 Output: 12 V / 5 A (265 VAC)

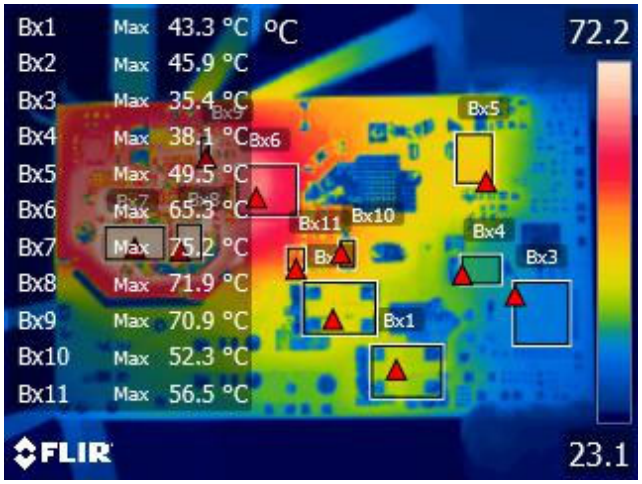


Figure 58 – Bottom Thermal Image, T_{AMB} = 24.8 ºC.
Bx1: Bridge Rectifier 1 = 43.3 ºC.
Bx2: Bridge Rectifier 2 = 45.9 ºC.
Bx3: HiperPFS-5 = 35.4 ºC.
Bx4: PFC Boost Diode = 38.1 ºC.
Bx5: ClampZero = 49.5 ºC.
Bx6: InnoSwitch4-Pro = 65.3 ºC.
Bx7: SR FET = 75.2 ºC.
Bx8: Schottky Diode = 71.9 ºC.
Bx9: IS Pin Resistor = 70.9 ºC.
Bx10: Primary Bias Diode = 52.3 ºC.
Bx11: BPP Linear Regulator BJT = 56.5 ºC.

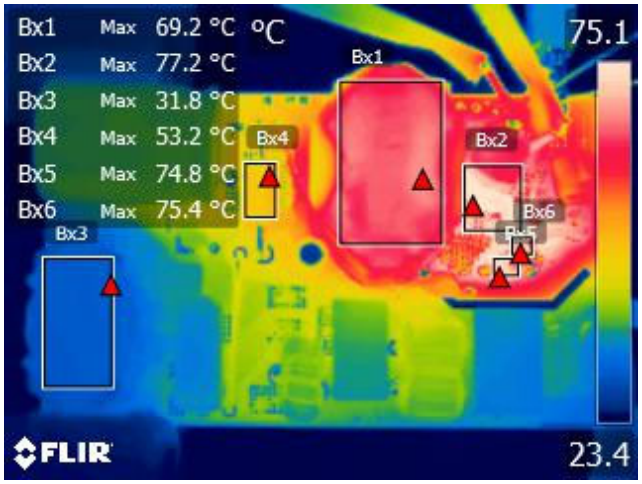


Figure 59 – Top Thermal Image, T_{AMB} = 24.8 ºC.
Bx1: Transformer Core = 69.2 ºC.
Bx2: Transformer Wire = 77.2 ºC.
Bx3: PFC Inductor Core = 31.8 ºC.
Bx4: Boost Pre-Charge Diode = 53.2 ºC.
Bx5: SR FET Snubber Resistor = 74.8 ºC.
Bx6: SR FET Snubber Diode = 75.4 ºC.

14.1.2.7 Output: 15 V / 5 A (90 VAC)

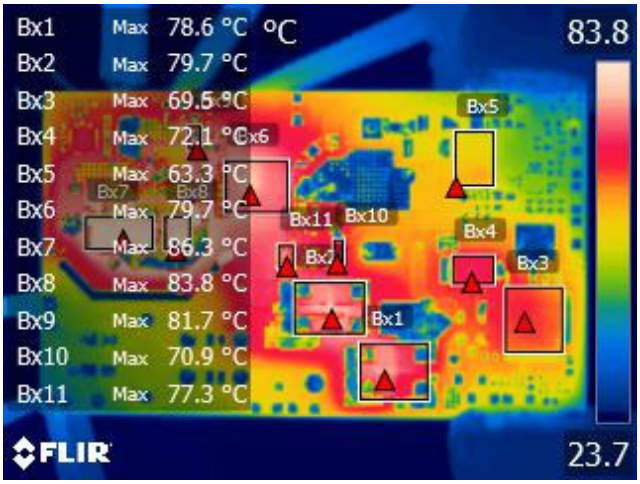


Figure 60 – Bottom Thermal Image, T_{AMB} = 24.5 ºC.
Bx1: Bridge Rectifier 1 = 78.6 ºC.
Bx2: Bridge Rectifier 2 = 79.7 ºC.
Bx3: HiperPFS-5 = 69.5 ºC.
Bx4: PFC Boost Diode = 72.1 ºC.
Bx5: ClampZero = 63.3 ºC.
Bx6: InnoSwitch4-Pro = 79.7 ºC.
Bx7: SR FET = 86.3 ºC.
Bx8: Schottky Diode = 83.8 ºC.
Bx9: IS Pin Resistor = 81.7 ºC.
Bx10: Primary Bias Diode = 70.9 ºC.
Bx11: BPP Linear Regulator BJT = 77.3 ºC.

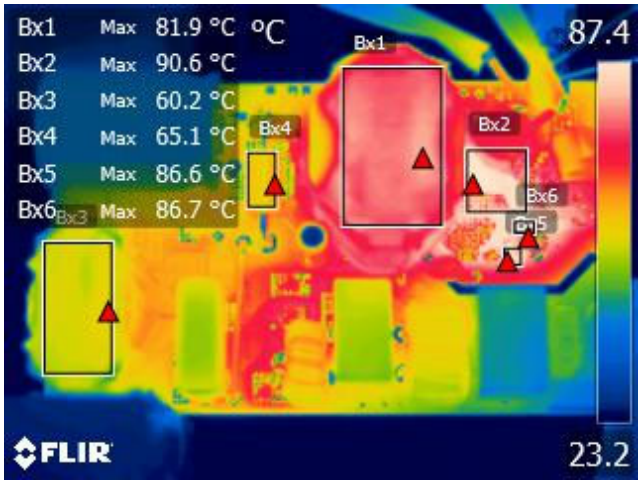


Figure 61 – Top Thermal Image, T_{AMB} = 24.5 ºC.
Bx1: Transformer Core = 81.9 ºC.
Bx2: Transformer Wire = 90.6 ºC.
Bx3: PFC Inductor Core = 60.2 ºC.
Bx4: Boost Pre-Charge Diode = 65.1 ºC.
Bx5: SR FET Snubber Resistor = 86.6 ºC.
Bx6: SR FET Snubber Diode = 86.7 ºC.

14.1.2.8 Output: 15 V / 5 A (265 VAC)

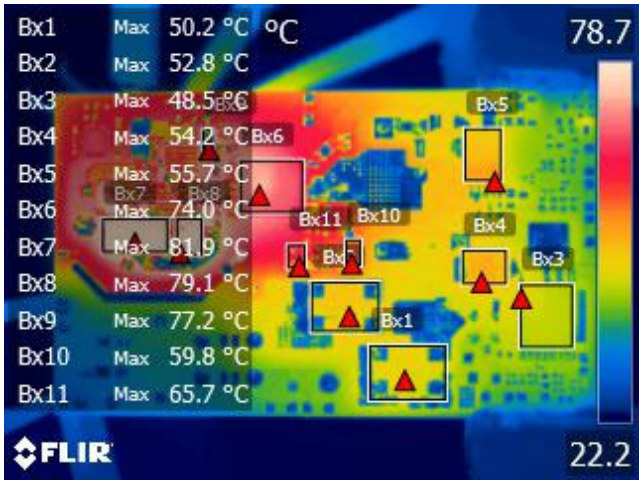


Figure 62 – Bottom Thermal Image, T_{AMB} = 24.2 ºC.
Bx1: Bridge Rectifier 1 = 50.2 ºC.
Bx2: Bridge Rectifier 2 = 52.8 ºC.
Bx3: HiperPFS-5 = 48.5 ºC.
Bx4: PFC Boost Diode = 54.2 ºC.
Bx5: ClampZero = 55.7 ºC.
Bx6: InnoSwitch4-Pro = 74.0 ºC.
Bx7: SR FET = 81.9 ºC.
Bx8: Schottky Diode = 79.1 ºC.
Bx9: IS Pin Resistor = 77.2 ºC.
Bx10: Primary Bias Diode = 59.8 ºC.
Bx11: BPP Linear Regulator BJT = 65.7 ºC.

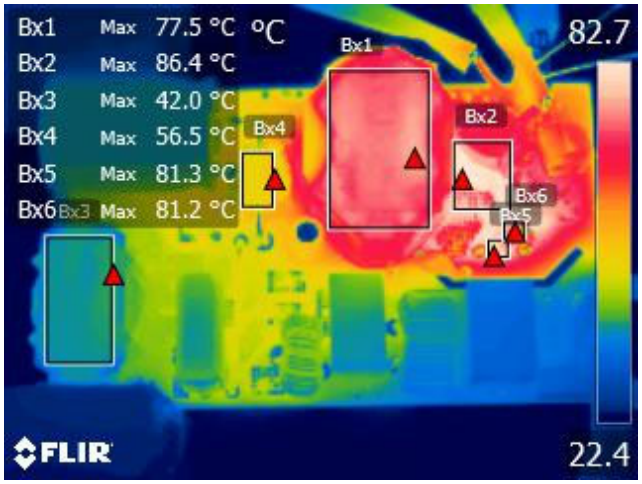


Figure 63 – Top Thermal Image, T_{AMB} = 24.2 ºC.
Bx1: Transformer Core = 77.5 ºC.
Bx2: Transformer Wire = 86.4 ºC.
Bx3: PFC Inductor Core = 42.0 ºC.
Bx4: Boost Pre-Charge Diode = 56.5 ºC.
Bx5: SR FET Snubber Resistor = 81.3 ºC.
Bx6: SR FET Snubber Diode = 81.2 ºC.

14.1.2.9 Output: 20 V / 5 A (90 VAC)

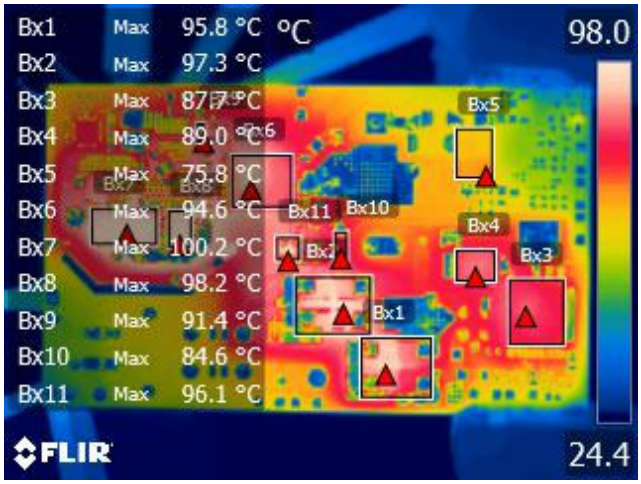


Figure 64 – Bottom Thermal Image, T_{AMB} = 26.4 ºC.
Bx1: Bridge Rectifier 1 = 95.8 ºC.
Bx2: Bridge Rectifier 2 = 97.3 ºC.
Bx3: HiperPFS-5 = 87.7 ºC.
Bx4: PFC Boost Diode = 89.0 ºC.
Bx5: ClampZero = 75.8 ºC.
Bx6: InnoSwitch4-Pro = 94.6 ºC.
Bx7: SR FET = 100.2 ºC.
Bx8: Schottky Diode = 98.2 ºC.
Bx9: IS Pin Resistor = 91.4 ºC.
Bx10: Primary Bias Diode = 84.6 ºC.
Bx11: BPP Linear Regulator BJT = 96.1 ºC.

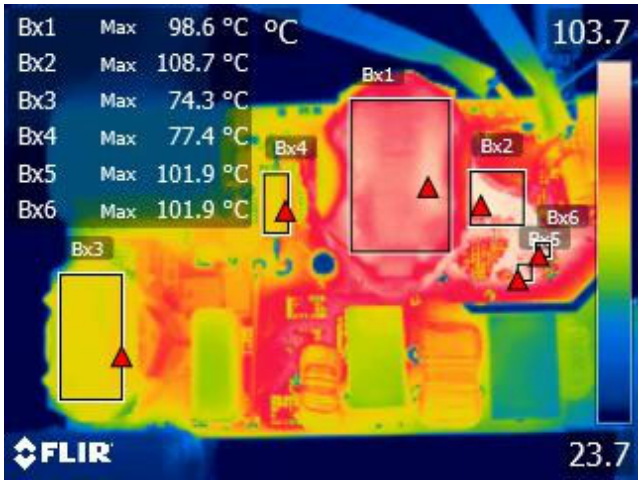


Figure 65 – Top Thermal Image, T_{AMB} = 26.4 ºC.
Bx1: Transformer Core = 98.6 ºC.
Bx2: Transformer Wire = 108.7 ºC.
Bx3: PFC Inductor Core = 74.3 ºC.
Bx4: Boost Pre-Charge Diode = 77.4 ºC.
Bx5: SR FET Snubber Resistor = 101.9 ºC.
Bx6: SR FET Snubber Diode = 101.9 ºC.

14.1.2.10 Output: 20 V / 5 A (265 VAC)

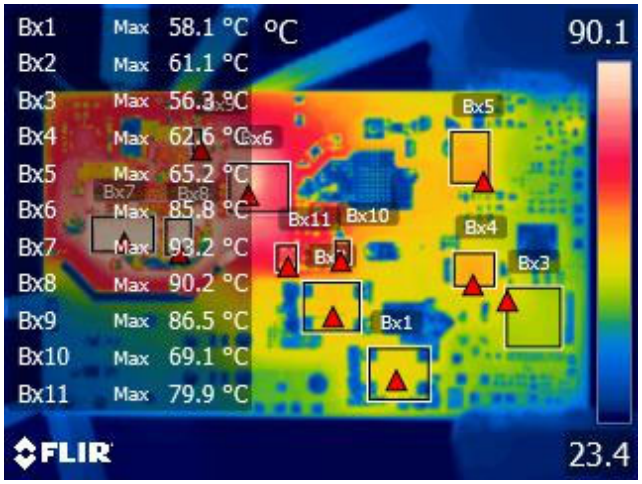


Figure 66 – Bottom Thermal Image, T_{AMB} = 25.0 ºC.
Bx1: Bridge Rectifier 1 = 58.1 ºC.
Bx2: Bridge Rectifier 2 = 61.1 ºC.
Bx3: HiperPFS-5 = 56.3 ºC.
Bx4: PFC Boost Diode = 62.6 ºC.
Bx5: ClampZero = 65.2 ºC.
Bx6: InnoSwitch4-Pro = 85.8 ºC.
Bx7: SR FET = 93.2 ºC.
Bx8: Schottky Diode = 90.2 ºC.
Bx9: IS Pin Resistor = 86.5 ºC.
Bx10: Primary Bias Diode = 69.1 ºC.
Bx11: BPP Linear Regulator BJT = 79.9 ºC.

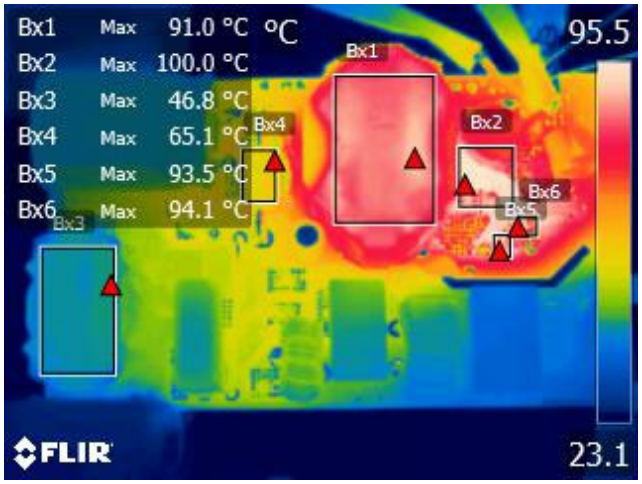


Figure 67 – Top Thermal Image, T_{AMB} = 25.0 ºC.
Bx1: Transformer Core = 91.0 ºC.
Bx2: Transformer Wire = 100.0 ºC.
Bx3: PFC Inductor Core = 46.8 ºC.
Bx4: Boost Pre-Charge Diode = 65.1 ºC.
Bx5: SR FET Snubber Resistor = 93.5 ºC.
Bx6: SR FET Snubber Diode = 94.1 ºC.

15 Waveforms

Note: 1. Output voltage captured at the end of 100 mΩ cable unless otherwise specified.
2. Waveforms taken at room temperature ambient (approximately 25 °C).

15.1 *Input Voltage and Current Waveforms*

Note: Input voltage and current waveforms are captured for conditions when PFC is enabled

15.1.1 Output: 15 V / 5 A

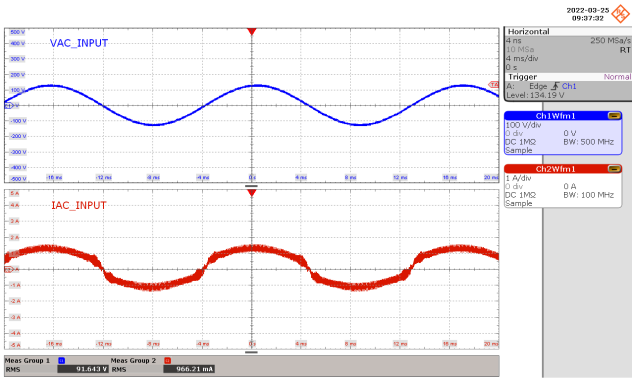


Figure 68 – Input Voltage and Current.
90 VAC, 15.0 V, 5 A Load.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 1 A / div.
Time: 4 ms / div.

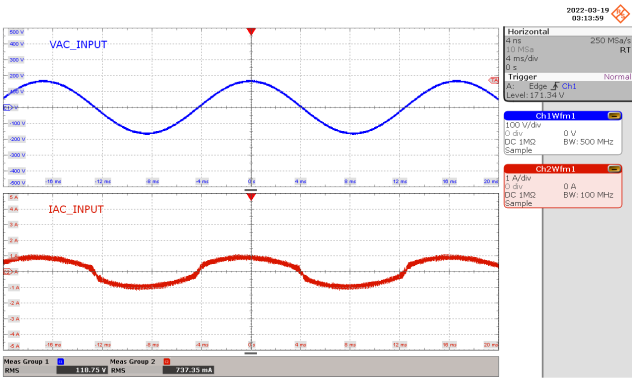


Figure 69 – Input Voltage and Current.
115 VAC, 15.0 V, 5 A Load.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 1 A / div.
Time: 4 ms / div.

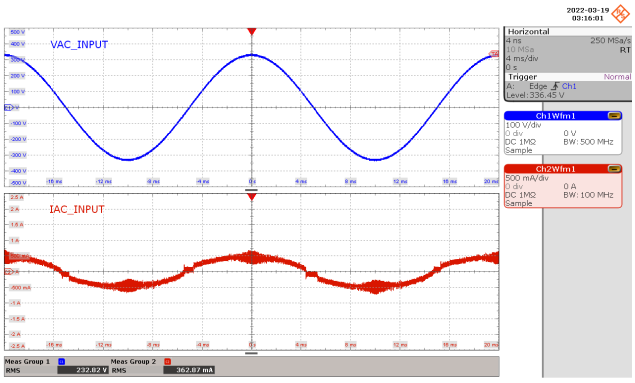


Figure 70 – Input Voltage and Current.
230 VAC, 15.0 V, 5 A Load.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 500 mA / div.
Time: 4 ms / div.

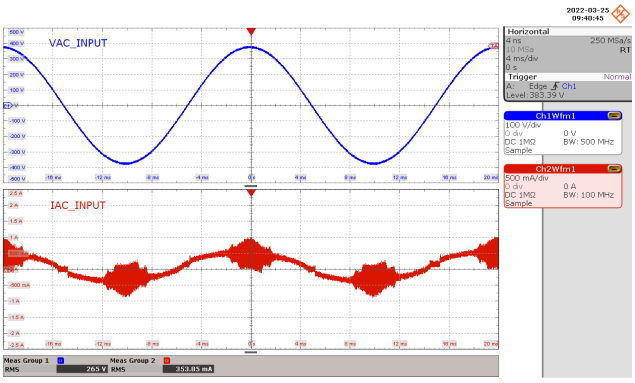


Figure 71 – Input Voltage and Current.
265 VAC, 15.0 V, 5 A Load.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 500 mA / div.
Time: 4 ms / div.

15.1.2 Output: 20 V / 5 A

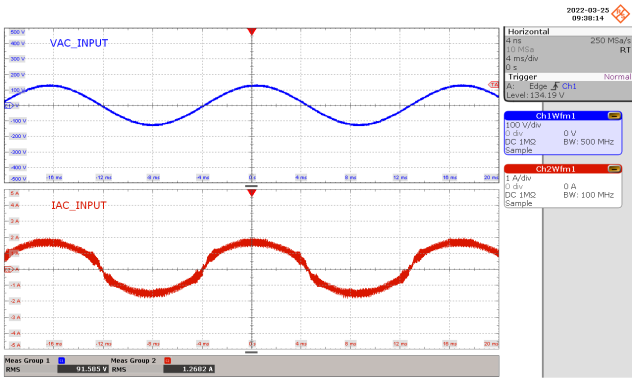


Figure 72 – Input Drain Voltage and Current.
90 VAC, 20.0 V, 5 A Load.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 1 A / div.
Time: 4 ms / div.

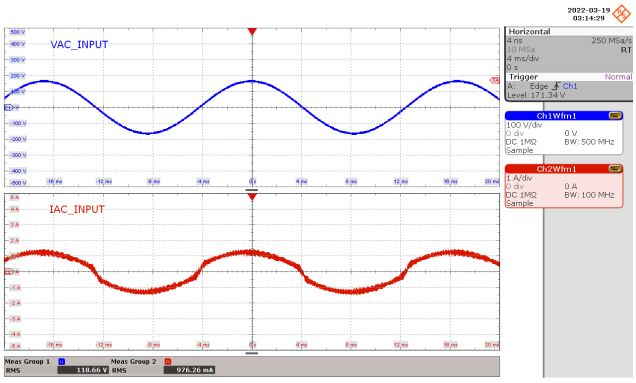


Figure 73 – Input Voltage and Current.
115 VAC, 20.0 V, 5 A Load.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 1 A / div.
Time: 4 ms / div.

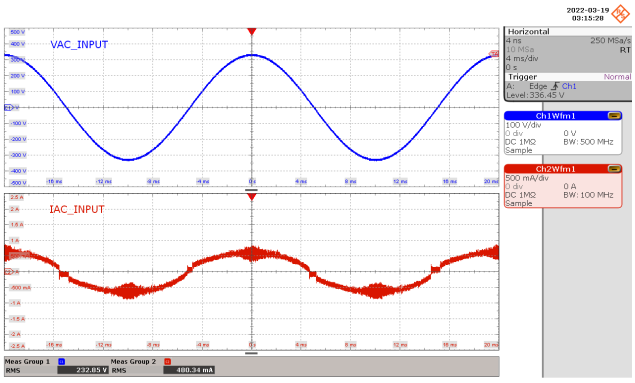


Figure 74 – Input Drain Voltage and Current.
230 VAC, 20.0 V, 5 A Load.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 500 mA / div.
Time: 4 ms / div.

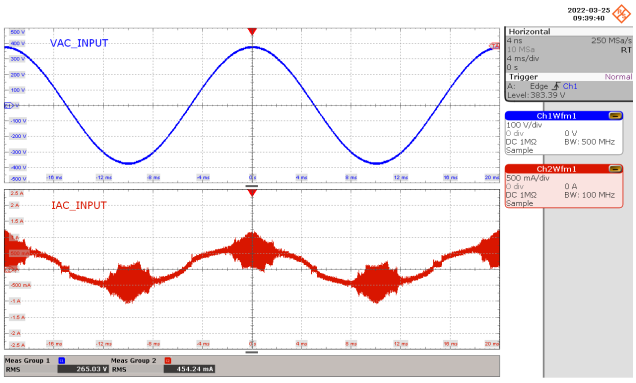


Figure 75 – Input Voltage and Current.
265 VAC, 20.0 V, 5 A Load.
CH1: V_{IN_AC}, 100 V / div.
CH2: I_{IN_AC}, 500 mA / div.
Time: 4 ms / div.

15.2 *PFC Inductor Current and HiperPFS-5 Drain Voltage Waveforms*

Note: HiperPFS-5 drain voltage and PFC inductor current waveforms are captured for conditions when PFC is enabled

15.2.1 Output: 15 V / 5 A

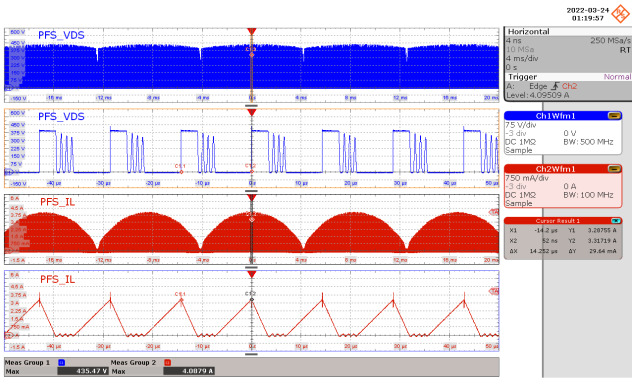


Figure 76 – PFC Inductor Current and HiperPFS-5 Drain Voltage.
90 VAC, 15.0 V, 5 A Load.
V_{DS_PFS} = 435 V Maximum.
I_{L_PFC} = 4.08 A Maximum.
CH1: V_{DS_PFS}, 75 V / div.
CH2: I_{L_PFC}, 750 mA / div.
Time: 4 ms / div. (10 µs / div. Zoom).

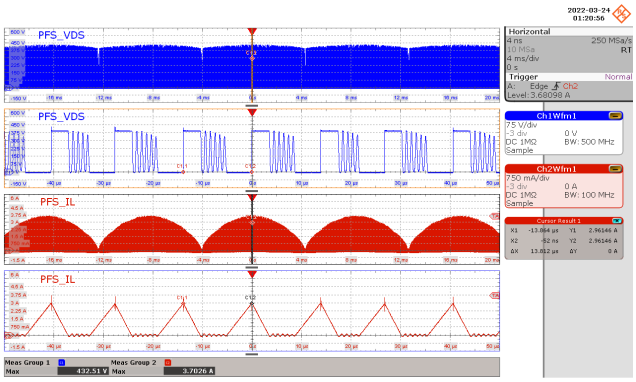


Figure 77 – PFC Inductor Current and HiperPFS-5 Drain Voltage.
115 VAC, 15.0 V, 5 A Load.
V_{DS_PFS} = 432 V Maximum.
I_{L_PFC} = 3.70 A Maximum.
CH1: V_{DS_PFS}, 75 V / div.
CH2: I_{L_PFC}, 750 mA / div.
Time: 4 ms / div. (10 µs / div. Zoom).

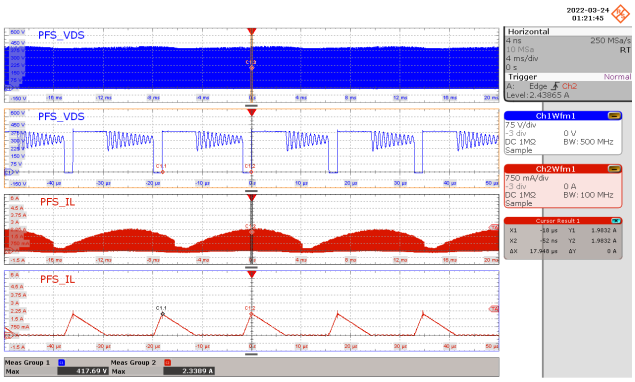


Figure 78 – PFC Inductor Current and HiperPFS-5 Drain Voltage.
230 VAC, 15.0 V, 5 A Load.
V_{DS_PFS} = 417 V Maximum.
I_{L_PFC} = 2.33 A Maximum.
CH1: V_{DS_PFS}, 75 V / div.
CH2: I_{L_PFC}, 750 mA / div.
Time: 4 ms / div. (10 µs / div. Zoom).

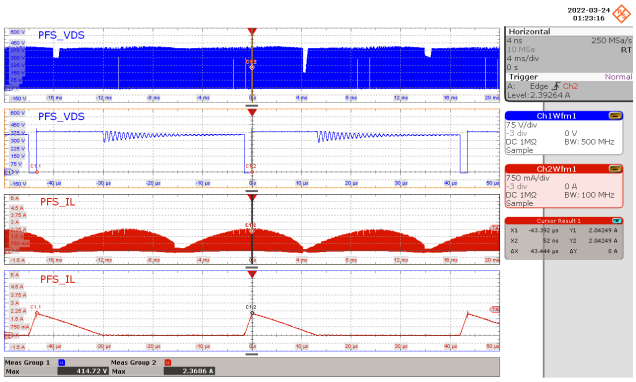


Figure 79 – PFC Inductor Current and HiperPFS-5 Drain Voltage.
265 VAC, 15.0 V, 5 A Load.
V_{DS_PFS} = 414 V Maximum.
I_{L_PFC} = 2.36 A Maximum.
CH1: V_{DS_PFS}, 75 V / div.
CH2: I_{L_PFC}, 750 mA / div.
Time: 4 ms / div. (10 µs / div. Zoom).

15.2.2 Output: 20 V / 5 A

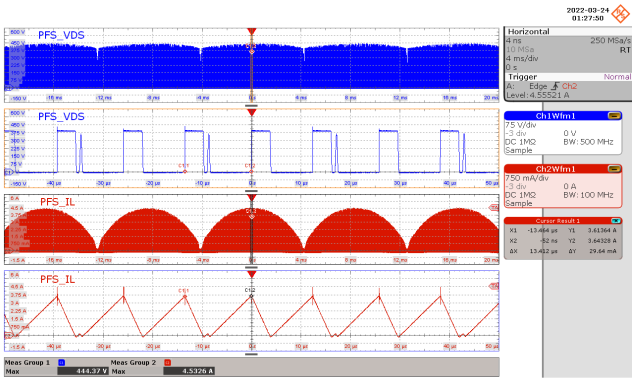


Figure 80 – PFC Inductor Current and HiperPFS-5 Drain Voltage.
90 VAC, 20.0 V, 5 A Load.
V_{DS_PFS} = 444 V Maximum.
I_{L_PFC} = 4.53 A Maximum.
CH1: V_{DS_PFS}, 75 V / div.
CH2: I_{L_PFC}, 750 mA / div.
Time: 4 ms / div. (10 μs / div. Zoom).

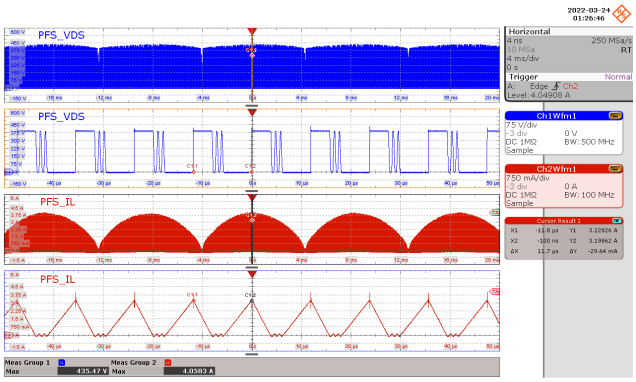


Figure 81 – PFC Inductor Current and HiperPFS-5 Drain Voltage.
115 VAC, 20.0 V, 5 A Load.
V_{DS_PFS} = 435 V Maximum.
I_{L_PFC} = 4.05 A Maximum.
CH1: V_{DS_PFS}, 75 V / div.
CH2: I_{L_PFC}, 750 mA / div.
Time: 4 ms / div. (10 μs / div. Zoom).

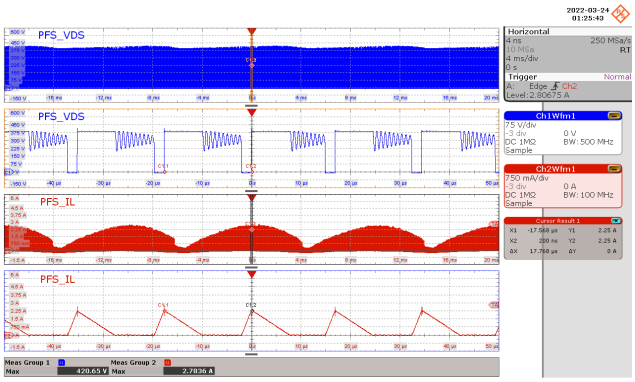


Figure 82 – PFC Inductor Current and HiperPFS-5 Drain Voltage.
230 VAC, 20.0 V, 5 A Load.
V_{DS_PFS} = 420 V Maximum.
I_{L_PFC} = 2.78 A Maximum.
CH1: V_{DS_PFS}, 75 V / div.
CH2: I_{L_PFC}, 750 mA / div.
Time: 4 ms / div. (10 μs / div. Zoom).

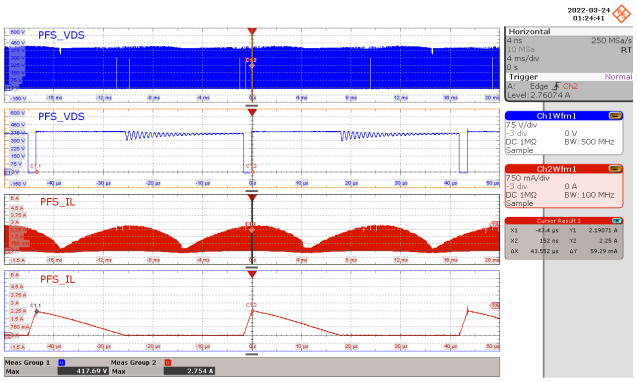


Figure 83 – PFC Inductor Current and HiperPFS-5 Drain Voltage.
265 VAC, 20.0 V, 5 A Load.
V_{DS_PFS} = 417 V Maximum.
I_{L_PFC} = 2.75 A Maximum.
CH1: V_{DS_PFS}, 75 V / div.
CH2: I_{L_PFC}, 750 mA / div.
Time: 4 ms / div. (10 μs / div. Zoom).

15.3 *Start-up Waveforms*

15.3.1 Output Voltage and Current

Output voltage on board, load current, and input voltage were captured.

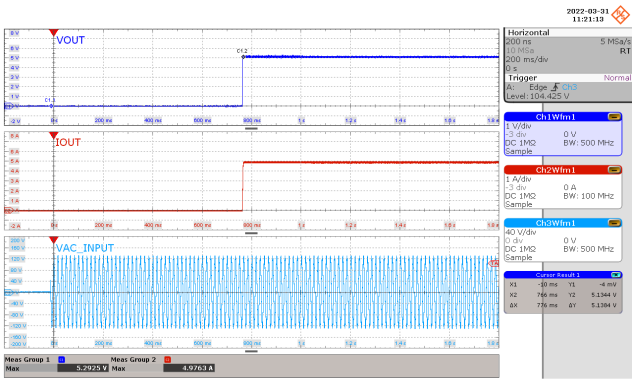


Figure 84 – Output Voltage and Current.
90 VAC, 5.0 V, 5 A (CR Mode,
930 mΩ at the End of 100 mΩ Cable).
$V_{OUT,MAX}$ = 5.2925 V Steady-State.
CH1: V_{OUT}, 1 V / div.
CH2: I_{LOAD}, 1 A / div.
CH3: V_{AC_INPUT}, 40 V / div.
Time: 200 ms / div.

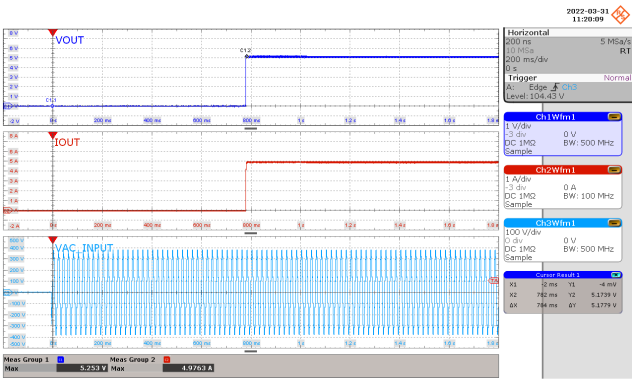


Figure 85 – Output Voltage and Current.
265 VAC, 5.0 V, 5 A (CR Mode,
930 mΩ at the End of 100 mΩ Cable).
$V_{OUT,MAX}$ = 5.253 V Steady-State.
CH1: V_{OUT}, 1 V / div.
CH2: I_{LOAD}, 1 A / div.
CH3: V_{AC_INPUT}, 100 V / div.
Time: 200 ms / div.

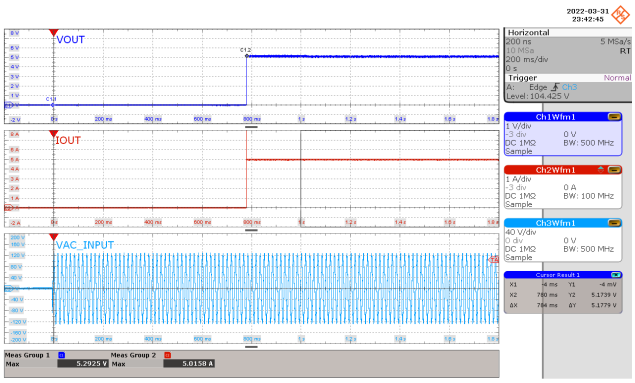


Figure 86 – Output Voltage and Current.
90 VAC, 5.0 V, 5 A (CC Mode).
$V_{OUT,MAX}$ = 5.2925 V Steady-State.
CH1: V_{OUT}, 1 V / div.
CH2: I_{LOAD}, 1 A / div.
CH3: V_{AC_INPUT}, 40 V / div.
Time: 200 ms / div.

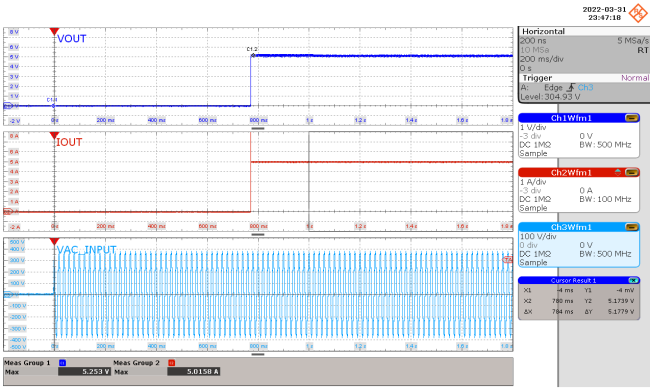


Figure 87 – Output Voltage and Current.
265 VAC, 5.0 V, 5 A (CC Mode).
$V_{OUT,MAX}$ = 5.253 V Steady-State.
CH1: V_{OUT}, 1 V / div.
CH2: I_{LOAD}, 1 A / div.
CH3: V_{AC_INPUT}, 100 V / div.
Time: 200 ms / div.

15.3.2 Primary Drain Voltage and Current

Primary Drain Voltage, Drain Current, and output voltage before the bus switch were captured.

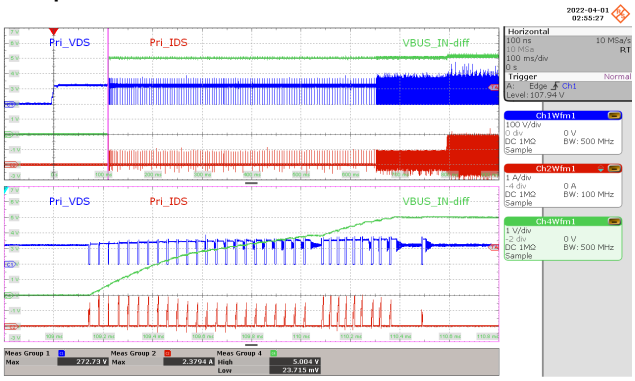


Figure 88 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 5 A (CR Mode,
930 mΩ at the End of 100 mΩ Cable).
V_{DS_PRI} = 272 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 1 A / div.
CH4: V_{BUS_IN}, 1 V / div.
Time: 100 ms / div. (200 μs / div. Zoom).

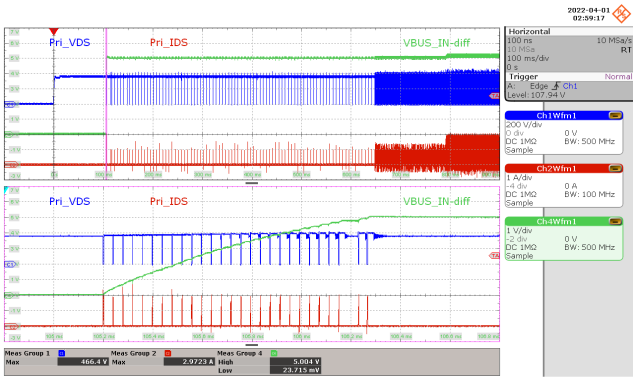


Figure 89 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 5 A (CR Mode,
930 mΩ at the End of 100 mΩ Cable).
V_{DS_PRI} = 466 V Maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 1 A / div.
CH4: V_{BUS_IN}, 1 V / div.
Time: 100 ms / div. (200 μs / div. Zoom).

15.3.3 SR FET Drain Voltage

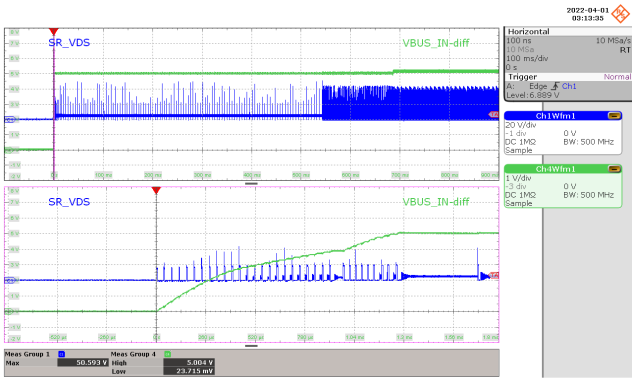


Figure 90 – SR FET Drain Voltage and Current.
90 VAC, 5.0 V, 5 A (CR Mode,
930 mΩ at the End of 100 mΩ Cable).
V_{DS_SRFET} = 50.5 V Maximum.
CH1: V_{DS_SRFET}, 20 V / div.
CH4: V_{BUS_IN}, 1 V / div.
Time: 100 ms / div. (260 μs / div. Zoom).

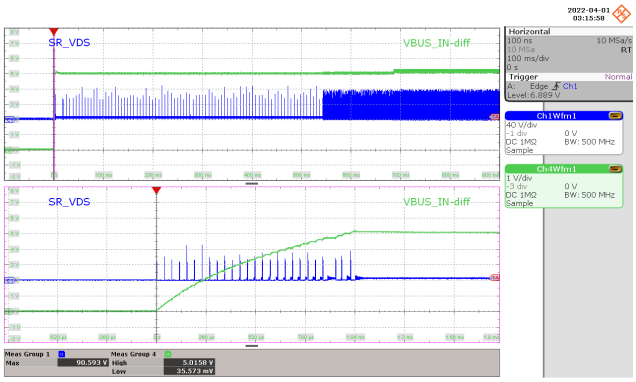


Figure 91 – SR FET Drain Voltage and Current.
265 VAC, 5.0 V, 5 A (CR Mode,
930 mΩ at the End of 100 mΩ Cable).
V_{DS_SRFET} = 90.5 V Maximum.
CH1: V_{DS_SRFET}, 40 V / div.
CH4: V_{BUS_IN}, 1 V / div.
Time: 100 ms / div. (260 μs / div. Zoom).

15.4 *Primary Drain Voltage and Current (Steady-State)*

15.4.1 Output: 5 V / 5 A

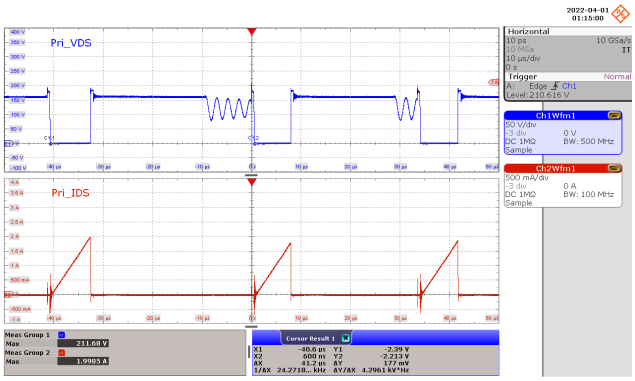


Figure 92 – Primary Drain Voltage and Current.
90 VAC, 5.0 V, 5 A Load.
V_{DS_PRI} = 211 V Maximum.
CH1: V_{DS_PRI}, 50 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

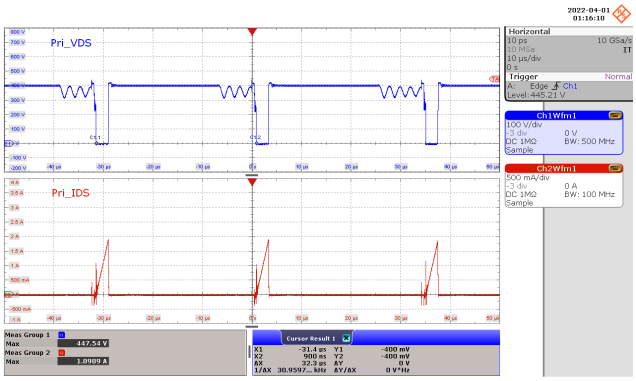


Figure 93 – Primary Drain Voltage and Current.
265 VAC, 5.0 V, 5 A Load.
V_{DS_PRI} = 447 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

15.4.2 Output: 9 V / 5 A

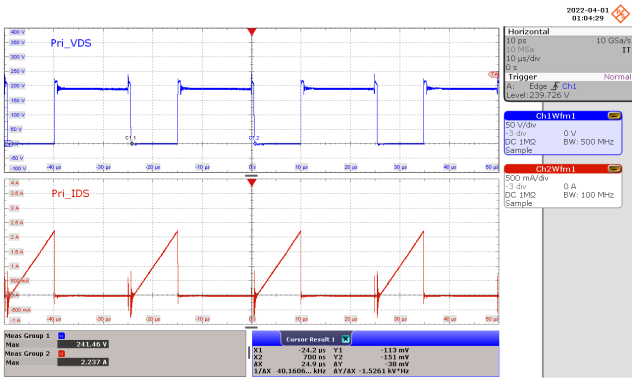


Figure 94 – Primary Drain Voltage and Current.
90 VAC, 9.0 V, 5 A Load.
V_{DS_PRI} = 241 V Maximum.
CH1: V_{DS_PRI}, 50 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

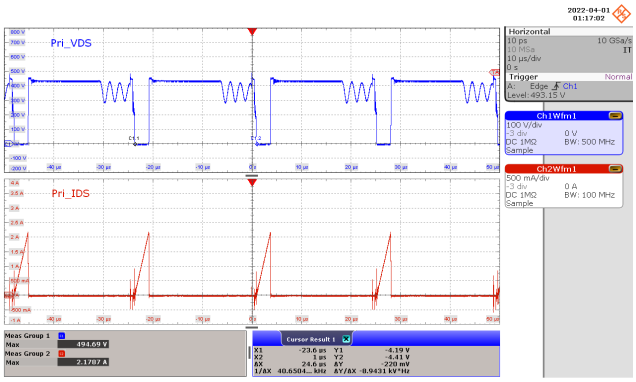


Figure 95 – Primary Drain Voltage and Current.
265 VAC, 9.0 V, 5 A Load.
V_{DS_PRI} = 494 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

15.4.3 Output: 12 V / 5 A

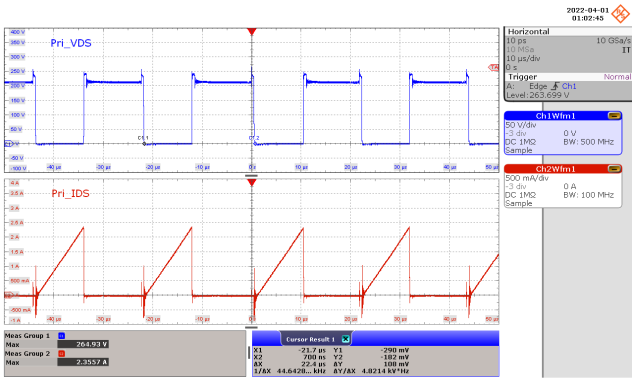


Figure 96 – Primary Drain Voltage and Current.
90 VAC, 12.0 V, 5 A Load.
V_{DS_PRI} = 264 V Maximum.
CH1: V_{DS_PRI}, 50 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

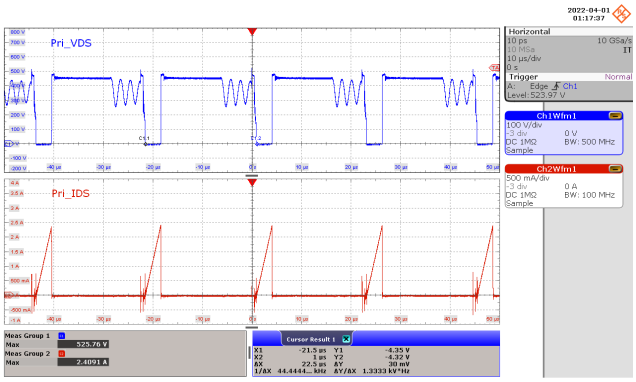


Figure 97 – Primary Drain Voltage and Current.
265 VAC, 12.0 V, 5 A Load.
V_{DS_PRI} = 525 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

15.4.4 Output: 15 V / 5 A

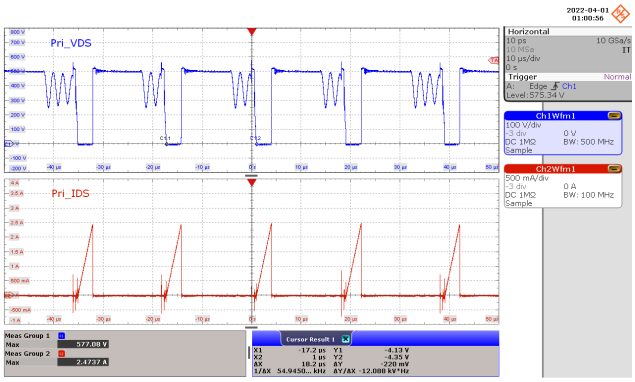


Figure 98 – Primary Drain Voltage and Current.
90 VAC, 15.0 V, 5 A Load.
V_{DS_PRI} = 577 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

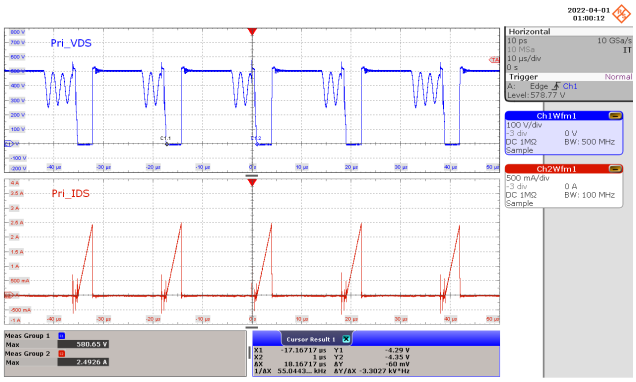


Figure 99 – Primary Drain Voltage and Current.
265 VAC, 15.0 V, 5 A Load.
V_{DS_PRI} = 580 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

15.4.5 Output: 20 V / 5 A

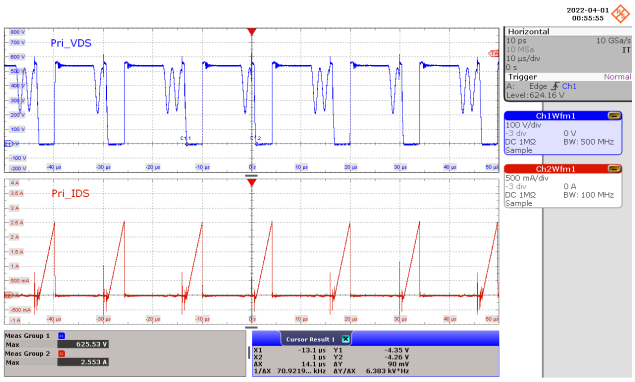


Figure 100 – Primary Drain Voltage and Current.
90 VAC, 20.0 V, 5 A Load.
V_{DS_PRI} = 625 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

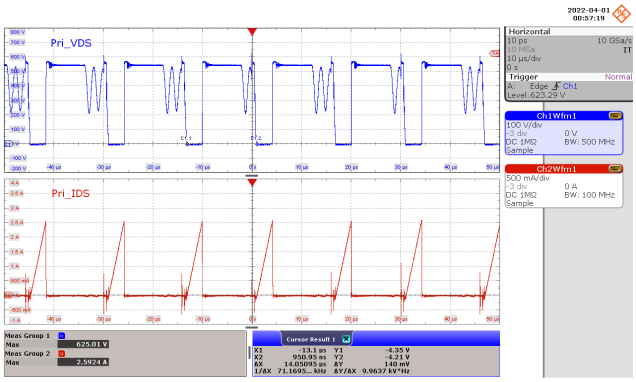


Figure 101 – Primary Drain Voltage and Current.
265 VAC, 20.0 V, 5 A Load.
V_{DS_PRI} = 625 V Maximum.
CH1: V_{DS_PRI}, 100 V / div.
CH2: I_{DS_PRI}, 500 mA / div.
Time: 10 µs / div.

15.5 *ClampZero Drain Voltage and Current (Steady-State)*

15.5.1 Output: 5 V / 5 A

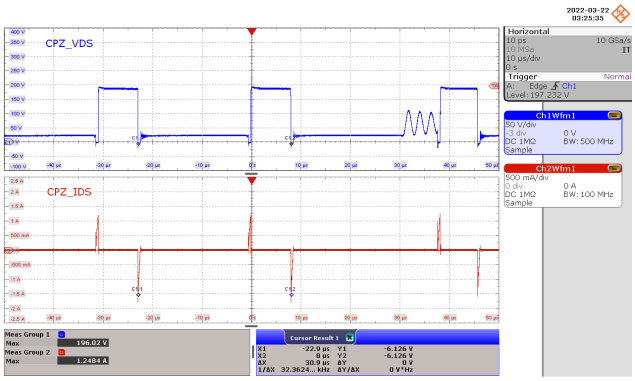


Figure 102 – ClampZero Drain Voltage and Current.
90 VAC, 5.0 V, 5 A Load.
V_{DS_CPZ} = 196 V Maximum.
CH1: V_{DS_CPZ}, 50 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

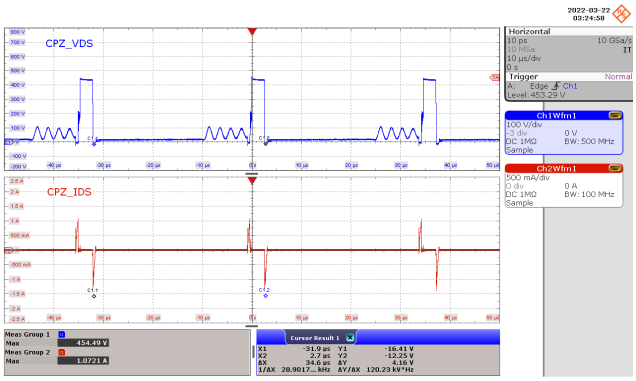


Figure 103 – ClampZero Drain Voltage and Current.
265 VAC, 5.0 V, 5 A Load.
V_{DS_CPZ} = 454 V Maximum.
CH1: V_{DS_CPZ}, 100 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

15.5.2 Output: 9 V / 5 A

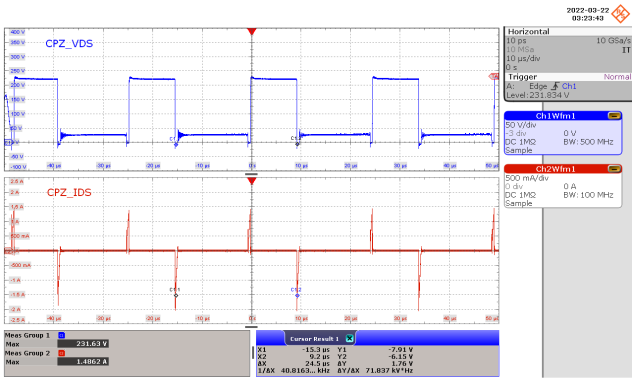


Figure 104 – ClampZero Drain Voltage and Current.
90 VAC, 9.0 V, 5 A Load.
V_{DS_CPZ} = 231 V Maximum.
CH1: V_{DS_CPZ}, 50 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

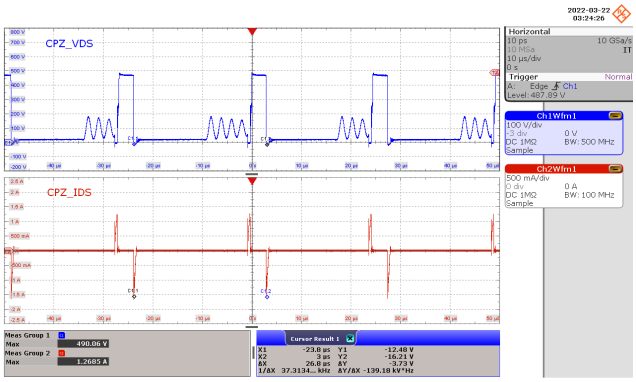


Figure 105 – ClampZero Drain Voltage and Current.
265 VAC, 9.0 V, 5 A Load.
V_{DS_CPZ} = 490 V Maximum.
CH1: V_{DS_CPZ}, 100 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

15.5.3 Output: 12 V / 5 A

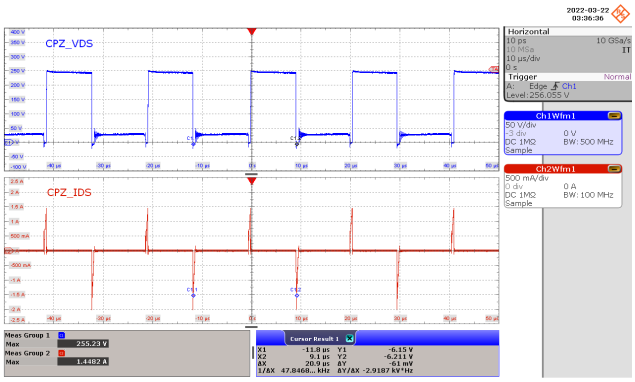


Figure 106 – ClampZero Drain Voltage and Current.
90 VAC, 12.0 V, 5 A Load.
V_{DS_CPZ} = 255 V Maximum.
CH1: V_{DS_CPZ}, 50 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

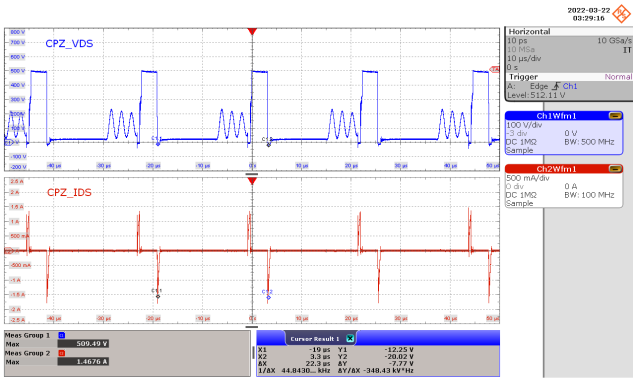


Figure 107 – ClampZero Drain Voltage and Current.
265 VAC, 12.0 V, 5 A Load.
V_{DS_CPZ} = 509 V Maximum.
CH1: V_{DS_CPZ}, 100 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

15.5.4 Output: 15 V / 5 A

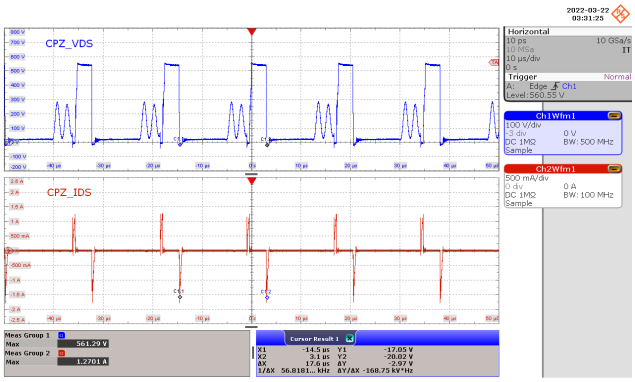


Figure 108 – ClampZero Drain Voltage and Current.
90 VAC, 15.0 V, 5 A Load.
V_{DS_CPZ} = 561 V Maximum.
CH1: V_{DS_CPZ}, 100 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

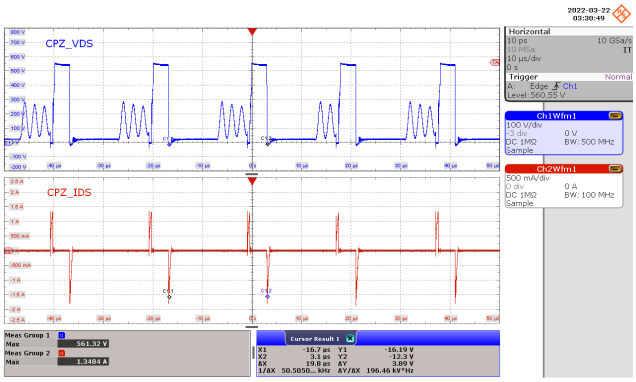


Figure 109 – ClampZero Drain Voltage and Current.
265 VAC, 15 V, 5 A Load.
V_{DS_CPZ} = 561 V Maximum.
CH1: V_{DS_CPZ}, 100 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

15.5.5 Output: 20 V / 5 A

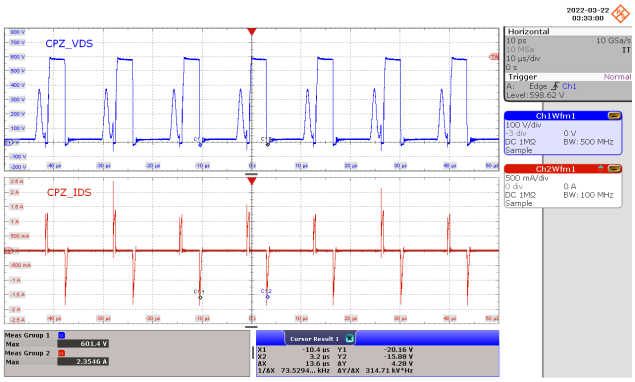


Figure 110 – ClampZero Drain Voltage and Current.
90 VAC, 20.0 V, 5 A Load.
V_{DS_CPZ} = 601 V Maximum.
CH1: V_{DS_CPZ}, 100 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

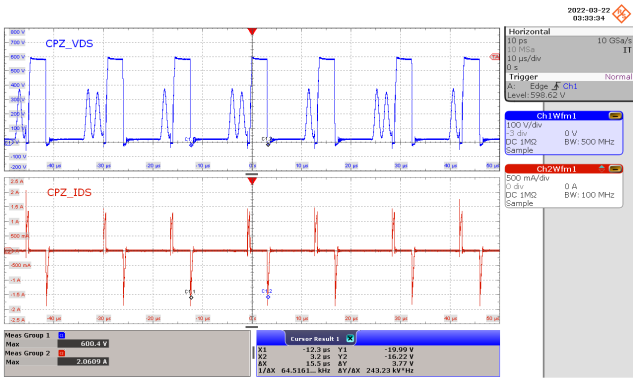


Figure 111 – ClampZero Drain Voltage and Current.
265 VAC, 20.0 V, 5 A Load.
V_{DS_CPZ} = 600 V Maximum.
CH1: V_{DS_CPZ}, 100 V / div.
CH2: I_{DS_CPZ}, 500 mA / div.
Time: 10 µs / div.

15.6 *SR FET Drain Voltage (Steady-State)*

15.6.1 Output: 5 V / 5 A

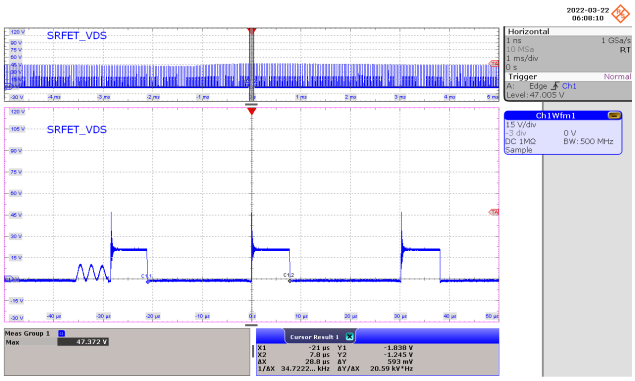


Figure 112 – SR FET Drain Voltage.
90 VAC, 5.0 V, 5 A Load.
V_{DS_SRFET} = 47.3 V Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 μs / div. Zoom)

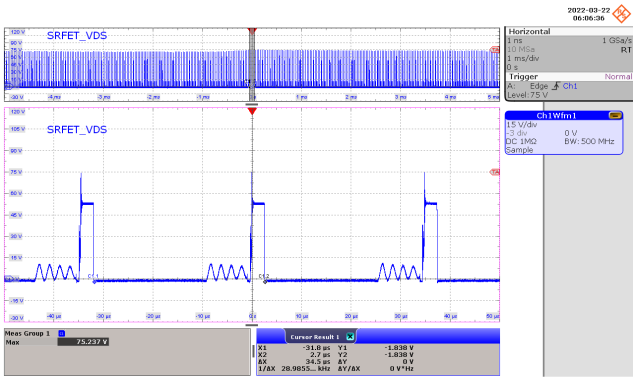


Figure 113 – SR FET Drain Voltage.
265 VAC, 5.0 V, 5 A Load.
V_{DS_SRFET} = 75.2 V Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 μs / div. Zoom)

15.6.2 Output: 9 V / 5 A

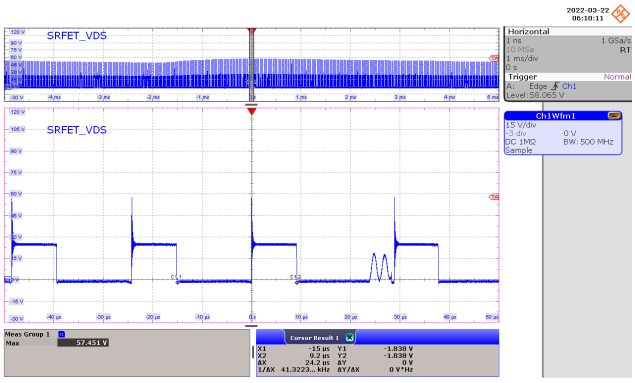


Figure 114 – SR FET Drain Voltage.
90 VAC, 9.0 V, 5 A Load.
V_{DS_SRFET} = 57.4 V Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 μs / div. Zoom)

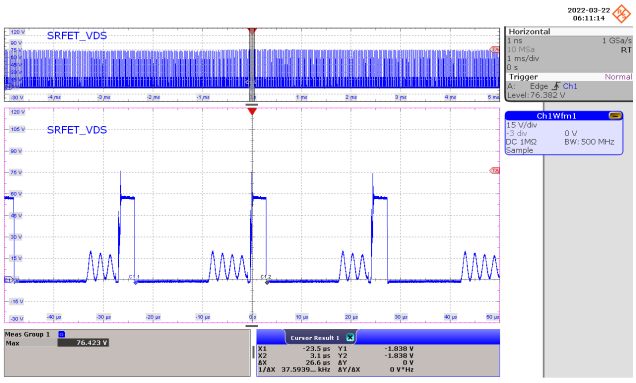


Figure 115 – SR FET Drain Voltage.
265 VAC, 9.0 V, 5 A Load.
V_{DS_SRFET} = 76.4 V Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 μs / div. Zoom)

15.6.3 Output: 12 V / 5 A

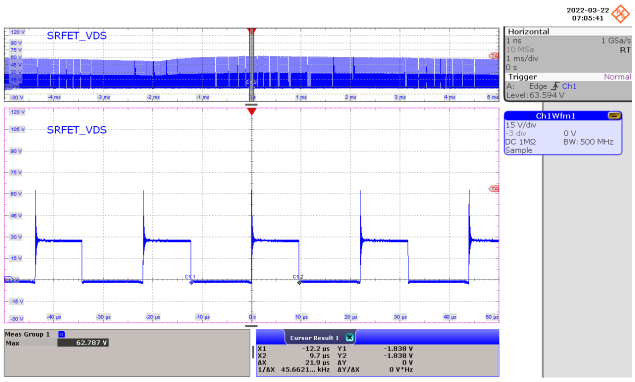


Figure 116 – SR FET Drain Voltage.
90 VAC, 12.0 V, 5 A Load.
V_{DS_SRFET} = 62.7 V Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 µs / div. Zoom)

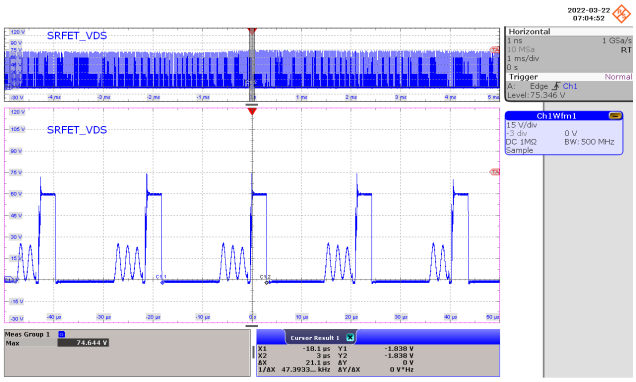


Figure 117 – SR FET Drain Voltage.
265 VAC, 12.0 V, 5 A Load.
V_{DS_SRFET} = 74.6 V Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 µs / div. Zoom)

15.6.4 Output: 15 V / 5 A

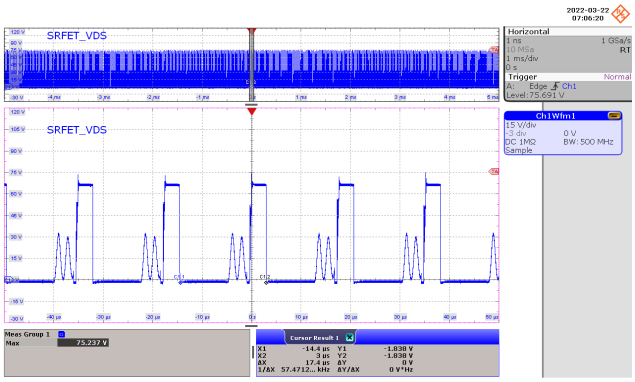


Figure 118 – SR FET Drain Voltage.
90 VAC, 15.0 V, 5 A Load.
V_{DS_SRFET} = 75.2 V Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 µs / div. Zoom)

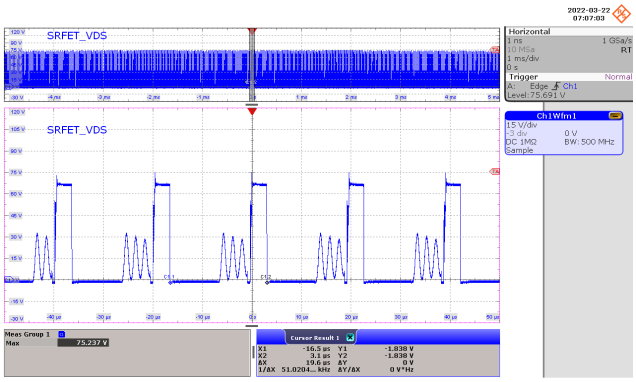


Figure 119 – SR FET Drain Voltage.
265 VAC, 15 V, 5 A Load.
V_{DS_SRFET} = 75.2 V Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 µs / div. Zoom)

15.6.5 Output: 20 V / 5 A

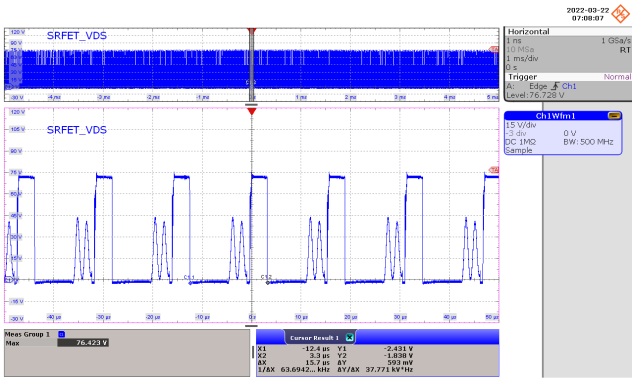


Figure 120 – SR FET Drain Voltage.
90 VAC, 20.0 V, 5 A Load.
V_{DS_SRFET} = 76.4 Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 μs / div. Zoom)

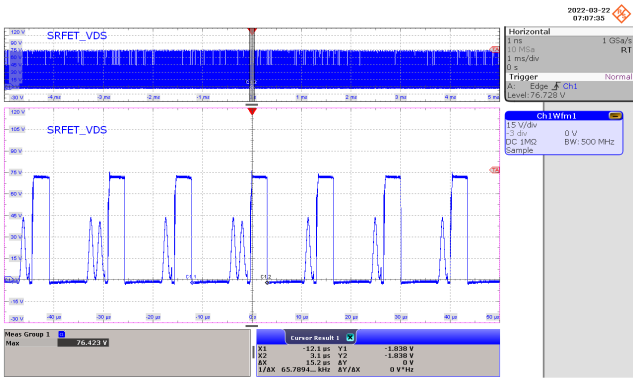


Figure 121 – SR FET Drain Voltage.
265 VAC, 20.0 V, 5 A Load.
V_{DS_SRFET} = 76.4 V Maximum.
CH1: V_{DS_SRFET}, 15 V / div.
Time: 1 ms / div. (10 μs / div. Zoom)

15.7 *Primary and SR FET Drain Voltage and Current (during Output Voltage Transition)*

15.7.1 Primary Drain Voltage and Current, 3.3 V to 21 V PPS Transition

Primary Drain Voltage, Drain Current, and output voltage on the board were captured. The USB PD Sink Request was changed from 3.3 V to 21 V / 5 A PPS (PDO6, 100 W Power-Limited) while the load current is at 4.5 A (~95% of current limit).

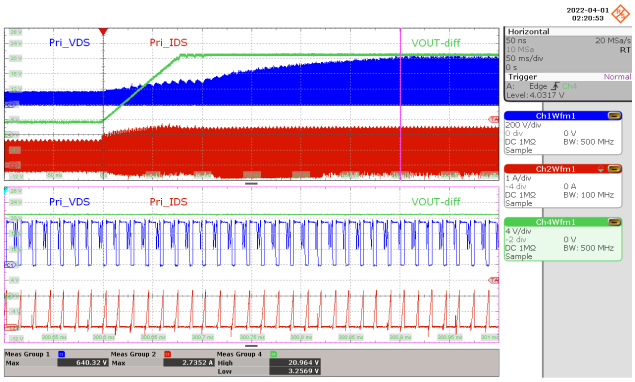


Figure 122 – Primary Drain Voltage and Current.
90 VAC, 3.3 V to 21 V V_{OUT} Transition, 4.5 A Load.
V_{DS_PRI} = 640 V Maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 1 A / div.
CH4: V_{OUT}, 4 V / div.
Time: 50 ms / div. (50 μs / div. Zoom).

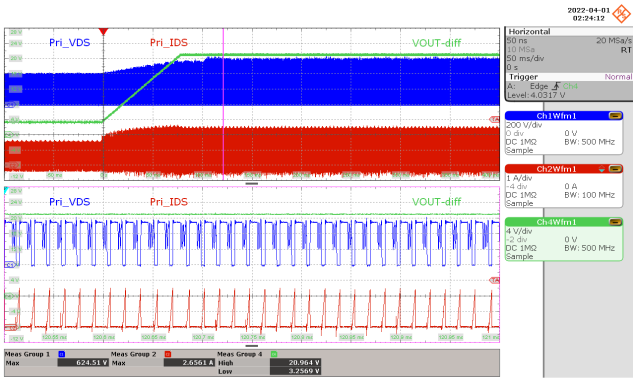


Figure 123 – Primary Drain Voltage and Current.
265 VAC, 3.3 V to 21 V V_{OUT} Transition, 4.5 A Load.
V_{DS_PRI} = 624 V Maximum.
CH1: V_{DS_PRI}, 200 V / div.
CH2: I_{DS_PRI}, 1 A / div.
CH4: V_{OUT}, 4 V / div.
Time: 50 ms / div. (50 μs / div. Zoom).

15.7.2 SR FET Drain Voltage, 3.3 V to 21 V Transition

SR FET Drain Voltage and output voltage on the board were captured. The USB PD Sink Request was changed from 3.3 V to 21 V / 5 A PPS (PDO6, 100 W Power-Limited) while the load current is at 4.5 A (95% of current limit).

Note: The maximum drain to source operating voltage rating of the SR FET is 100 V, while the maximum voltage spike can go up to 120 V for 10 µs.

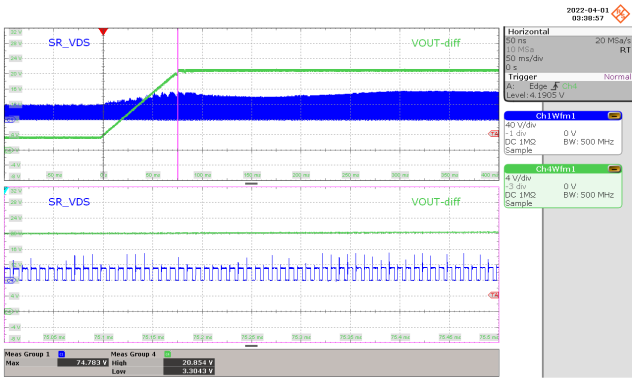


Figure 124 – SR FET Drain Voltage.
90 VAC, 3.3 V to 21 V V_{OUT} Transition, 4.5 A Load.
V_{DS_SRFET} = 74 V Maximum.
CH1: V_{DS_SRFET}, 40 V / div.
CH4: V_{OUT}, 4 V / div.
Time: 50 ms / div. (50 µs / div. Zoom).

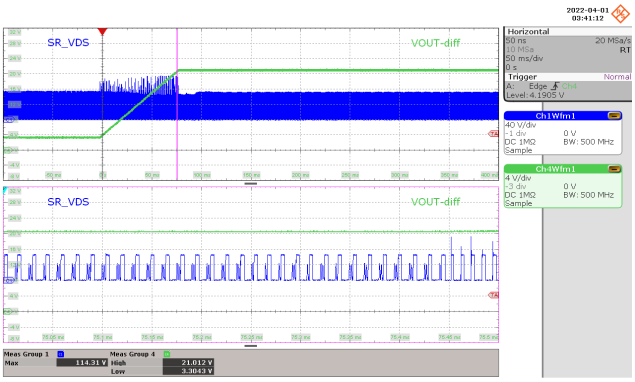


Figure 125 – SR FET Drain Voltage.
265 VAC, 3.3 V to 21 V V_{OUT} Transition, 4.5 A Load.
V_{DS_SRFET} = 114 V Maximum.
CH1: V_{DS_SRFET}, 40 V / div.
CH4: V_{OUT}, 4 V / div.
Time: 50 ms / div. (50 µs / div. Zoom).

15.8 *Load Transient Response*

Output voltage waveform on the board was captured with dynamic load transient from 10% to 100%. Duration for load states (high = 20 ms; low = 20 ms) was chosen to clearly show steady-state for each load condition. Load slew rate (150 mA / µs) is based on USB PD 3.0 specification.

USB PD 3.0 specification allows a voltage overshoot / undershoot of ±0.5 V (vSrcValid) on top of ±5% tolerance from the operating voltage (vSrcNew) within the first 5 ms of applying a load transient (tSrcTransient). Beyond 5 ms, the voltage limits are tightened to ±5% within the operating voltage.

15.8.1 Output: 5 V / 5 A

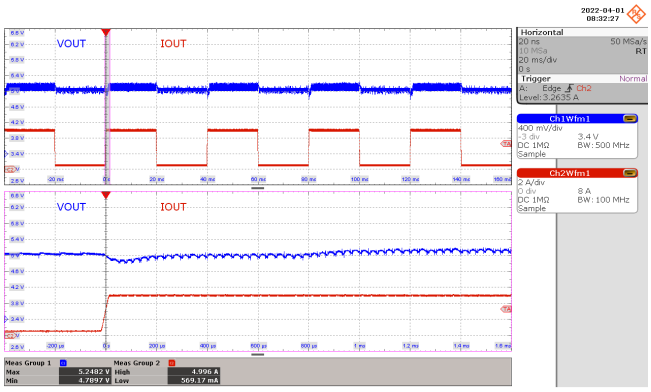


Figure 126 – Transient Response.
90 VAC, 5.0 V, 0.5 to 5 A Load.
V_{OUT} = 5.24 V Max., 4.78 V Min.
CH1: V_{OUT}, 400 mV / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

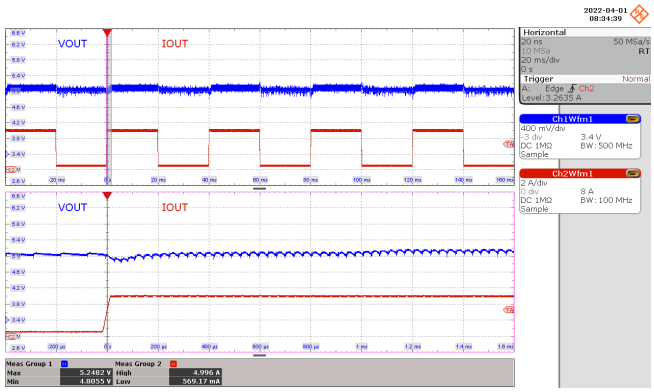


Figure 127 – Transient Response.
265 VAC, 5.0 V, 0.5 to 5 A Load.
V_{OUT} = 5.24 V Max., 4.80 V Min.
CH1: V_{OUT}, 400 mV / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

15.8.2 Output: 9 V / 5 A

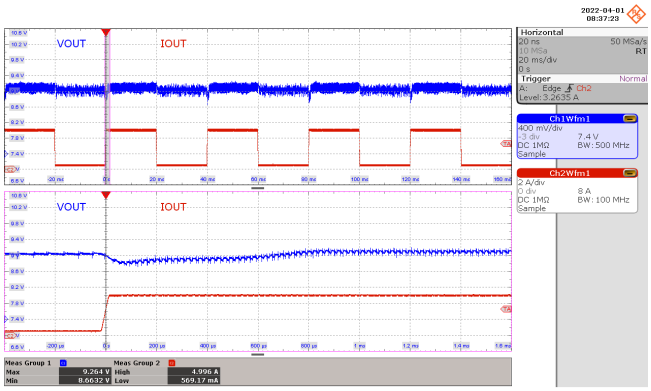


Figure 128 – Transient Response.
90 VAC, 9.0 V, 0.5 to 5 A Load.
V_{OUT} = 9.26 V Max., 8.66 V Min.
CH1: V_{OUT}, 400 mV / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

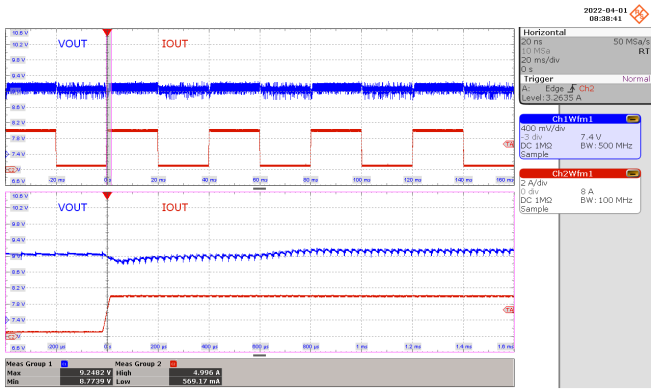


Figure 129 – Transient Response.
265 VAC, 9.0 V, 0.5 to 5 A Load.
V_{OUT} = 9.24 V Max., 8.77 V Min.
CH1: V_{OUT}, 400 mV / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

15.8.3 Output: 12 V / 5 A

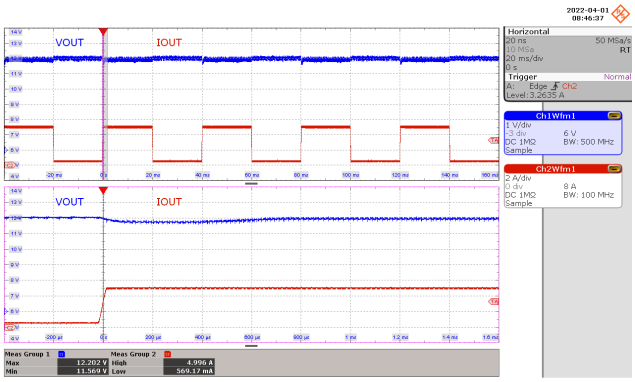


Figure 130 – Transient Response.
90 VAC, 12.0 V, 0.5 to 5 A Load.
V_{OUT} = 12.20 V Max., 11.56 V Min.
CH1: V_{OUT}, 1 V / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

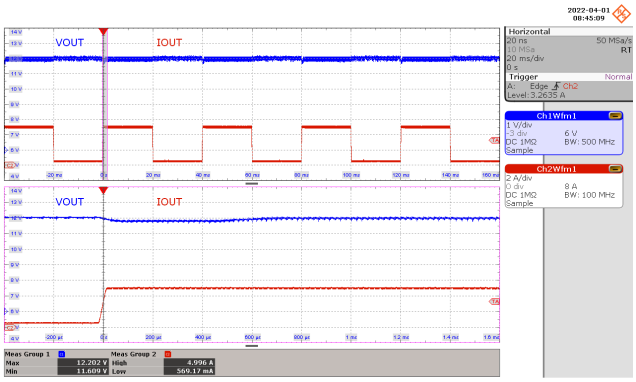


Figure 131 – Transient Response.
265 VAC, 12.0 V, 0.5 to 5 A Load.
V_{OUT} = 12.20 V Max., 11.60 V Min.
CH1: V_{OUT}, 1 V / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

15.8.4 Output: 15 V / 5 A

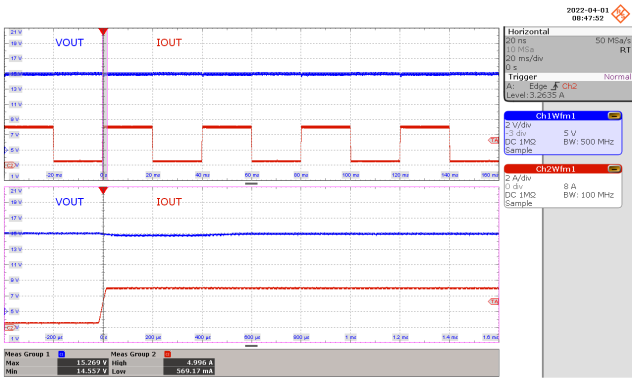


Figure 132 – Transient Response.
90 VAC, 15.0 V, 0.5 to 5 A Load.
V_{OUT} = 15.26 V Max., 14.55 V Min.
CH1: V_{OUT}, 2 V / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

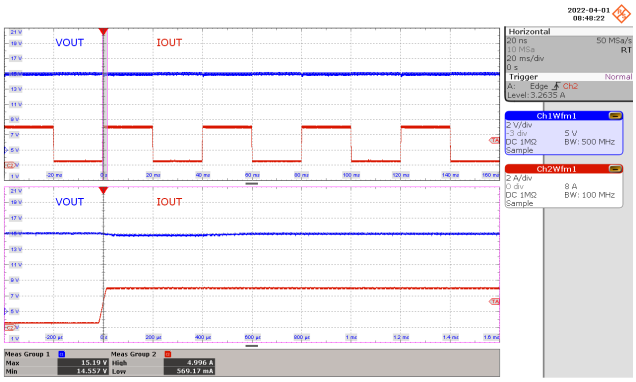


Figure 133 – Transient Response.
265 VAC, 15.0 V, 0.5 to 5 A Load.
V_{OUT} = 15.19 V Max., 14.55 V Min.
CH1: V_{OUT}, 2 V / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

15.8.5 Output: 20 V / 5 A

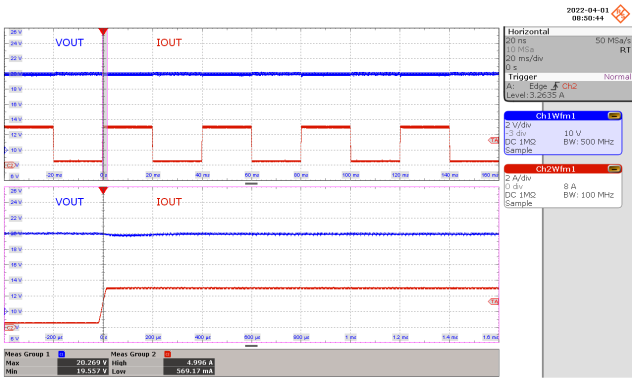


Figure 134 – Transient Response.
90 VAC, 20.0 V, 0.5 to 5 A Load.
V_{OUT} = 20.26 V Max., 19.55 V Min.
CH1: V_{OUT}, 2 V / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

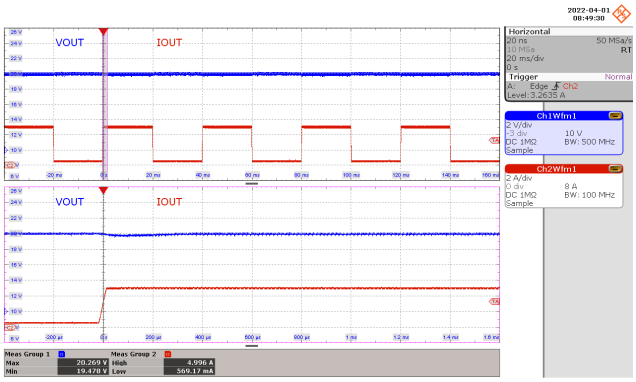


Figure 135 – Transient Response.
265 VAC, 20.0 V, 0.5 to 5 A Load.
V_{OUT} = 20.26 V Max., 19.47 V Min.
CH1: V_{OUT}, 2 V / div.
CH2: I_{OUT}, 2 A / div.
Time: 20 ms / div. (200 µs / div. Zoom).

15.9 *Output Ripple Measurements*

15.9.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

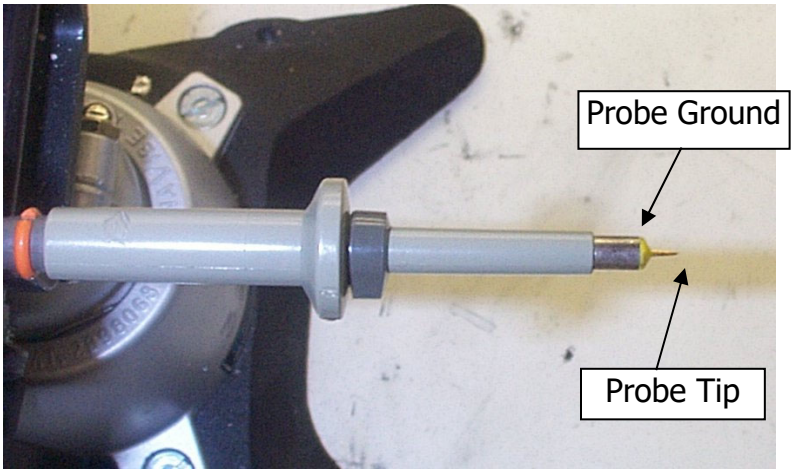


Figure 136 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

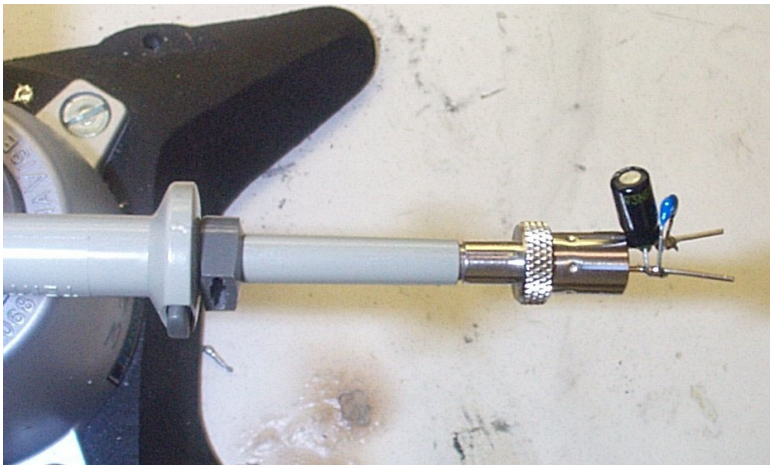


Figure 137 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

15.9.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured at the end of 100 mΩ cable using the ripple measurement probe with decoupling capacitors.

15.9.2.1 Output: 5 V / 5 A

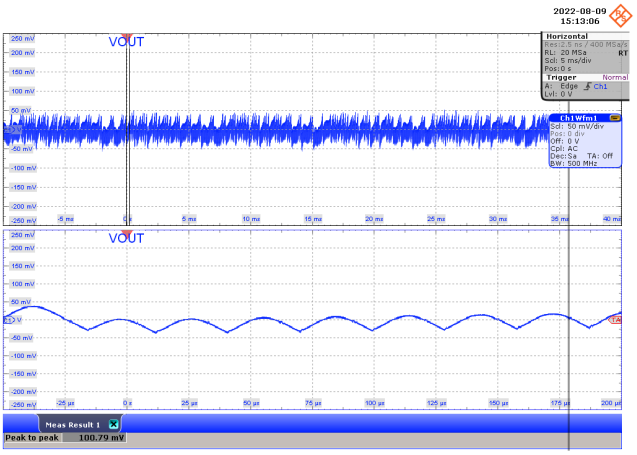


Figure 138 – Output Voltage Ripple.
90 VAC, 5.0 V, 5 A Load.
$V_{OUT(AC)}$ = 100 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

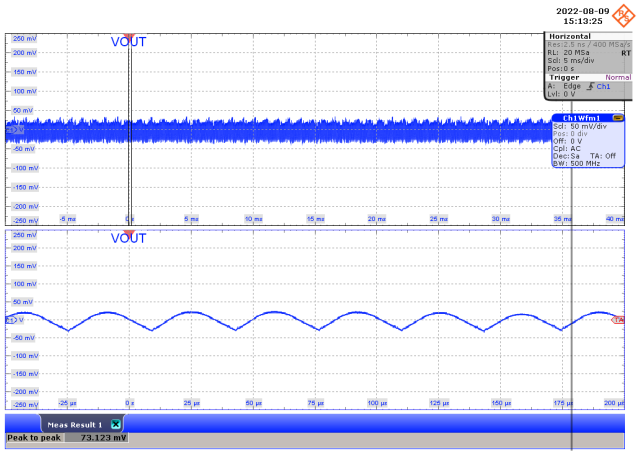


Figure 139 – Output Voltage Ripple.
265 VAC, 5.0 V, 5 A Load.
$V_{OUT(AC)}$ = 73 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

15.9.2.2 Output: 9 V / 5 A

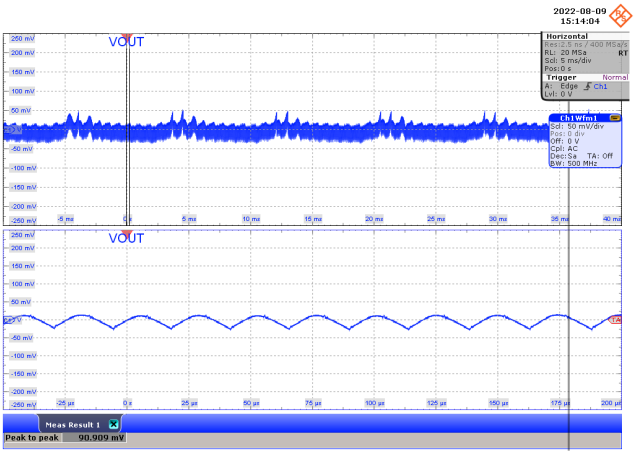


Figure 140 – Output Voltage Ripple.
90 VAC, 9.0 V, 5 A Load.
$V_{OUT(AC)}$ = 90 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

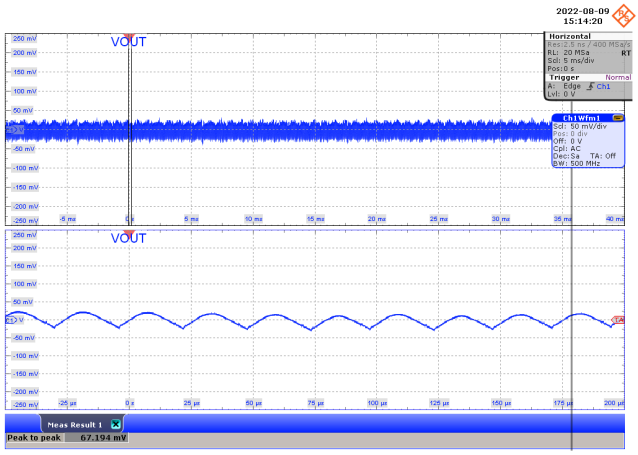


Figure 141 – Output Voltage Ripple.
265 VAC, 9.0 V, 5 A Load.
$V_{OUT(AC)}$ = 67 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

15.9.2.3 Output: 12 V / 5 A

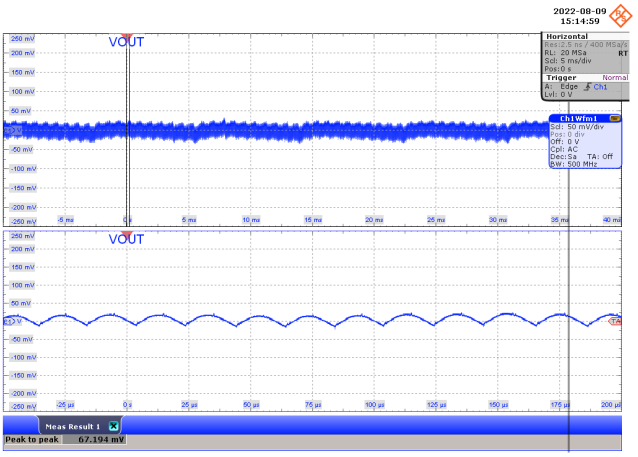


Figure 142 – Output Voltage Ripple.
90 VAC, 12.0 V, 5 A Load.
$V_{OUT(AC)}$ = 67 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

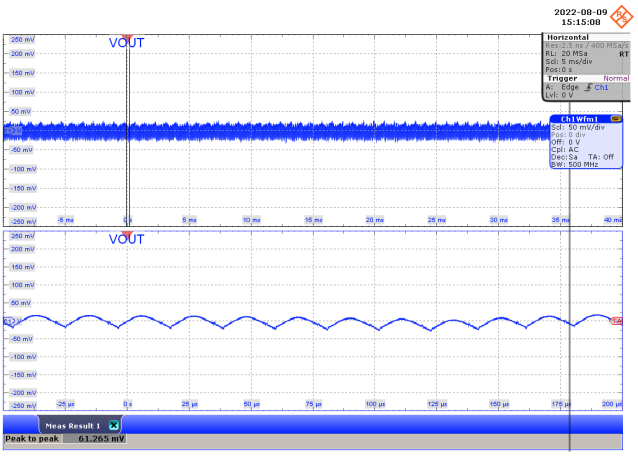


Figure 143 – Output Voltage Ripple.
265 VAC, 12.0 V, 5 A Load.
$V_{OUT(AC)}$ = 61 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

15.9.2.4 Output: 15 V / 5 A

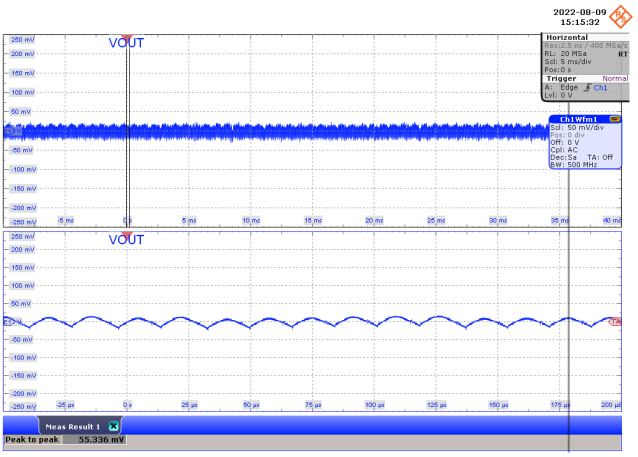


Figure 144 – Output Voltage Ripple.
90 VAC, 15.0 V, 5 A Load.
$V_{OUT(AC)}$ = 55 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

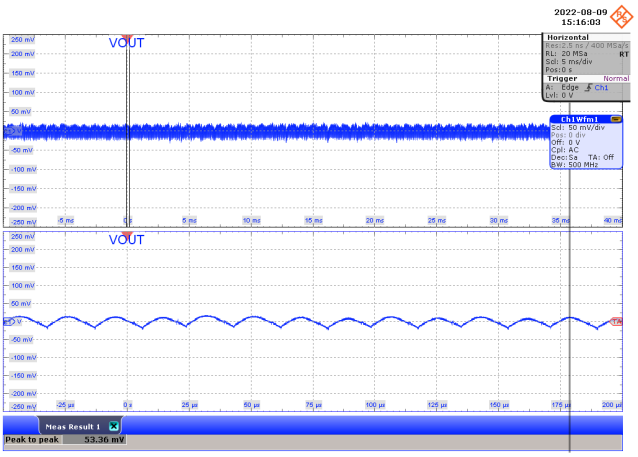


Figure 145 – Output Voltage Ripple.
265 VAC, 15.0 V, 5 A Load.
$V_{OUT(AC)}$ = 53 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

15.9.2.5 Output: 20 V / 5 A

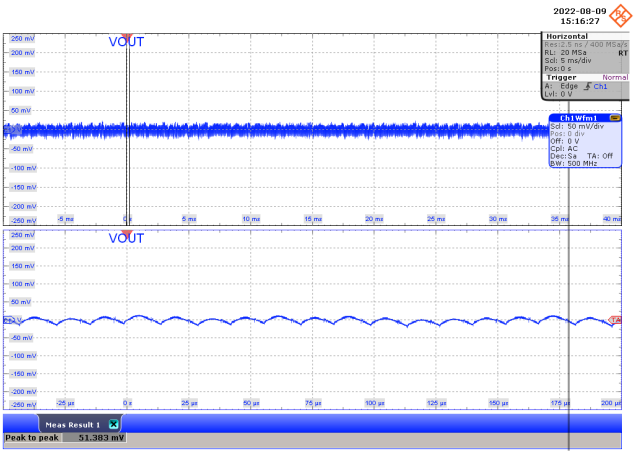


Figure 146 – Output Voltage Ripple.
90 VAC, 20.0 V, 5 A Load.
$V_{OUT(AC)}$ = 51 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

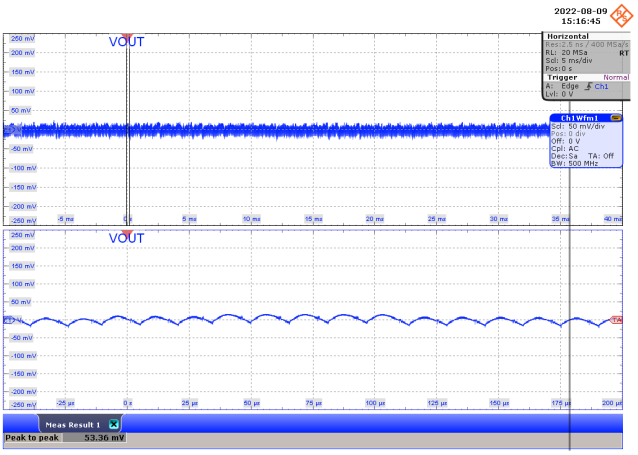


Figure 147 – Output Voltage Ripple.
265 VAC, 20.0 V, 5 A Load.
$V_{OUT(AC)}$ = 53 mV Peak-to-Peak.
CH1: $V_{OUT(AC)}$, 50 mV / div.
Time: 5 ms / div. (25 μs / div. Zoom).

15.9.3 Output Voltage Ripple Amplitude vs. Load

15.9.3.1 Output: 5 V / 5 A

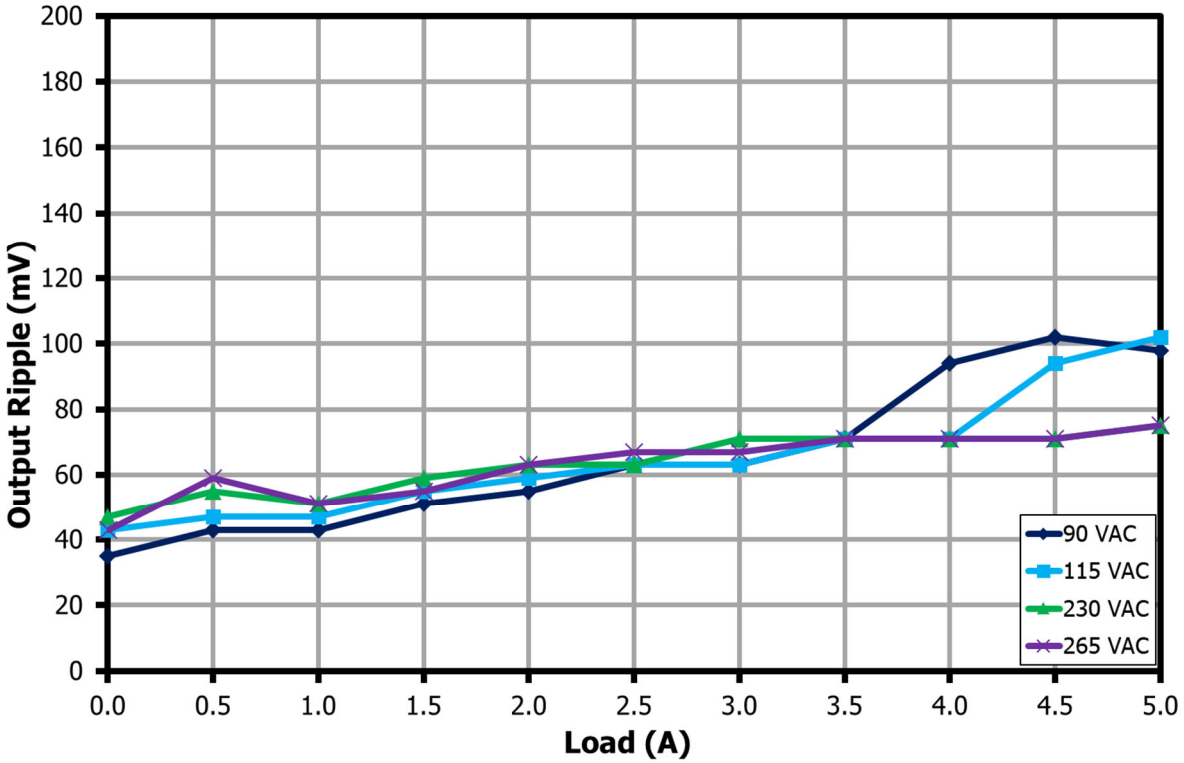


Figure 148 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 5 V Output.

15.9.3.2 Output: 9 V / 5 A

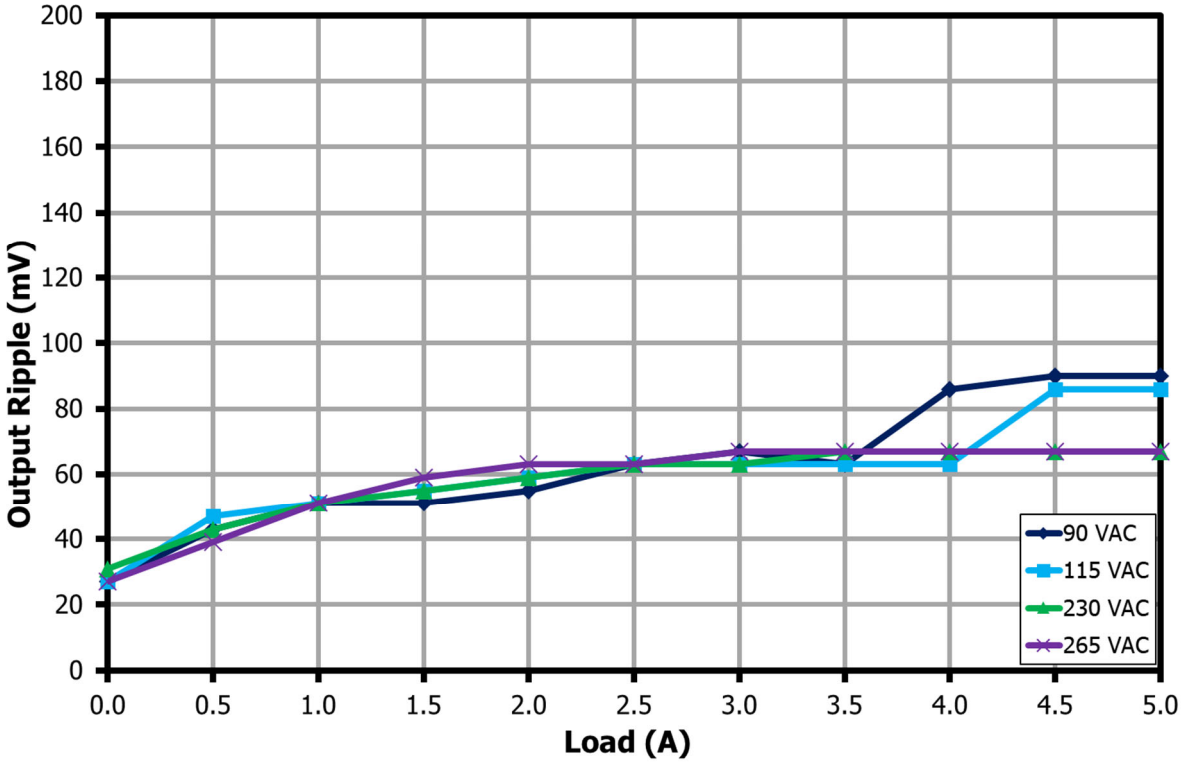


Figure 149 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 9 V Output.

15.9.3.3 Output: 12 V / 5 A

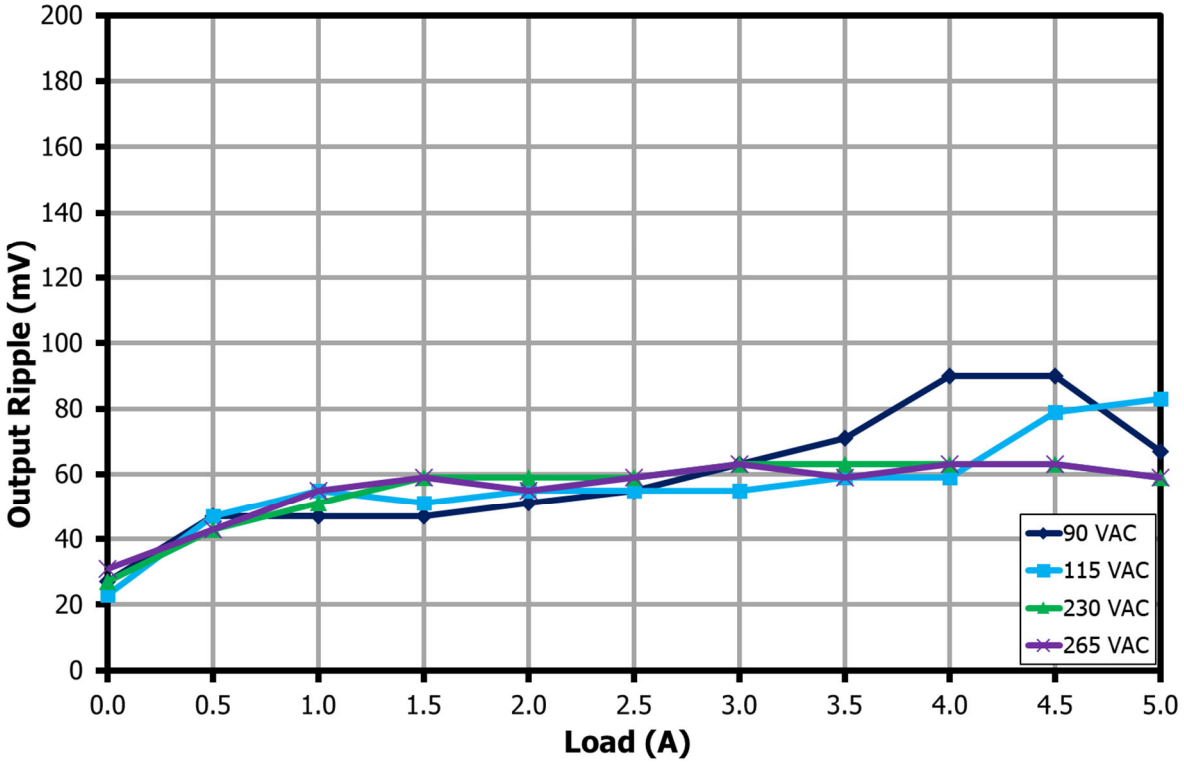


Figure 150 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 12 V Output.

15.9.3.4 Output: 15 V / 5 A

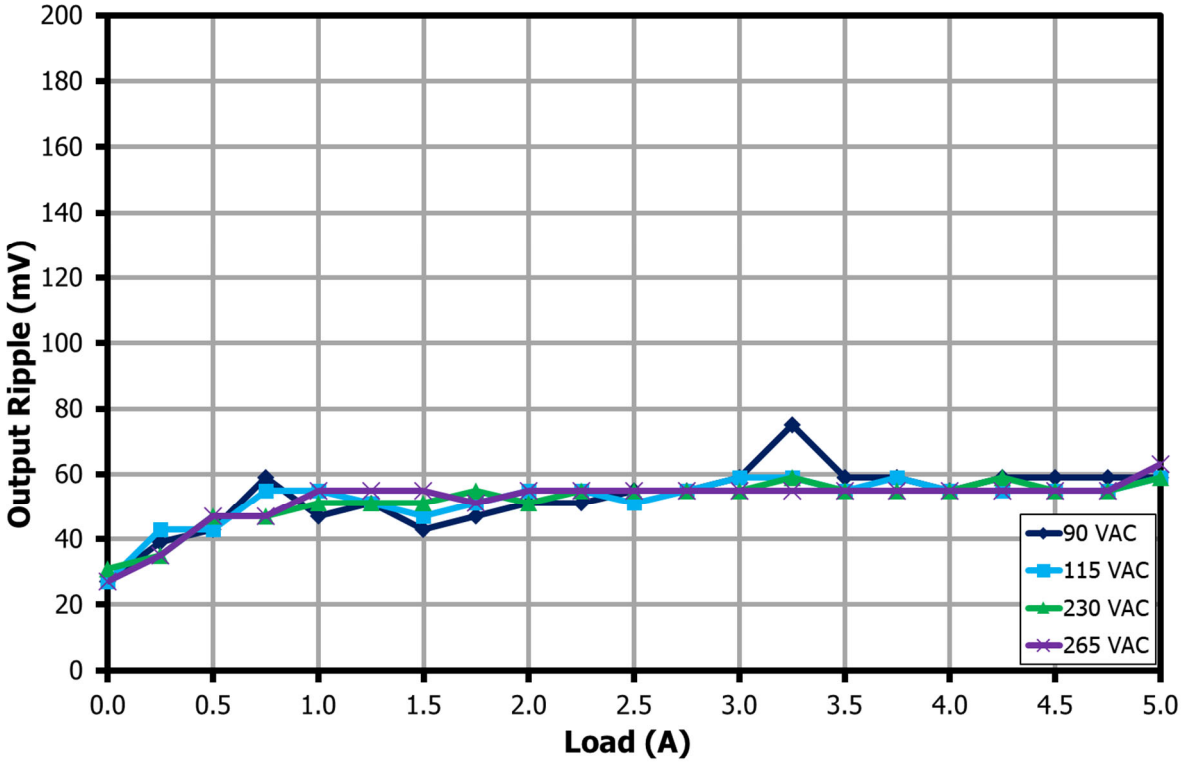


Figure 151 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 15 V Output.

15.9.3.5 Output: 20 V / 5 A

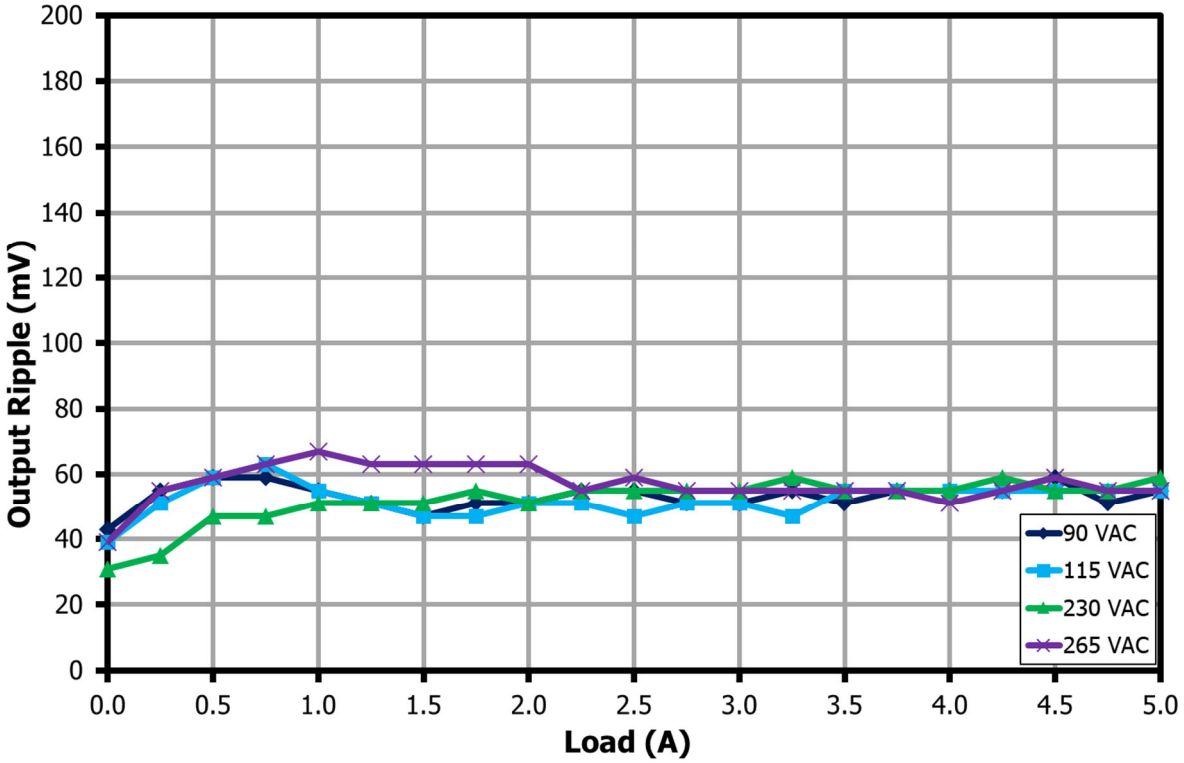


Figure 152 – Peak-to-Peak Output Voltage Ripple Amplitude vs. Load for 20 V Output.

16 CV/CC Profile

One Programmable Power Supply (PPS) Augmented Power Data Object (APDO) is supported in this design:

- PDO6: 3.3 V – 21 V / 5 A PPS (100 W power-limited)

CVCC profiles were taken with the output voltage measured on the board.

16.1 *Output: 20 V / 5 A PPS Request, PDO6 (100 W Power-Limited)*

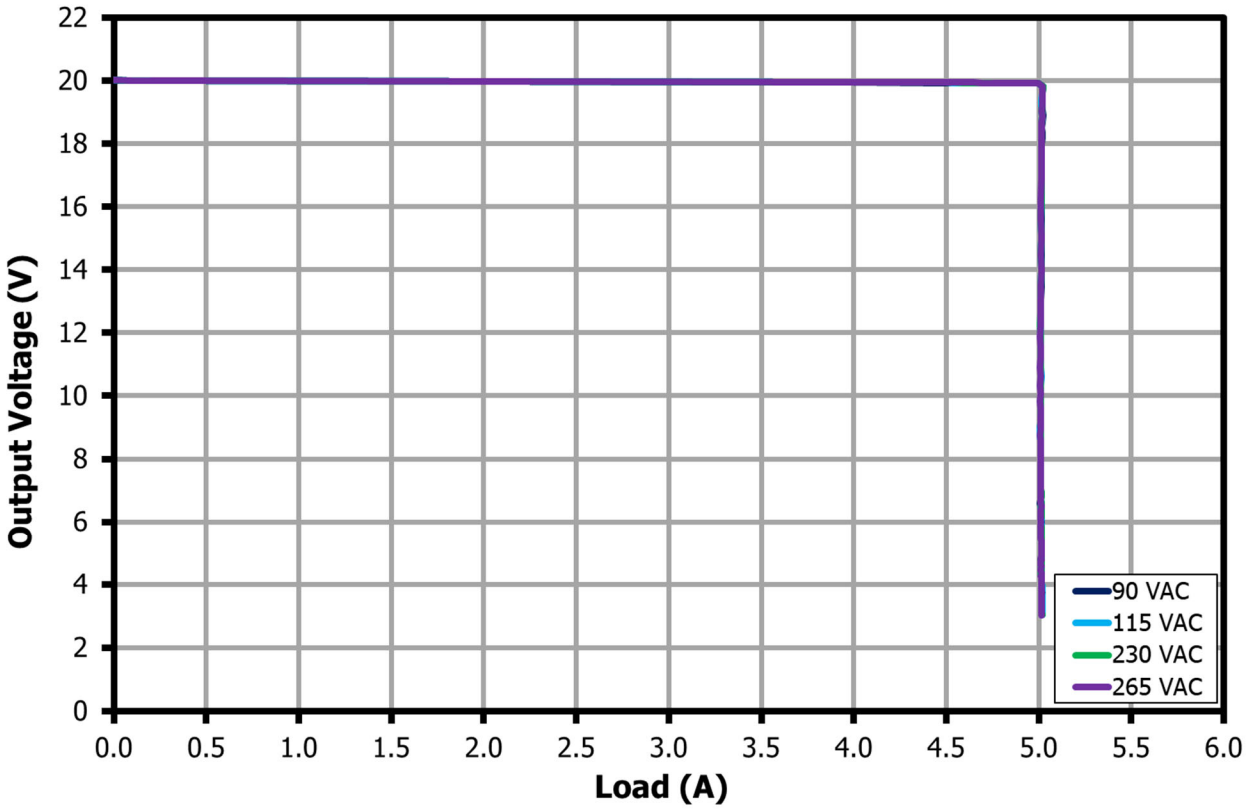


Figure 153 – CV/CC Profile for 20 V / 5 A PPS Request.

16.2 *Output: 21 V / 5 A PPS Request, PDO6 (100 W Power-Limited)*

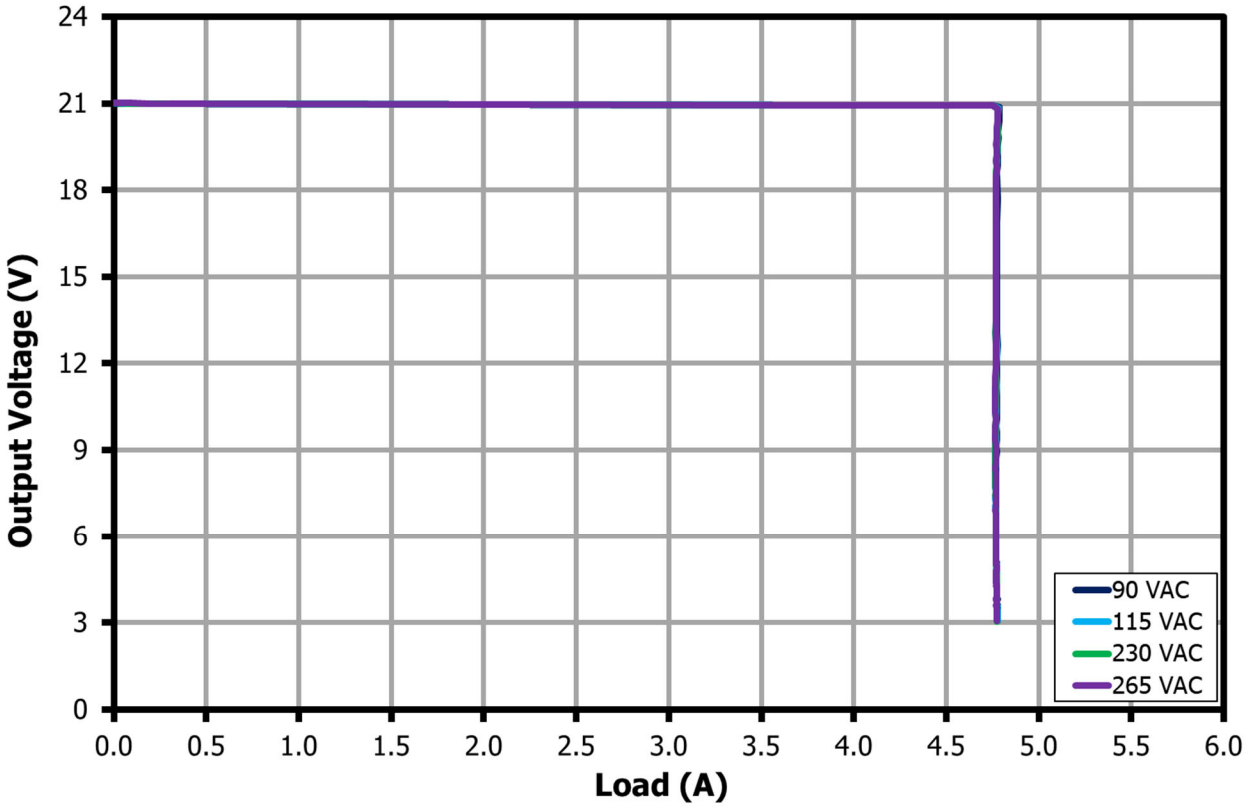


Figure 154 – CV/CC Profile for 21 V / 5 A PPS Request.

17 Voltage Step and Current Limit Test using QuadraMAX and Total Phase Analyzer

The power supply was evaluated and passed both QuadraMAX PPS Voltage Step Test (VST) and PPS Current Limit Test (CLT). The output voltage and current during VST and CLT as recorded by the Total Phase Analyzer are presented below.

17.1 *Voltage Step Test (VST)*

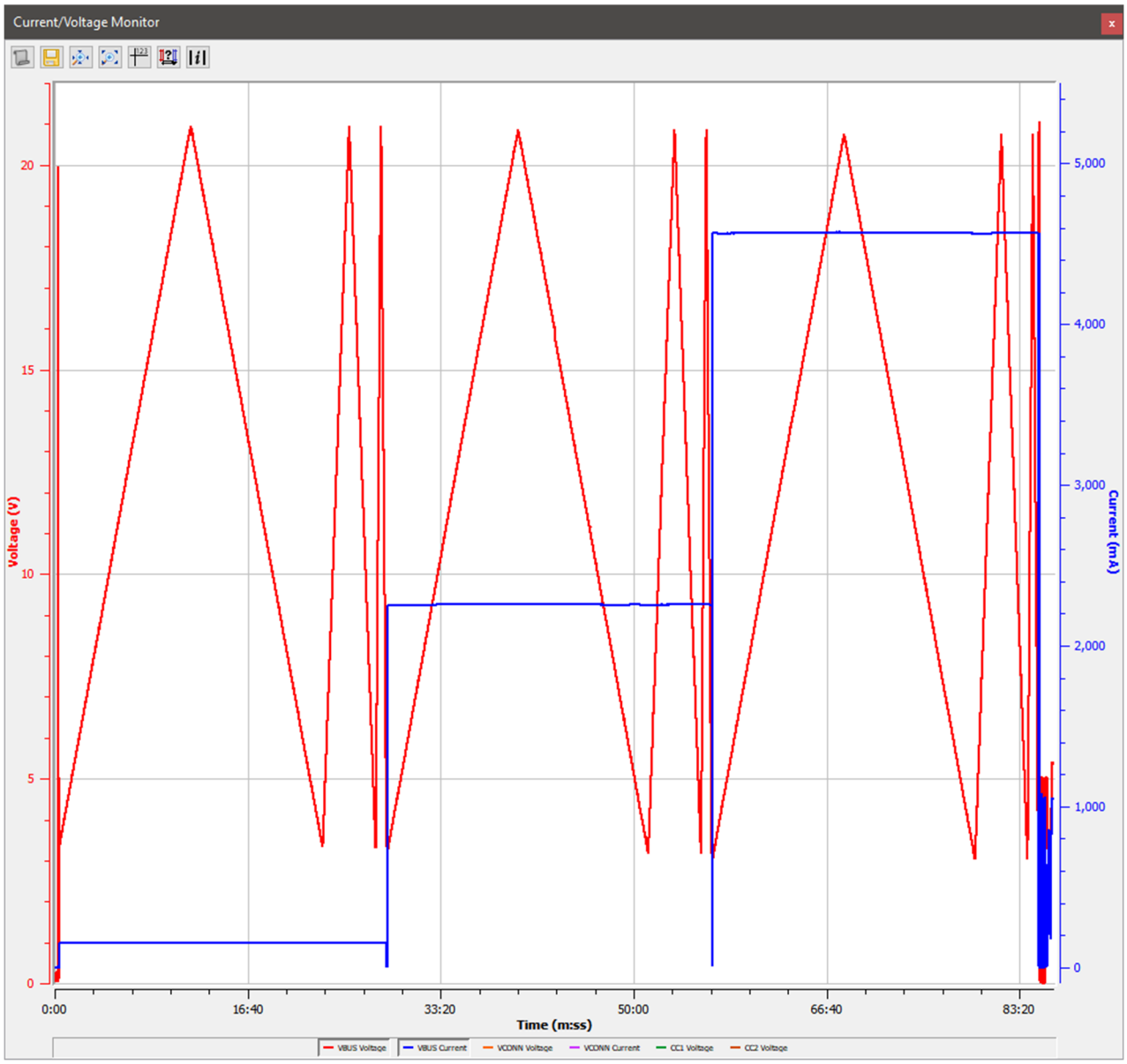


Figure 155 – Plot of SPT.6 VST from Total Phase Analyzer.

17.2 *Current Limit Test (CLT)*

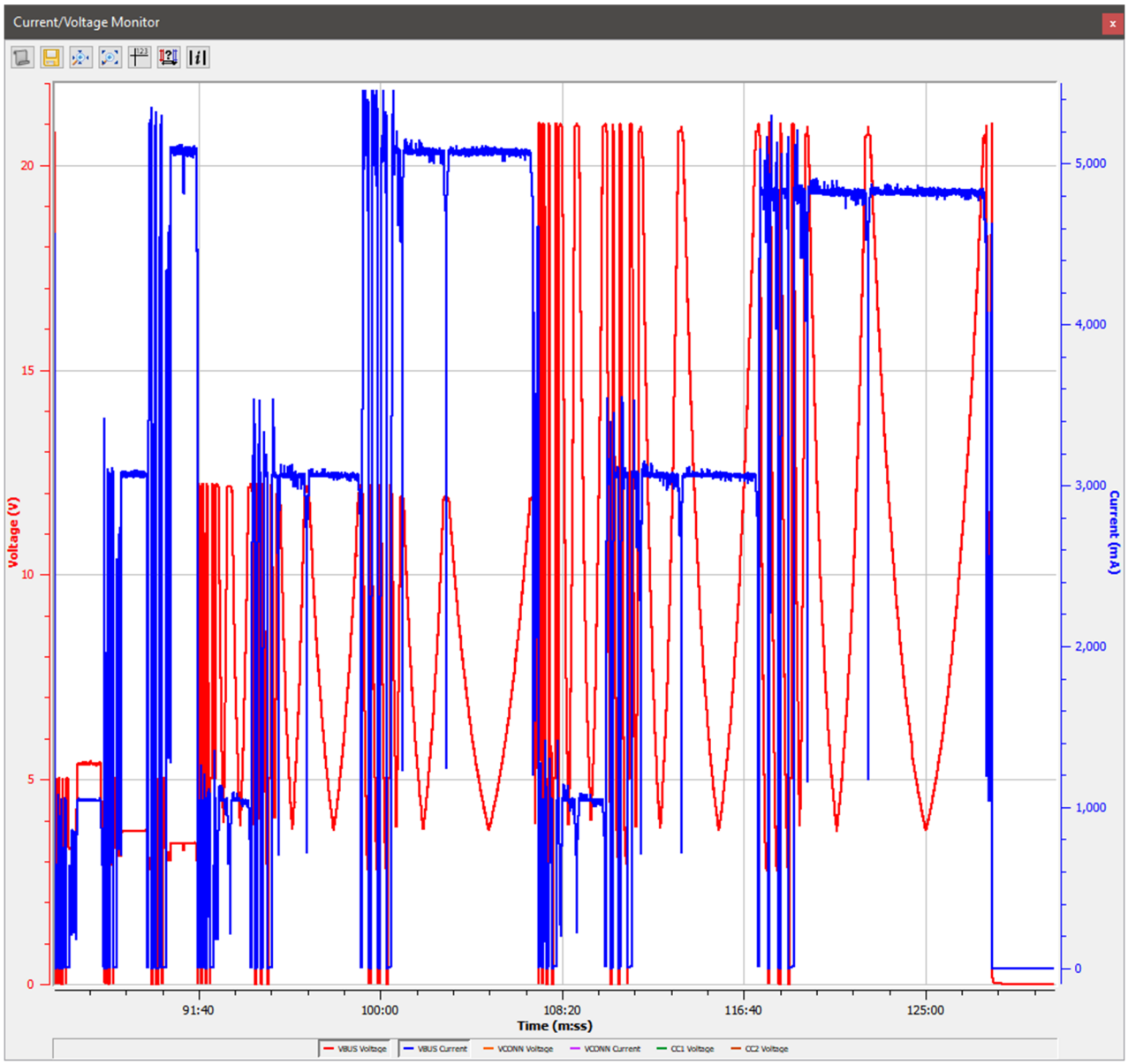


Figure 156 – Plot of SPT.7 CLT from Total Phase Analyzer.

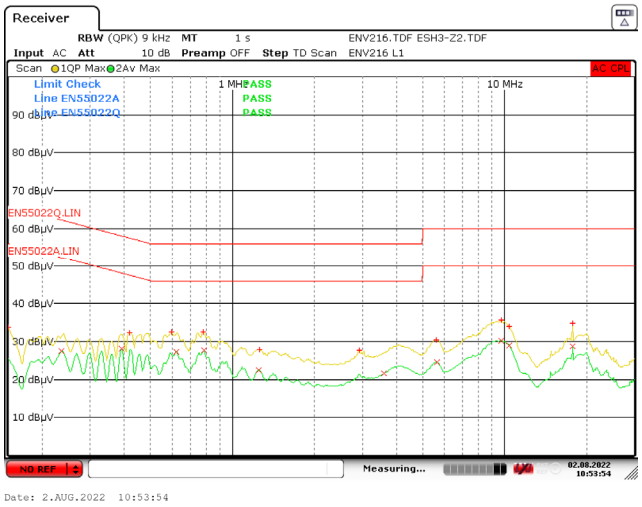
18 Conducted EMI

18.1 *Test Set-up*

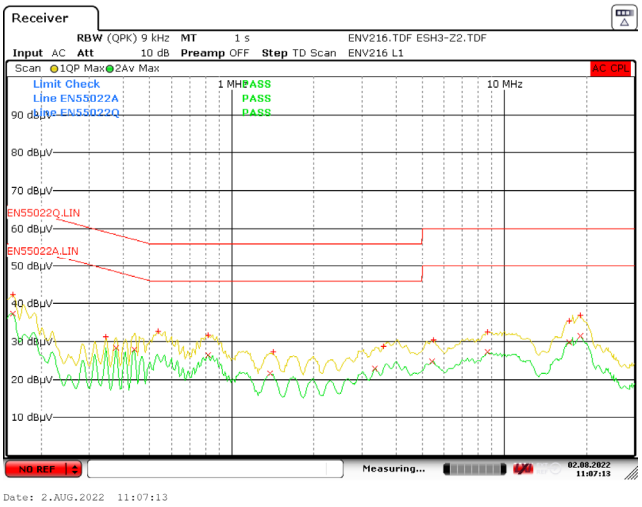
Parameter	Value
Input Voltage	115 VAC, 230 VAC
Output Voltage	5 V, 9 V, 12 V, 15 V, 20 V
Output Load	100%
Soak Time per Line	10 minutes
Termination	Floating output ground

18.2 *Floating Ground (QPK / AV)*

18.2.1 Output: 5 V / 5 A

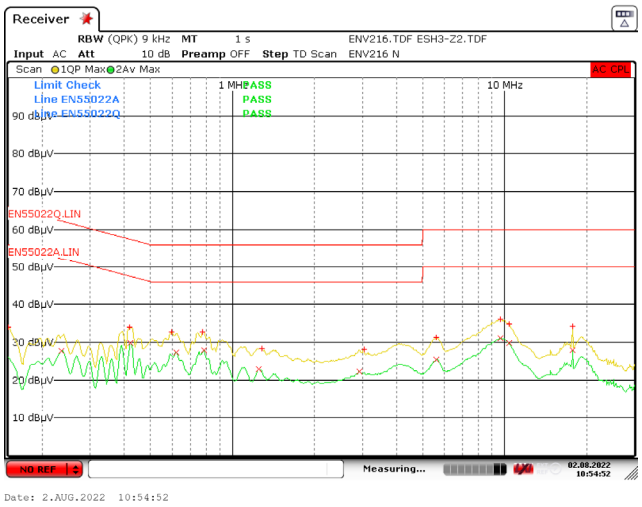


115 VAC.

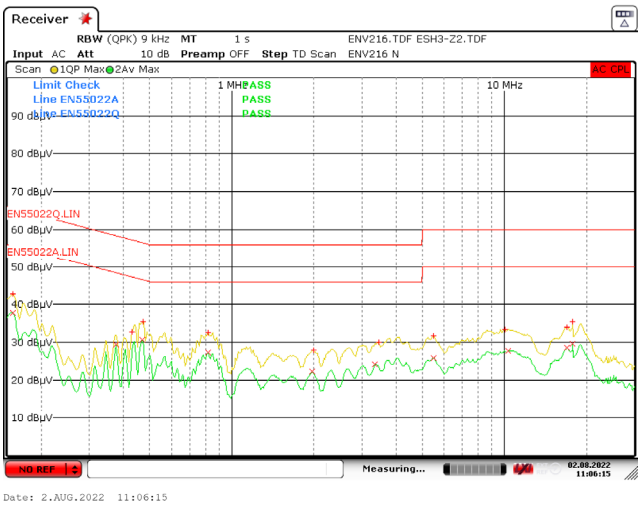


230 VAC.

Figure 157 – Floating Ground EMI, 5 V / 5 A Load [Line Scan].



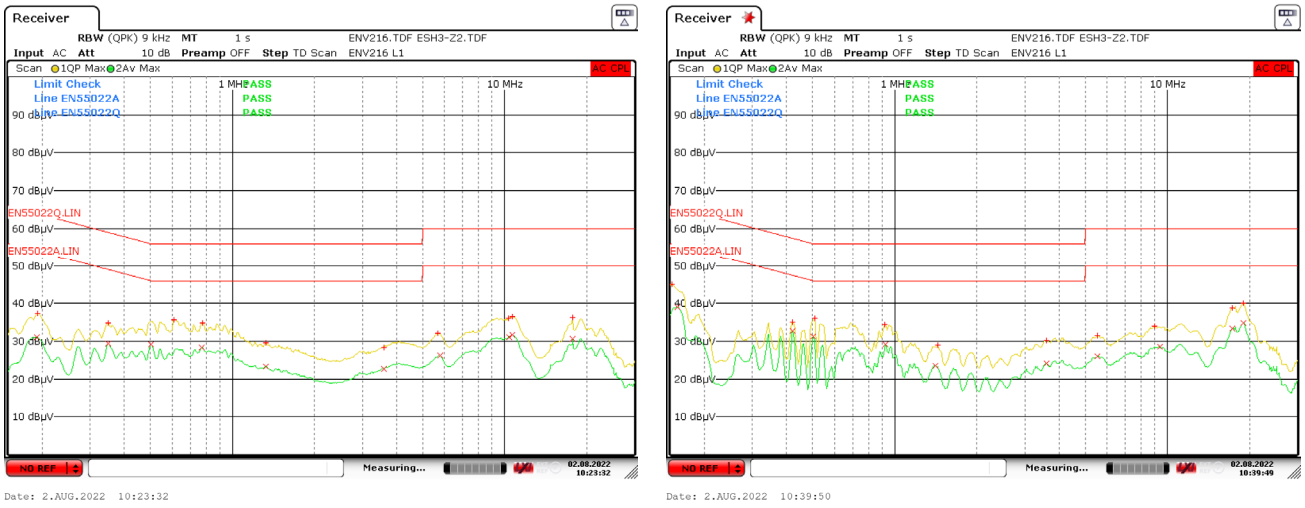
115 VAC.



230 VAC.

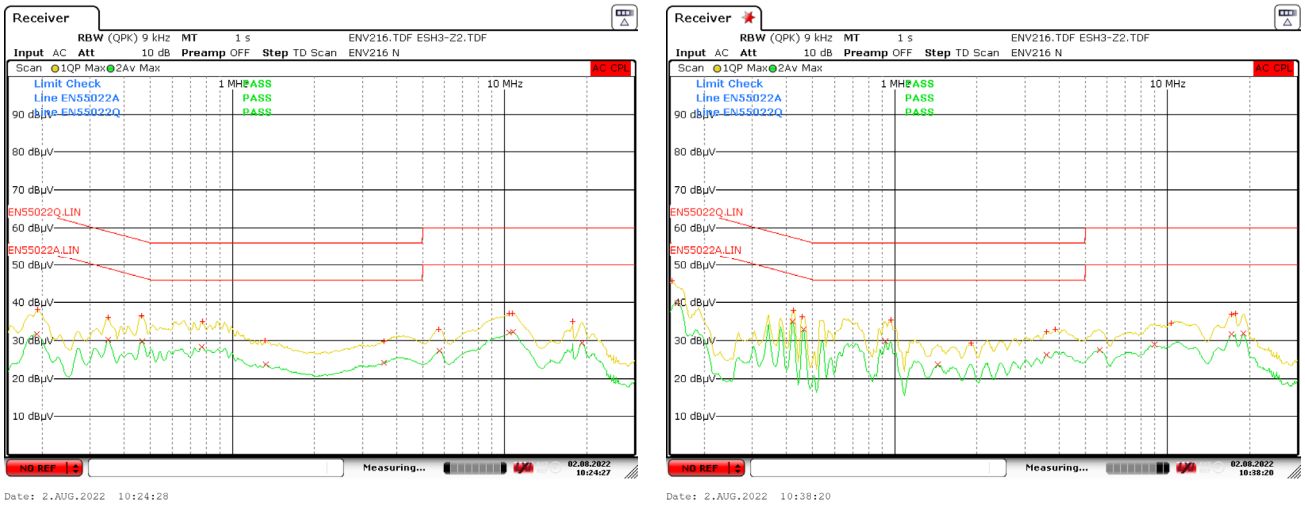
Figure 158 – Floating Ground EMI, 5 V / 5 A Load [Neutral Scan].

18.2.2 Output: 9 V / 5 A



115 VAC. 230 VAC.

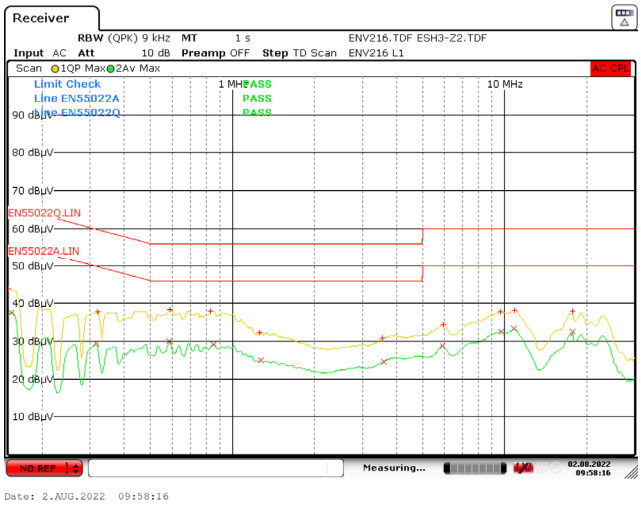
Figure 159 – Floating Ground EMI, 9 V / 5 A Load [Line Scan].



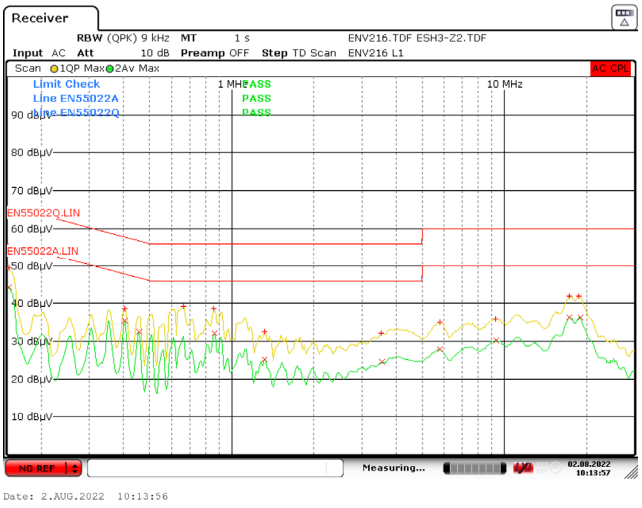
115 VAC. 230 VAC.

Figure 160 – Floating Ground EMI, 9 V / 5 A Load [Neutral Scan].

18.2.3 Output: 12 V / 5 A

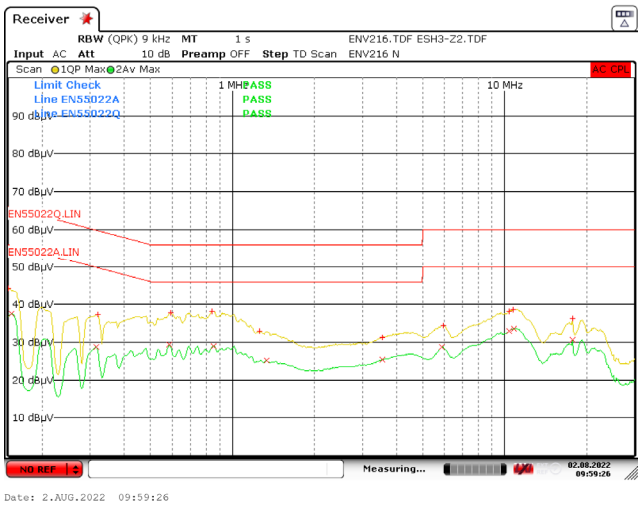


115 VAC.

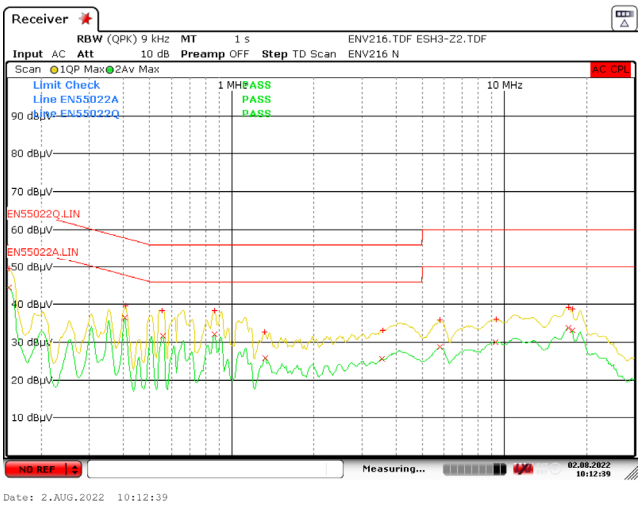


230 VAC.

Figure 161 – Floating Ground EMI, 12 V / 5 A Load [Line Scan].



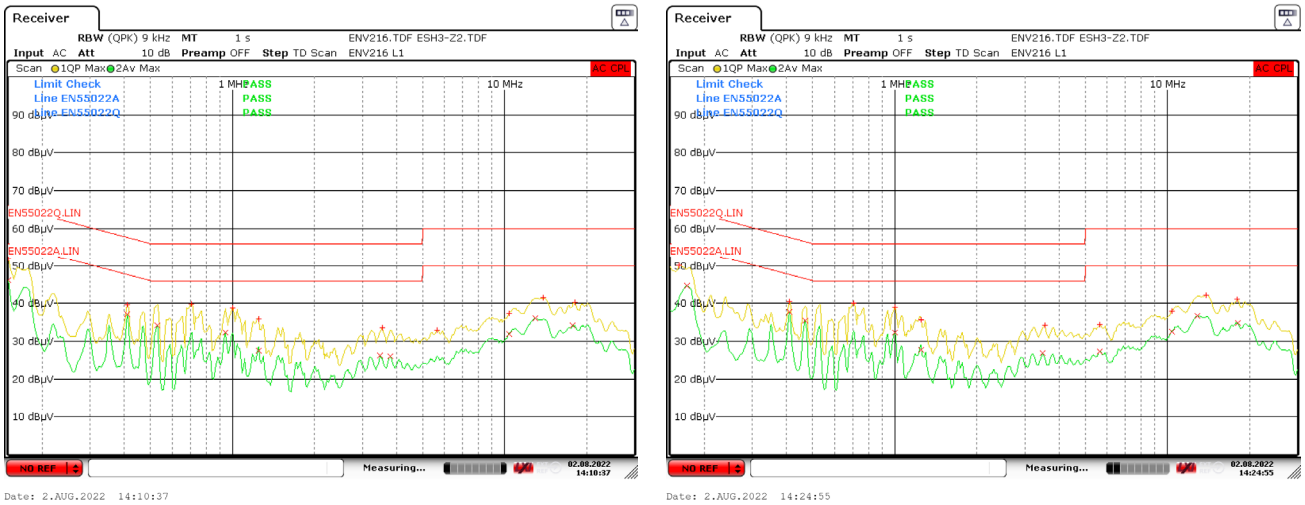
115 VAC.



230 VAC.

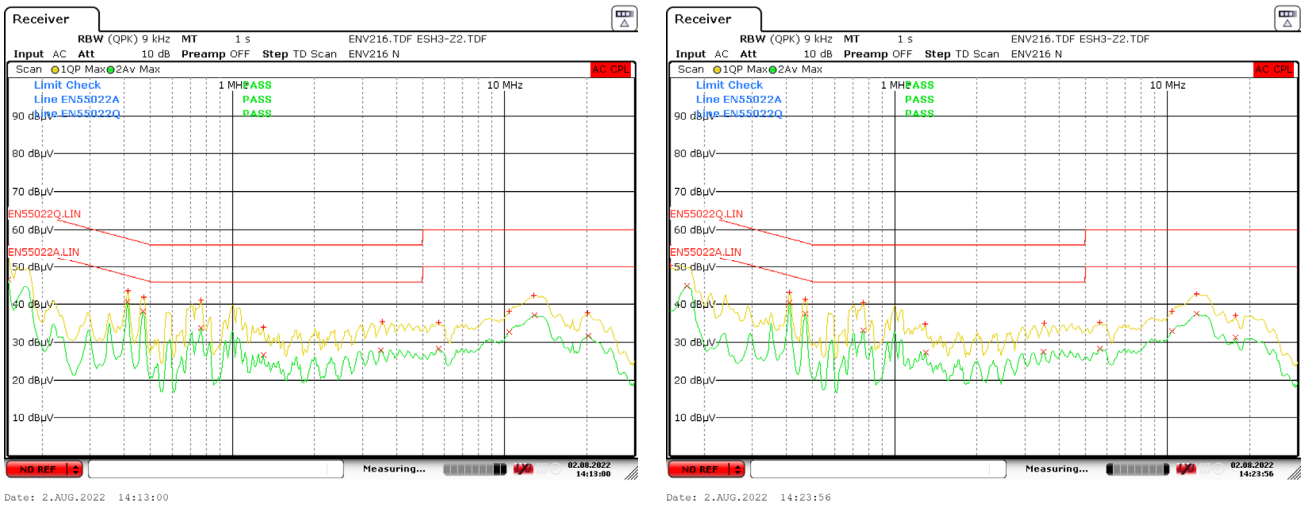
Figure 162 – Floating Ground EMI, 12 V / 5 A Load [Neutral Scan].

18.2.4 Output: 15 V / 5 A



115 VAC. 230 VAC.

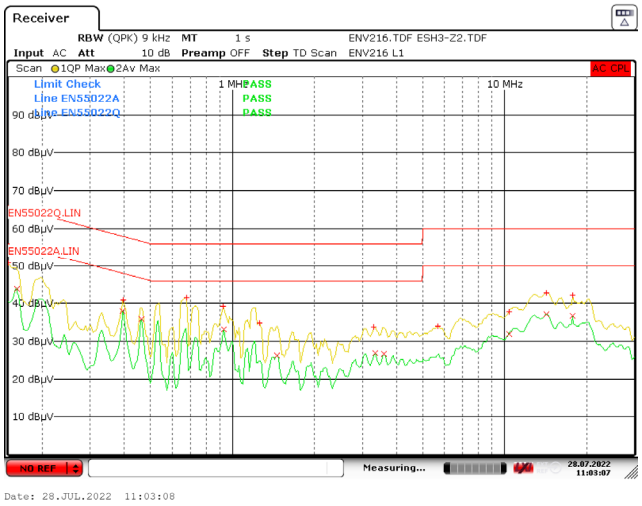
Figure 163 – Floating Ground EMI, 15 V / 5 A Load [Line Scan].



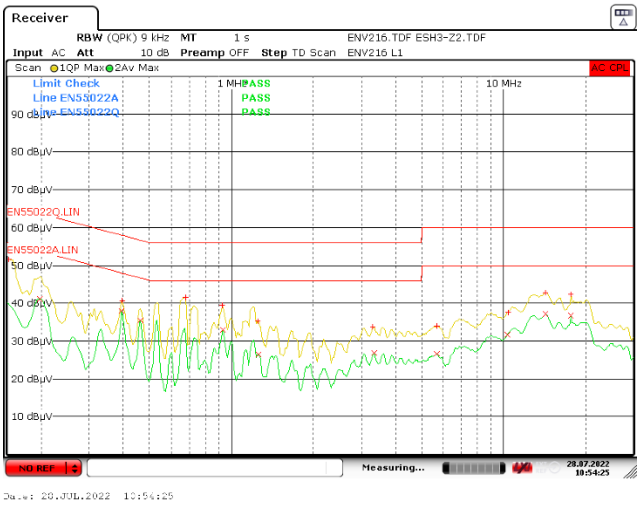
115 VAC. 230 VAC.

Figure 164 – Floating Ground EMI, 15 V / 5 A Load [Neutral Scan].

18.2.5 Output: 20 V / 5 A

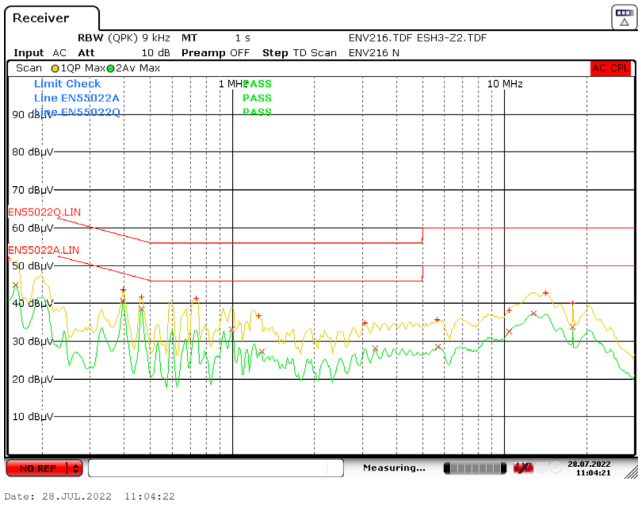


115 VAC.

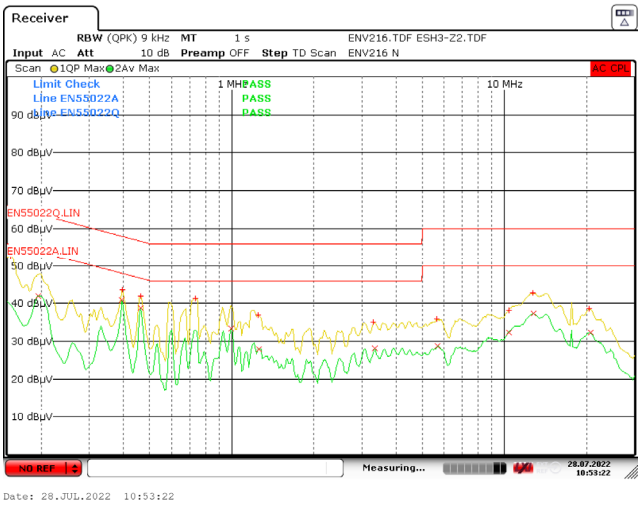


230 VAC.

Figure 165 – Floating Ground EMI, 20 V / 5 A Load [Line Scan].



115 VAC.



230 VAC.

Figure 166 – Floating Ground EMI, 20 V / 5 A Load [Neutral Scan].

19 Combination Wave Surge

The unit was subjected to ±1000 V differential mode and ±2000 V common mode combination wave surge at several line phase angles with 10 strikes for each condition.

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

19.1 *Differential Mode Surge (L1 to L2), 230 VAC Input*

19.1.1 Test Set-up

Parameter	Value
Input	230 VAC
Output	5 V / 0 A, 20 V / 5 A
Coupling	IEC (L → N)
Impedance	2Ω
Repetition Time	30 s
Number of Strikes per Test	10
Surge Voltage	±1000 V
Phase Angle	0º, 90º, 270º

19.1.2 Test Results

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 5 A
+1000	L1 to L2	0	Pass	Pass
-1000	L1 to L2	0	Pass	Pass
+1000	L1 to L2	90	Pass	Pass
-1000	L1 to L2	90	Pass	Pass
+1000	L1 to L2	270	Pass	Pass
-1000	L1 to L2	270	Pass	Pass

19.2 *Common Mode Surge (L1, L2 to PE), 230 VAC Input*

19.2.1 Test Set-up

Parameter	Value
Input	230 VAC
Output	5 V / 0 A, 20 V / 5 A
Coupling	IEC (L1, L2 → PE)
Impedance	12Ω
Repetition Time	30 s
Number of Strikes per Test	10
Surge Voltage	±2000 V
Phase Angle	0º, 90º, 270º

19.2.2 Test Results

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 5 A
+2000	L1, L2 to PE	0	Pass	Pass
-2000	L1, L2 to PE	0	Pass	Pass
+2000	L1, L2 to PE	90	Pass	Pass
-2000	L1, L2 to PE	90	Pass	Pass
+2000	L1, L2 to PE	270	Pass	Pass
-2000	L1, L2 to PE	270	Pass	Pass

19.3 *Common Mode Surge (L1 to PE), 230 VAC Input*

19.3.1 Test Set-up

Parameter	Value
Input	230 VAC
Output	5 V / 0 A, 20 V / 5 A
Coupling	IEC (L1 → PE)
Impedance	12Ω
Repetition Time	30 s
Number of Strikes per Test	10
Surge Voltage	±2000 V
Phase Angle	0º, 90º, 270º

19.3.2 Test Results

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 5 A
+2000	L1 to PE	0	Pass	Pass
-2000	L1 to PE	0	Pass	Pass
+2000	L1 to PE	90	Pass	Pass
-2000	L1 to PE	90	Pass	Pass
+2000	L1 to PE	270	Pass	Pass
-2000	L1 to PE	270	Pass	Pass

19.4 *Common Mode Surge (L2 to PE), 230 VAC Input*

19.4.1 Test Set-up

Parameter	Value
Input	230 VAC
Output	5 V / 0 A, 20 V / 5 A
Coupling	IEC (L2 → PE)
Impedance	12Ω
Repetition Time	30 s
Number of Strikes per Test	10
Surge Voltage	±2000 V
Phase Angle	0º, 90º, 270º

19.4.2 Test Results

Surge Level (V)	Injection Location	Injection Phase (°)	Test Result 5 V / 0 A without PD Sink	Test Result 20 V / 5 A
+2000	L2 to PE	0	Pass	Pass
-2000	L2 to PE	0	Pass	Pass
+2000	L2 to PE	90	Pass	Pass
-2000	L2 to PE	90	Pass	Pass
+2000	L2 to PE	270	Pass	Pass
-2000	L2 to PE	270	Pass	Pass

20 Electrostatic Discharge

The unit was tested with ±8.0 kV to ±16.5 kV air discharge and ±8.0 to ±8.8 kV contact discharge with 10 strikes for each condition at the following locations:

- End of cable +VOUT and GND
- End of cable USB PD Sink CC Lines
- On-board +VOUT and GND

A test failure was defined as an output latch-off that needs operator intervention to recover, or a complete loss of function that is not recoverable.

20.1 *VOUT and GND ESD Performance*

Discharge points were added on the board and at the end of cable on the USB PD Sink (TinyPAT) to test VOUT and GND ESD performance. A 1-meter 5 A USB Type C cable with e-marker (Veckle) was used to support 100 W load.

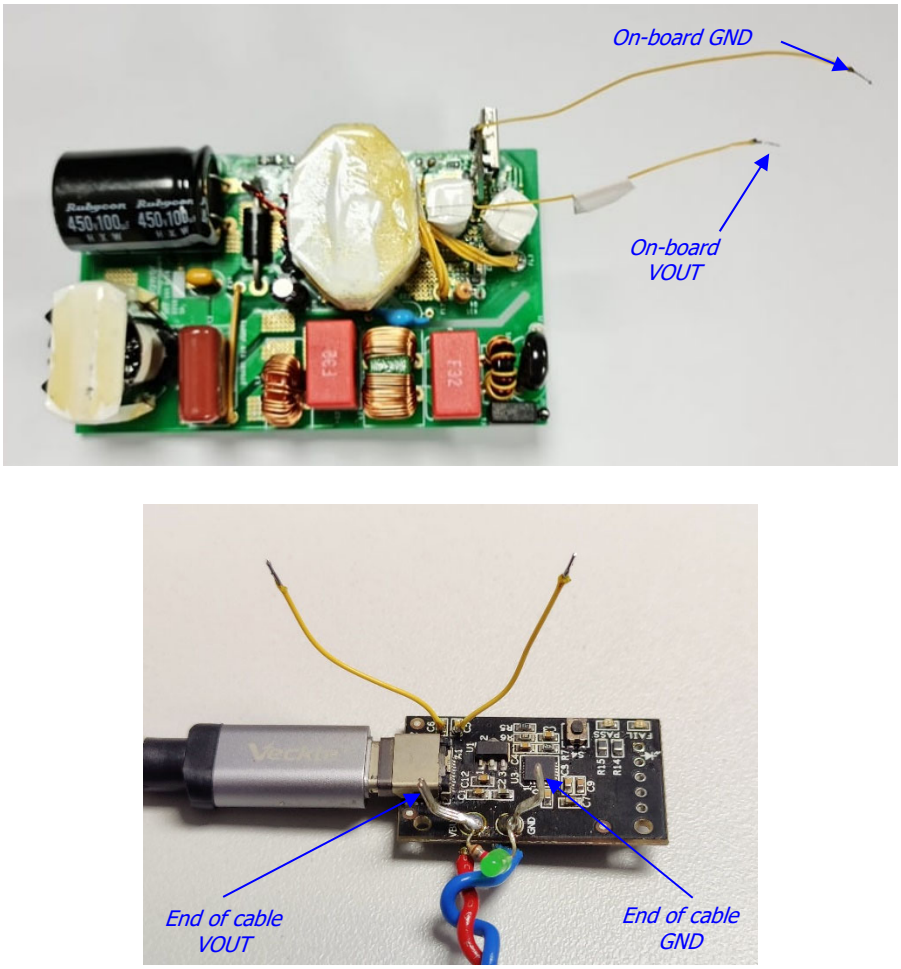


Figure 167 – ESD Discharge Points.

20.1.1 Air Discharge, End of Cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)		Test Result 20 V / 5 A	Test Result 5 V / 0 A with PD Sink
+8	End of Cable	+VOUT	Pass	Pass
		GND	Pass	Pass
-8		+VOUT	Pass	Pass
		GND	Pass	Pass
+10		+VOUT	Pass	Pass[1]
		GND	Pass	Pass
-10		+VOUT	Pass	Pass
		GND	Pass	Pass[1]
+12		+VOUT	Pass[1]	Pass[1]
		GND	Pass	Pass[1]
-12		+VOUT	Pass	Pass[1]
		GND	Pass[1]	Pass[1]
+14		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
-14		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+15		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
-15		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+16.5		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
-16.5		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]

[1]Power supply might initiate Hard Reset due to either:

- PD controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

20.1.2 Air Discharge, On-board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)		Test Result 20 V / 5 A	Test Result 5 V / 0 A with PD Sink
+8	On the Board	+VOUT	Pass	Pass
		GND	Pass	Pass
-8		+VOUT	Pass	Pass
		GND	Pass	Pass
+10		+VOUT	Pass	Pass
		GND	Pass	Pass
-10		+VOUT	Pass	Pass
		GND	Pass	Pass
+12		+VOUT	Pass	Pass[1]
		GND	Pass	Pass[1]
-12		+VOUT	Pass	Pass[1]
		GND	Pass	Pass[1]
+14		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
-14		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+15		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
-15		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
+16.5		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]
-16.5		+VOUT	Pass[1]	Pass[1]
		GND	Pass[1]	Pass[1]

[1]Power supply might initiate Hard Reset due to either:

- PD controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

20.1.3 Contact Discharge, End of Cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)		Test Result 20 V / 5 A	Test Result 5 V / 0 A with PD Sink
+8.0	End of Cable	+VOUT	Pass	Pass
		GND	Pass	Pass
-8.0		+VOUT	Pass	Pass
		GND	Pass	Pass
+8.8		+VOUT	Pass	Pass
		GND	Pass	Pass
-8.8		+VOUT	Pass	Pass
		GND	Pass	Pass

20.1.4 Contact Discharge, On the Board, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)		Test Result 20 V / 5 A	Test Result 5 V / 0 A with PD Sink
+8.0	On the Board	+VOUT	Pass[1]	Pass
		GND	Pass	Pass
-8.0		+VOUT	Pass	Pass
		GND	Pass[1]	Pass
+8.8		+VOUT	Pass[1]	Pass
		GND	Pass	Pass
-8.8		+VOUT	Pass	Pass
		GND	Pass	Pass

[1]Power supply might initiate Hard Reset due to either:

- PD controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

20.2 *CC1 and CC2 ESD Performance*

Discharge points were added to the communication lines of the USB PD Sink (TinyPAT) to test CC lines ESD performance. The two CC lines at the end of cable were differentiated by their voltage levels during the normal operation.

- Sink CC Line: Active (~1.7 V)
- Sink CC Line: Low (~0 V)

Performing ESD on CC lines using a 5 A cable with e-marker can damage the e-marker chip of the cable. A 1-meter 3 A passive USB Type C cable (Google) was used instead to evaluate the unit under test.

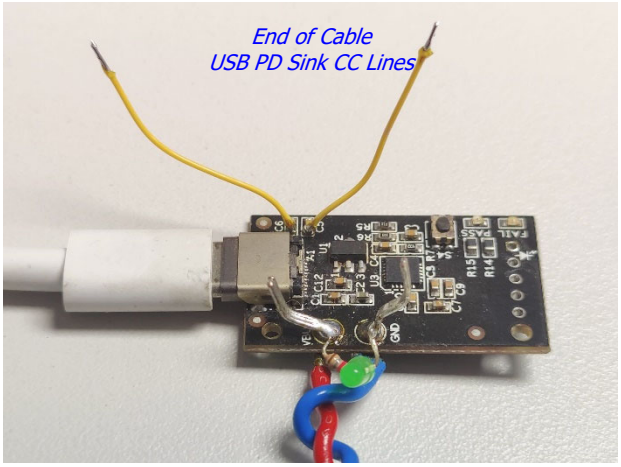


Figure 168 – ESD Discharge Points, USB PD Sink CC Lines.

20.2.1 Air Discharge, End of cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)		Test Result 5 V / 3 A
+15	End of Cable	CC Line: Active	Pass
		CC Line: Low	Pass[1]
-15		CC Line: Active	Pass[1]
		CC Line: Low	Pass[1]
+16.5		CC Line: Active	Pass[1]
		CC Line: Low	Pass[1]
-16.5		CC Line: Active	Pass[1]
		CC Line: Low	Pass

[1]Power supply might initiate Hard Reset due to either:

- PD controller protection, or
- USB-C power adapter tester Tiny-PAT protection at the load

20.2.2 Contact Discharge, End of Cable, 230 VAC Input

Discharge Voltage (kV)	ESD Strike Location (10 Strikes Each)		Test Result 5 V / 3 A
+8.0	End of Cable	CC Line: Active	Pass
		CC Line: Low	Pass
-8.0		CC Line: Active	Pass
		CC Line: Low	Pass
+8.8		CC Line: Active	Pass
		CC Line: Low	Pass
-8.8		CC Line: Active	Pass
		CC Line: Low	Pass

21 Revision History

Date	Author	Revision	Description & Changes	Reviewed
21-Oct-22	NKM/RRI	1.0	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

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