**CONCEPT**
A Power Integrations Company

2SC0635T
Preliminary Description and Application Manual

Dual-Channel Cost-Efficient Driver Core for IGBTs up to 4500V

Abstract

The 2SC0635T dual-channel SCALE™-2 driver core combines unrivalled compactness with broad applicability and cost efficiency. It is designed for industrial and traction applications requiring high reliability. The 2SC0635T drives all usual high-voltage IGBT modules up to 4500V. Its embedded paralleling capability allows easy inverter design covering higher power ratings. Multi-level topologies involving 1700V or 3300V IGBTs with higher isolation requirements can also be easily supported by 2SC0635T.

The 2SC0635T is the most compact driver core in its voltage and power range, featuring a footprint of only 75.5 x 66.8mm and an insertion height of maximum 26mm. It allows even the most restricted insertion spaces to be efficiently used.
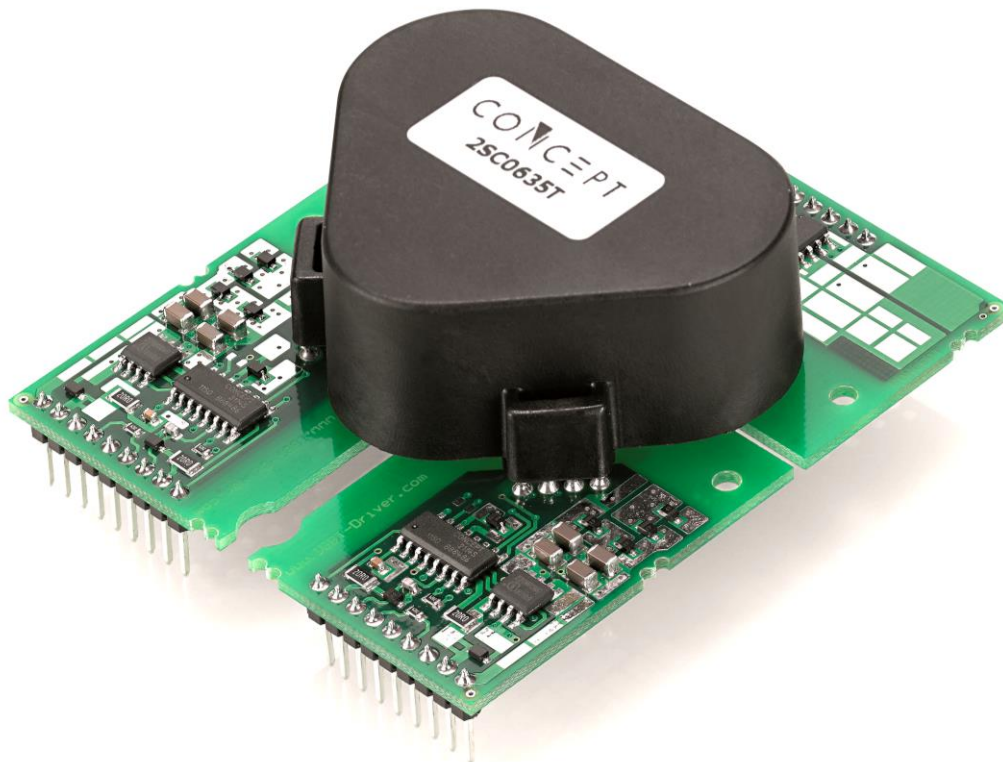
Fig. 1   2SC0635T driver core

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Driver Overview

The 2SC0635T is a driver core equipped with CONCEPT's latest SCALE-2 chipset /1/. The SCALE-2 chipset is a set of application-specific integrated circuits (ASICs) that cover the main range of functions needed to design intelligent gate drivers. The SCALE-2 driver chipset is a further development of the proven SCALE™-1 technology /2/.

The 2SC0635T targets medium- and high-power, dual-channel IGBT applications up to 4500V. The driver supports switching up to 100kHz at best-in-class efficiency. The 2SC0635T comprises a complete dual-channel IGBT driver core, fully equipped with an isolated DC/DC converter, short-circuit protection, Advanced Active Clamping and supply-voltage monitoring.
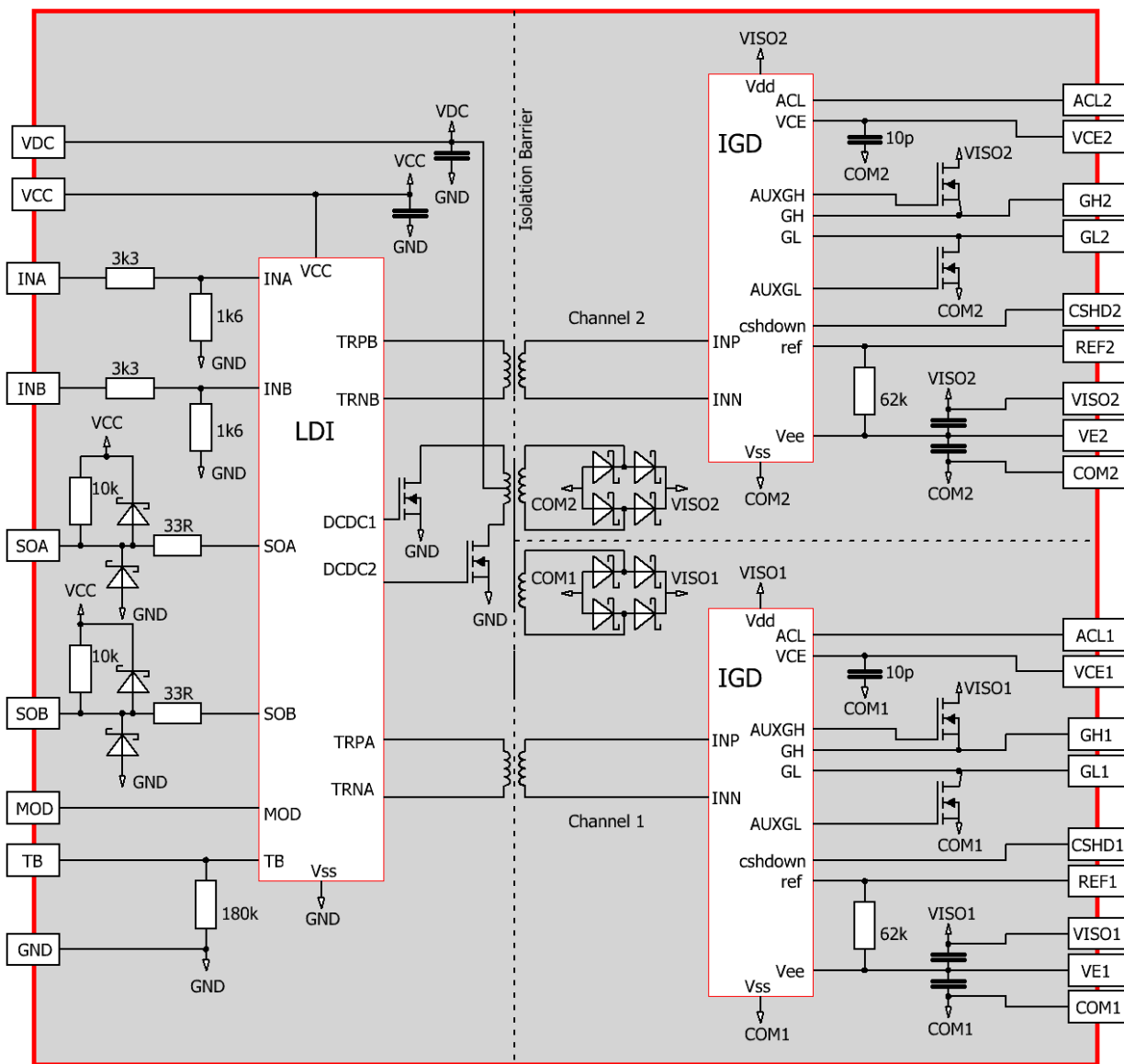
Fig. 2   Block diagram of the driver core 2SC0635T

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Mechanical Dimensions
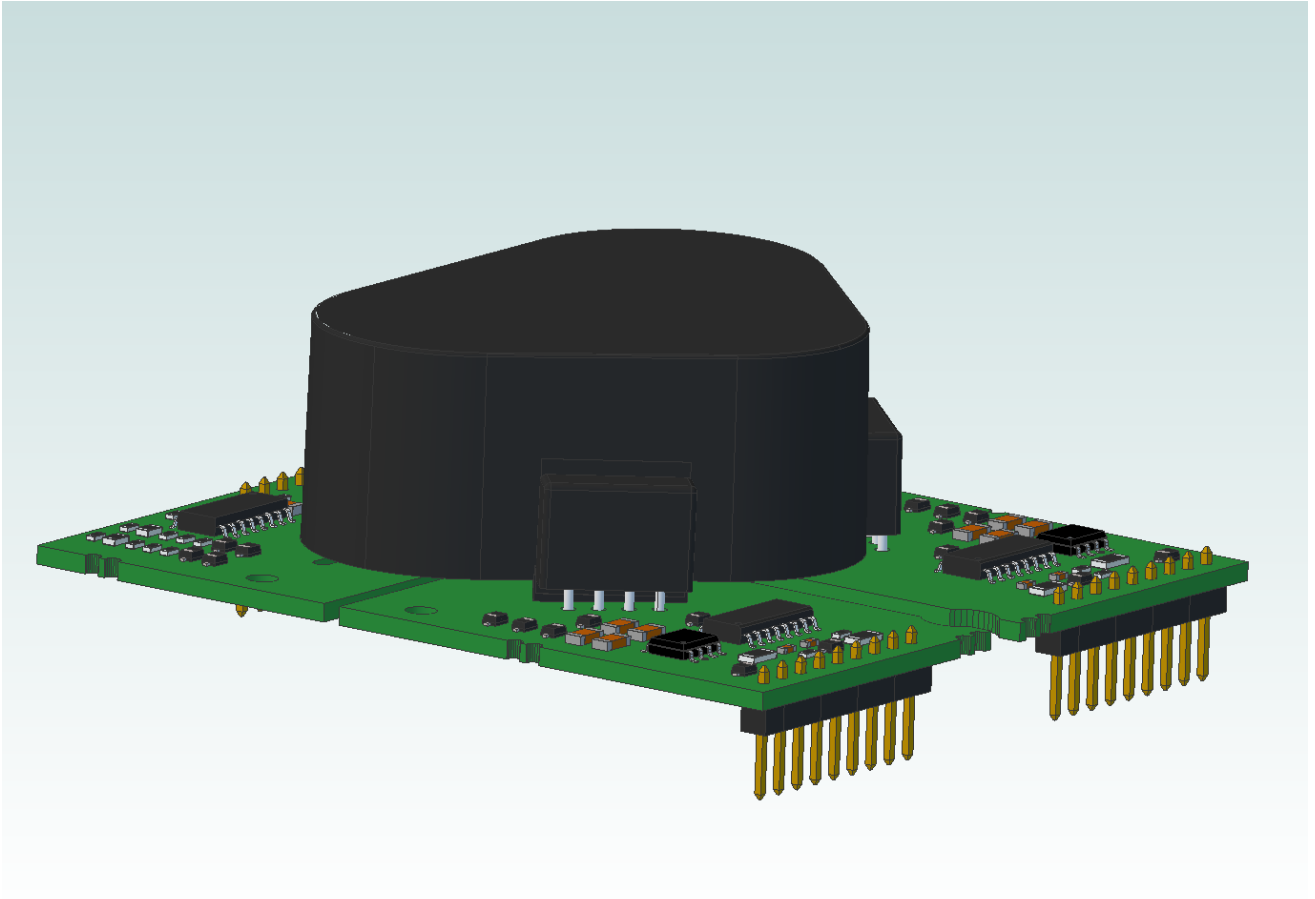
Fig. 3   Interactive 3D drawing of 2SC0635T2Ax-45

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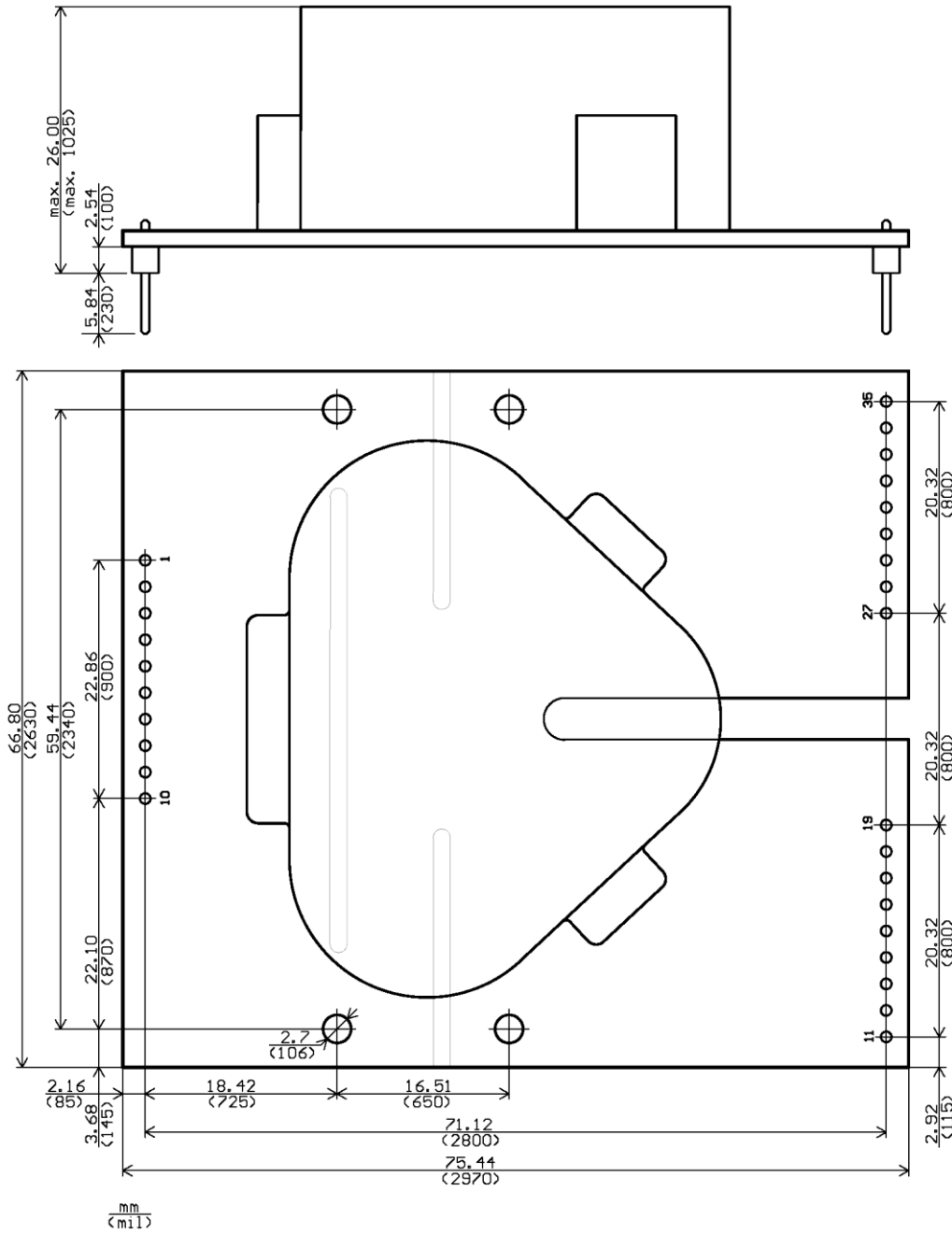
Fig. 4   Mechanical drawing of 2SC0635T2Ax-45

The primary-side and secondary-side pin grid is 2.54mm (100mil) with a pin cross section of 0.64mmx0.64mm. Total outline dimensions of the board are 66.8mmx75.5mm. The total height of the driver is maximum 26mm measured from the bottom of the pin bodies to the top of the populated PCB.

Note that the mechanical fixing points are placed in the clearance and creepage paths. Insulated fixation material (screws, distance bolts) must therefore be used in order not to reduce these.

Recommended diameter of solder pads: Ø 2mm (79 mil)
Recommended diameter of drill holes: Ø 1mm (39 mil)

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Pin Designation

Pin No. and Name	Function
Primary Side	
1 VDC	DC/DC converter supply
2 SO1	Status output channel 1; normally pulled up to VCC, pulled down to low on fault
3 SO2	Status output channel 2; normally pulled up to VCC, pulled down to low on fault
4 MOD	Mode selection (direct/half-bridge mode)
5 TB	Set blocking time
6 VCC	Supply voltage; 15V supply for primary side
7 GND	Ground
8 INA	Signal input A; non-inverting input relative to GND
9 INB	Signal input B; non-inverting input relative to GND
10 GND	Ground
Secondary Sides	
11 GL1	Gate low channel 1; pulls gate low through turn-off resistor
12 GH1	Gate high channel 1; pulls gate high through turn-on resistor
13 COM1	Secondary-side ground channel 1
14 VE1	Emitter channel 1; connect to (auxiliary) emitter of power switch
15 VISO1	DC/DC output channel 1
16 REF1	Set V_{CE} detection threshold channel 1; resistor to VE1
17 VCE1	V_{CE} sense channel 1; connect to IGBT collector through impedance network
18 ACL1	Active clamping feedback channel 1; leave open if not used
19 CSHD1	Set turn-off delay after fault detection; capacitor to COM1
20 Free	
21 Free	
22 Free	
23 Free	
24 Free	
25 Free	
26 Free	
27 CSHD2	Set turn-off delay after fault detection; capacitor to COM2
28 ACL2	Active clamping feedback channel 2; leave open if not used
29 VCE2	V_{CE} sense channel 2; connect to IGBT collector through impedance network
30 REF2	Set V_{CE} detection threshold channel 2; resistor to VE2
31 VISO2	DC/DC output channel 2
32 VE2	Emitter channel 2; connect to (auxiliary) emitter of power switch
33 COM2	Secondary-side ground channel 2
34 GH2	Gate high channel 2; pulls gate high through turn-on resistor
35 GL2	Gate low channel 2; pulls gate low through turn-off resistor

Note: Pins with the designation "Free" are not physically present.

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Recommended Interface Circuitry for the Primary-Side Connector
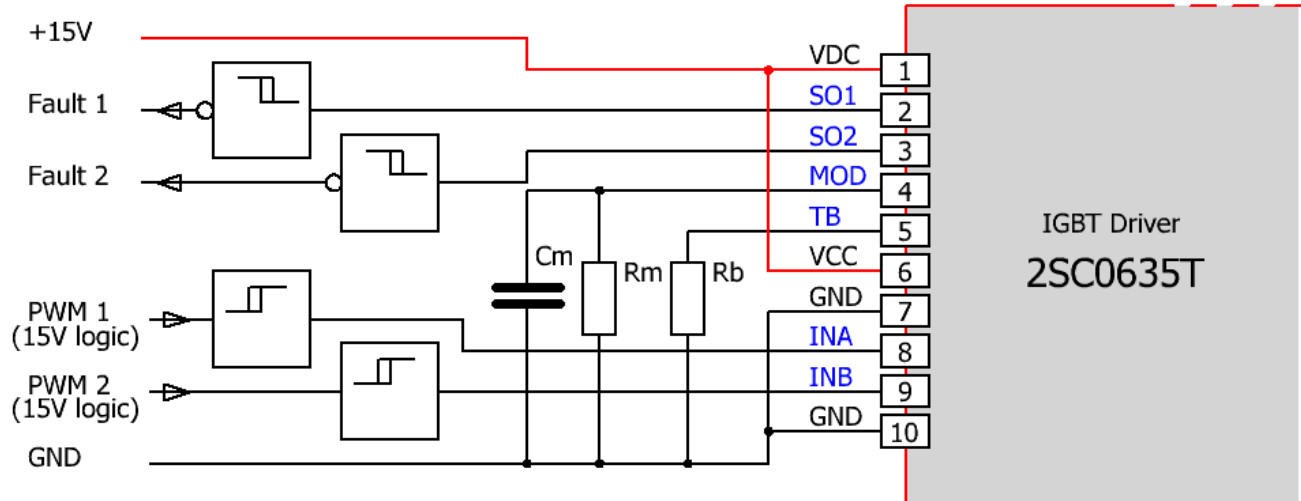
Fig. 5   Recommended user interface of 2SC0635T (primary side)

Both ground pins must be connected together with low parasitic inductance. A common ground plane or wide tracks are strongly recommended. The connecting distance between ground pins must be kept at a minimum.

Description of Primary-Side Interface

General

The primary-side interface of the driver 2SC0635T is very simple and easy to use.

The driver primary side is equipped with a 10-pin interface connector with the following terminals:

- 2 x power-supply terminals
- 2 x drive signal inputs
- 2 x status outputs (fault returns)
- 1 x mode selection input (half-bridge mode / direct mode)
- 1 x input to set the blocking time

All inputs and outputs are ESD-protected. Moreover, all digital inputs have Schmitt-trigger characteristics.

VCC terminal

The driver has one VCC terminal on the interface connector to supply the primary-side electronics with 15V.

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VDC terminal

The driver has one VDC terminal on the interface connector to supply the DC-DC converters for the secondary sides.

VDC should be supplied with 15V. It is recommended to connect the VCC and VDC terminals to a common 15V power supply. In this case the driver limits the inrush current at startup and no external current limitation of the voltage source for VDC is needed.

MOD (mode selection)

The MOD input allows the operating mode to be selected with a resistor connected to GND.

Direct mode

If the MOD input is connected to GND, direct mode is selected. In this mode, there is no interdependence between the two channels. Input INA directly influences channel 1 while INB influences channel 2. High level at an input (INA or INB) always results in turn-on of the corresponding IGBT. In a half-bridge topology, this mode should be selected only when the dead times are generated by the control circuitry so that each IGBT receives its own drive signal.

Caution: Synchronous or overlapping timing of both switches of a half-bridge basically shorts the DC link.

Half-bridge mode

If the MOD input is connected to GND with a resistor $72k<R_m<181k$, half-bridge mode is selected. In this mode, the inputs INA and INB have the following functions: INA is the drive signal input while INB acts as the enable input (see Fig. 6). It is recommended to place a capacitor $C_m=22nF$ in parallel to R_m in order to reduce the deviation between the dead times at the rising and falling edges of INA respectively.

When input INB is low level, both channels are blocked. If it goes high, both channels are enabled and follow the signal on the input INA. At the transition of INA from low to high, channel 2 turns off immediately and channel 1 turns on after a dead time T_d.
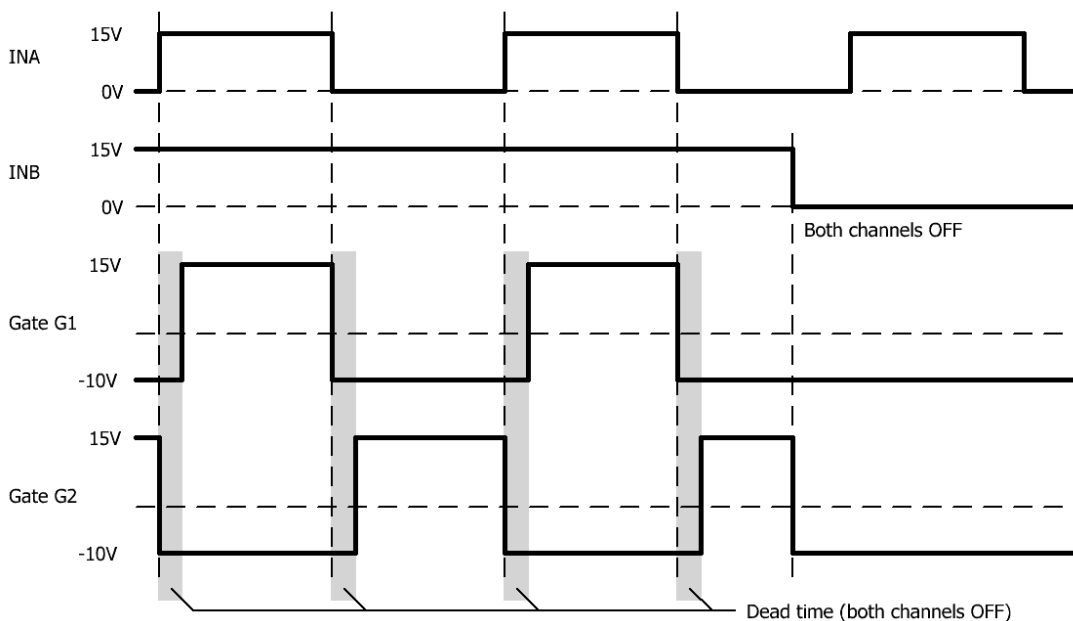

Fig. 6   Signals in half-bridge mode

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The value of the dead time T_d is determined by the value of the resistor R_m according to the following formula (typical value):

$$R_m[k\Omega] = 31.5 \cdot T_d[\mu s] + 52.7 \quad \text{where } 0.6\mu s < T_d < 4.1\mu s \text{ and } 72k\Omega < R_m < 181k\Omega$$

Note that the dead time may vary from sample to sample. A tolerance of approximately ±20% may be expected. If higher timing precisions are required, CONCEPT recommends using the direct mode and generating the dead time externally (refer to the Application Note AN-1101 /4/).

INA, INB (channel drive inputs, e.g. PWM)

INA and INB are basically drive inputs, but their function depends on the MOD input (see above). They safely recognize signals with a logic level of 15V. They have built-in voltage dividers with a total resistance of 4.9kΩ and feature Schmitt-trigger characteristics (refer to the driver data sheet /3/). An input transition is triggered at any edge of an incoming signal at INA or INB.

SO1, SO2 (status outputs)

When no fault condition is detected, an internal pull-up resistor of 10kΩ keeps the output voltage level at VCC. When a fault condition (primary-side supply undervoltage, secondary-side supply undervoltage, IGBT short-circuit or overcurrent) is detected, the corresponding status output SOx goes to low (connected to GND).

The maximum SOx current in a fault condition must not exceed the value specified in the driver data sheet /3/.

Both SOx outputs can be connected together to provide a common fault signal (e.g. for one phase). However, it is recommended to evaluate the status signals individually to allow fast and precise fault diagnosis.

How the status information is processed

a) A fault on the secondary side (detection of short-circuit of IGBT module or supply undervoltage) is transmitted to the corresponding SOx output immediately. The SOx output is automatically reset (returning to VCC) after the blocking time T_b has elapsed (refer to "TB (input for adjusting the blocking time T_b)" for timing information).

b) A supply undervoltage on the primary side is indicated to both SOx outputs at the same time. Both SOx outputs are automatically reset (returning to VCC) when the undervoltage on the primary side disappears.

TB (input for adjusting the blocking time T_b)

The terminal TB allows the factory-set blocking time to be reduced by connecting an external resistor to GND (see Fig. 5). The following equation calculates the value of R_b connected between pins TB and GND in order to define the desired blocking time T_b (typical value):

$$R_b[k\Omega] = \frac{180 \cdot (T_b[ms] + 51)}{129 - T_b[ms]} \quad \text{where} \quad 20ms < T_b < 129ms \text{ and } R_b > 120k\Omega$$

The blocking time can also be set to a minimum of 9µs (typical value) by selecting $R_b = 0\Omega$.

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If the input TB is left open, the blocking time is set to 130ms (factory-set value).

Note: It is also possible to apply a stabilized voltage at TB. The following equation is used to calculate the voltage V_b between TB and GND in order to program the desired blocking time T_b (typical value):

$$V_b [V] = 0.02 \cdot T_b [ms] + 1.02 \qquad \text{where} \quad 20ms < T_b < 130ms \text{ and } 1.42 < V_b < 3.62V$$

Recommended Interface Circuitry for the Secondary-Side Connectors
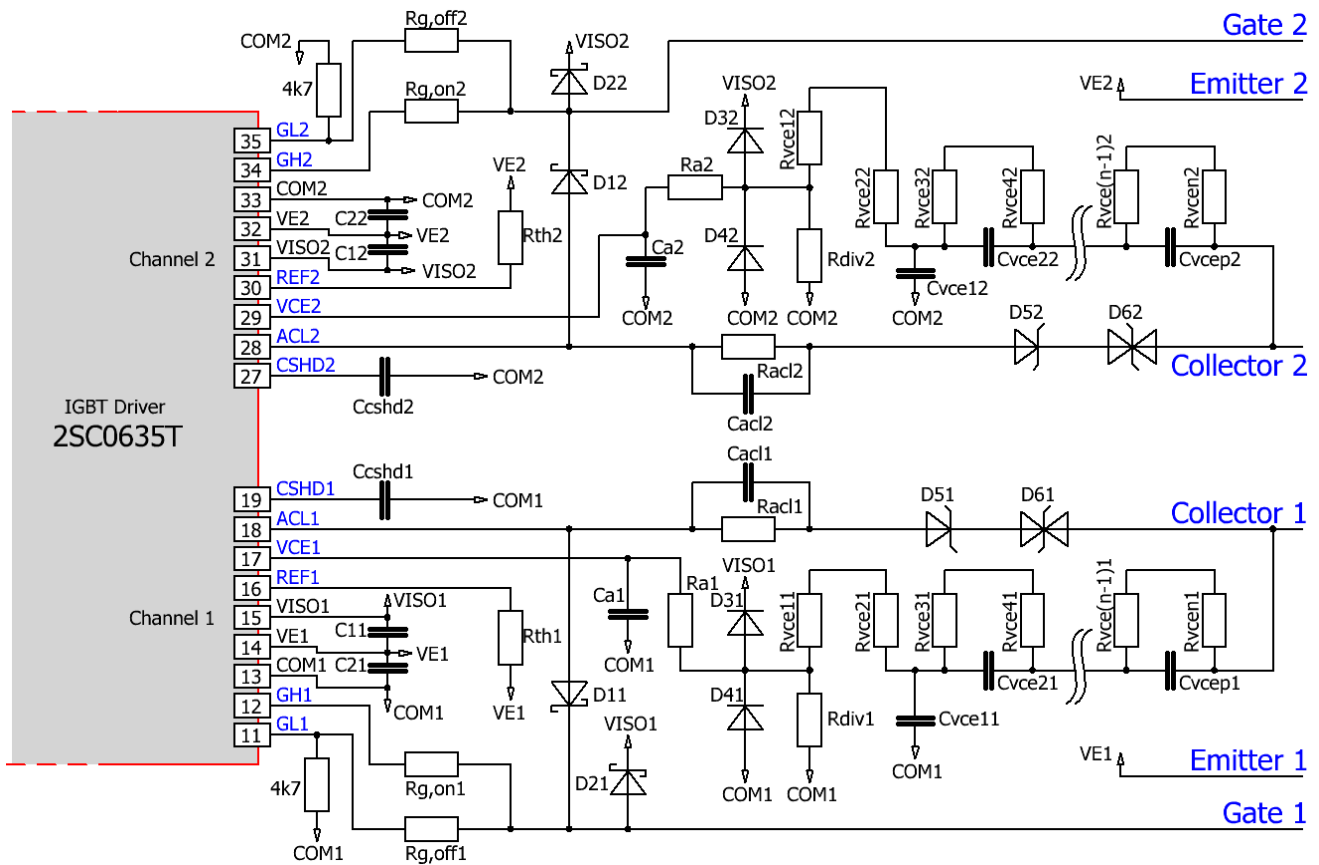
Fig. 7   Recommended user interface of 2SC0635T (secondary sides)

Description of Secondary-Side Interfaces

General

Each driver's secondary side (driver channel) is equipped with a 9-pin interface connector with the following terminals (x stands for the number of the drive channel 1 or 2):

- 1 x DC/DC output terminal VISOx
- 1 x DC/DC output terminal COMx
- 1 x emitter terminal VEx
- 1 x reference terminal REFx for overcurrent or short-circuit protection
- 1 x collector sense terminal VCEx
- 1 x input terminal CSHDx to set the turn-off delay after fault

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- 1 x active clamping terminal ACLx
- 1 x turn-on gate terminals GHx
- 1 x turn-off gate terminals GLx

All inputs and outputs are ESD-protected.

DC/DC output (VISOx), emitter (VEx) and COMx terminals

The driver is equipped with blocking capacitors on the secondary side of the DC/DC converter (for values, refer to the data sheet /3/).

It is recommended to insert an external capacitance of 9.4µF between the VISOx and VEx terminals (C_{1x} in Fig. 7) to drive IGBT modules with a gate charge of up to 4.7µC.

For IGBTs with a higher gate charge, the following additional minimum blocking capacitance values are required for every 1µC gate charge beyond 4.7µC:

- 4µF per 1µC between VISOx and VEx (C_{1x} in Fig. 7) as well as
- 2µF per 1µC between VEx and COMx (C_{2x} in Fig. 7)

It is recommended to use double the overall capacitance value between VISOx and VEx than between VEx and COMx, including that already assembled on the driver.

The blocking capacitors must be connected as closely as possible to the driver's terminal pins with minimum inductance. Ceramic capacitors with a dielectric strength >20V are recommended.

If the capacitance C_{1x} (resp. C_{2x}) exceeds 200µF (resp. 100µF), please contact CONCEPT's support service.

No static load must be applied between VISOx and VEx, or between VEx and COMx. A static load can be applied between VISOx and COMx if necessary.

Reference terminal (REFx)

The reference terminal REFx allows the threshold to be set for short-circuit and/or overcurrent protection with a resistor placed between REFx and VEx. An internal resistor of 62kΩ sets the default threshold value to 9.3V. It can be lowered with the use of an external resistor R_{thx} according to the following equation:

$$R_{thx}[k\Omega] = \frac{62 \cdot V_{thx}[V]}{9.3 - V_{thx}[V]} \qquad \text{where} \qquad V_{thx} < 9.3V$$

It is recommended to keep the reference voltage at its maximum default value of 9.3V (without using an external resistor R_{thx}).

Collector sense (VCEx)

The collector sense must be connected to the IGBT collector with the circuit shown in Fig. 7 in order to detect an IGBT overcurrent or short circuit.

General information and recommendations:

- It is recommended to dimension the overall value of the resistors $R_{totx} = \sum_{i=1}^{n} R_{vceix} = R_{vce\,1x} + ... + R_{vcenx}$ in order for a current of about 0.6...0.8mA to flow through them at the maximum DC-link voltage. This current must not exceed 0.8mA. It is recommended to use series-connected resistors; the minimum creepage and clearance distances required for the

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application must be considered and the maximum voltage, power and temperature rating of the resistors used must not be exceeded. Dimensioning recommendations are given below.

- All resistors R_{vceix} (i ≥ 1) must have the same value.

- R_{divx} allows the static threshold detection level V_{CEthx} to be increased if required (resistive voltage divider with R_{totx}). R_{divx} can be calculated as follows in order to determine the static detection level V_{CEthx}:

$$R_{divx}\,[k\Omega] = R_{totx}\,[k\Omega] \cdot \frac{V_{thx}\,[V] + \left|V_{GLx}\,[V]\right|}{V_{CEthx}\,[V] - V_{thx}\,[V]} \qquad (V_{CEthx} > V_{thx})$$

$|V_{GLx}|$ is the absolute value of the gate-emitter turn-off voltage at the driver output. It depends on the driver load and can be found in the driver data sheet /3/. V_{thx} is the reference value set at the reference terminal REFx as described in the "Reference terminal (REFx)" section.

- The recommended range for the overall capacitance value is $C_{totx} = \dfrac{1}{\displaystyle\sum_{k=1}^{p}\dfrac{1}{C_{vcekx}}} = 1\,pF\,\dots\,4\,pF$.

- All capacitances C_{vcekx} with k≥2 must have the same value.

- The capacitance C_{vce1x} must be chosen such that the following equation is fulfilled:

$$\frac{C_{vce1x}}{C_{totx}} = (0.7\dots0.9) \cdot \frac{R_{totx}}{R_{vce1x} + R_{vce2x}}$$

The maximum voltage rating of the capacitors used must not be exceeded. Dimensioning recommendations are given below.

- The diodes D_{3x} and D_{4x} must have a very low leakage current and a blocking voltage of > 40V (e.g. BAS416). Schottky diodes must be explicitly avoided.

- R_{ax} and C_{ax} are used to set the response time.

Recommended values for 4500V IGBTs with DC-link voltages up to 3200V

- $R_{vce1x}=R_{vce2x}=\dots= R_{vce20x}=220k\Omega$ (500mW, 400V_{peak}, 1%)

- $R_{divx}=620k\Omega$ (0603, 1%)

- $C_{vce1x}=15pF$ (C0G, 1000V, 5%)

- $C_{vce2x}=C_{vce3x}= \dots=C_{vce10x}=22pF$ (C0G, 630V, 5%)

- $C_{ax}=22pF$ (C0G, 50V, 5%)

- $R_{thx}=$not assembled

- $R_{ax}=$see Table 1 below (0603, 1%)

This setup uses 20 resistors R_{vceix} and 10 capacitors C_{vcekx} per channel and leads to a static desaturation detection threshold of about 143V.

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V_{DC}	R_{ax}=75kΩ	R_{ax}=100kΩ	R_{ax}=130kΩ
3200V	5.1µs	6.7µs	8.6µs
2000V	5.1µs	6.8µs	8.7µs
1500V	5.8µs	6.9µs	8.7µs
1000V	8.5µs	8.9µs	9.9µs
800V	12.6µs	12.3µs	12.5µs

Table 1   Typical response time as a function of the resistance R_{ax} and the DC-link voltage V_{DC}

Table 1 gives indicative values only. The response time depends on the specific layout and the IGBT module used. It is therefore recommended to measure the short-circuit duration in the final design.

Note that slow IGBT modules may report a wrong V_{CE} desaturation fault at turn-on. It is therefore recommended to test the setup under worst case conditions (maximum DC-link voltage, maximum collector current and highest IGBT junction temperature). Please also refer to AN-1101 /4/ for more information.

Recommended values for 3300V IGBTs with DC-link voltages up to 2200V

- $R_{vce1x}=R_{vce2x}=…= R_{vce14x}=220$kΩ (500mW, 400$V_{peak}$, 1%)

- $R_{divx}=1.5$MΩ (0603, 1%)

- $C_{vce1x}=15$pF (C0G, 5%, 1000V)

- $C_{vce2x}=C_{vce3x}= …=C_{vce7x}=22$pF (C0G, 630V, 5%)

- $C_{ax}=22$pF (C0G, 50V, 5%)

- $R_{thx}=$not assembled

- $R_{ax}=$see Table 1 below (0603, 1%)

This setup uses 14 resistors R_{vceix} and 7 capacitors C_{vcekx} per channel and leads to a static desaturation detection threshold of about 48V.

V_{DC}	R_{ax}=75kΩ	R_{ax}=100kΩ	R_{ax}=130kΩ
2200V	5.2µs	6.9µs	8.8µs
1500V	5.2µs	6.9µs	8.8µs
1100V	5.3µs	6.9µs	8.8µs
700V	6.6µs	7.5µs	9.1µs
600V	13.7µs	12.8µs	12.6µs

Table 2   Typical response time as a function of the resistance R_{ax} and the DC-link voltage V_{DC}

Table 2 gives indicative values only. The response time depends on the specific layout and the IGBT module used. It is therefore recommended to measure the short-circuit duration in the final design.

Note that slow IGBT modules may report a wrong V_{CE} desaturation fault at turn-on. It is therefore recommended to test the setup under worst case conditions (maximum DC-link voltage, maximum collector current and highest IGBT junction temperature). Please also refer to AN-1101 /4/ for more information.

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Input for adjusting the turn-off delay in fault condition (CSHDx)

The terminal CSHDx allows the delay in turning off the IGBT after a fault detection on the driver's secondary side (short-circuit, undervoltage) to be determined with a capacitor (C0G/50V) connected to COMx. Table 3 shows the resulting delay as a function of the circuit used at pin CSHDx.

Circuit at pin CSHDx	Typical turn-off delay
Left open	0.2µs
Capacitor between CSHDx and COMx	Turn-off delay [µs]= C[pF]/50 e.g: 2µs time delay for 100pF
CSHDx connected to COMx (short circuit)	The driver does not turn off automatically.

Table 3 Turn-off delay as a function of CSHDx wiring

As soon as the fault turn-off delay time has elapsed, the driver's channel is automatically turned off.

The driver's channel can also be turned off from the driver's primary side within the turn-off delay time determined by the CSHDx pin after a secondary-side fault detection. However, the following restrictions apply: they may be relevant, especially for multilevel applications:

- The driver's channel cannot be turned off from the primary side during the blocking time T_b.

- A first turn-off command (see first red arrow in Fig. 8) must be followed by a turn-on command (see second red arrow in Fig. 8 which must be applied after the blocking time has elapsed), before the driver's channel can be turned off. The driver's channel will only be turned off after the second turn-off command, as shown in Fig. 8.

Note that the driver's channel is blocked during 9µs after the turn-off event following a secondary-side fault. After this time (and the end of the driver's blocking time T_b), the driver's channel(s) can be turned on again. Both driver channels work fully independently.
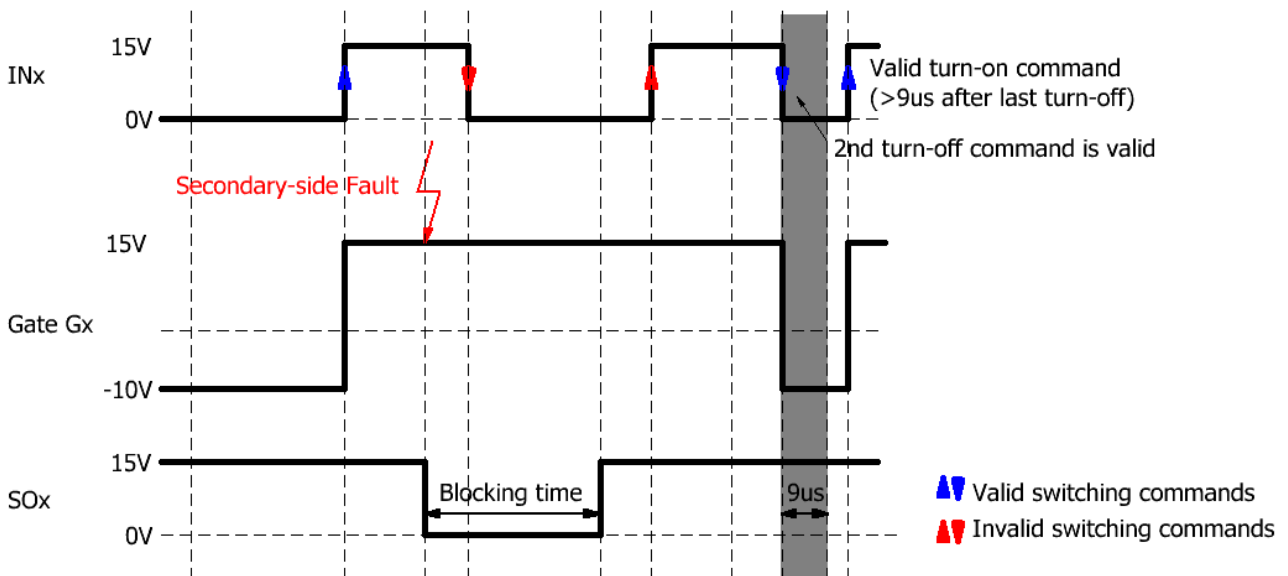

Fig. 8 Example of turn-off behavior after secondary-side fault detection (CSHDx connected to COMx)

Note that it will not be possible to turn the IGBT on during about 100ns per 100pF capacitance applied to CSHDx after a fault condition, starting from the turn-off event of the IGBT (minimum off-time required).

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Active clamping (ACLx)

Active clamping is a technique designed to partially turn on the power semiconductor as soon as the collector-emitter voltage exceeds a predefined threshold. The power semiconductor is then kept in linear operation.

Basic active clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor devices (TVS) to the IGBT gate. The 2SC0635T supports CONCEPT's Advanced Active Clamping, where the feedback is also provided to the driver's secondary side at pin ACLx (see Fig. 7): as soon as the voltage at pin ACLx exceeds about 1.3V, the turn-off MOSFET is progressively switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS. The turn-off MOSFET is completely off when the voltage at pin ACLx approaches 20V (measured to COMx).

It is recommended to use the circuit shown in Fig. 7. The following parameters must be adapted to the application:

- TVS D_{5x}, D_{6x}: it is recommended to use:

  - 3300V IGBTs with DC-link voltages up to 2200V: Seven unidirectional 300V TVS and one bidirectional 350V TVS. Good clamping results can be obtained with seven unidirectional TVS P6SMB300A and one bidirectional TVS P6SMB350CA from Diotec.

  - 4500V IGBTs with DC-link voltages up to 3200V: Eight unidirectional 400V TVS and one bidirectional 350V TVS. Good clamping results can be obtained with eight unidirectional TVS P6SMB400A and one bidirectional TVS P6SMB350CA from Diotec.

  At least one bidirectional TVS (D_{6x}) per channel (≥300V for 3300V IGBTs and ≥400V for 4500V IGBTs) must be used in order to avoid negative current flowing through the TVS chain during turn-on of the antiparallel diode of the IGBT module due to its forward recovery behavior. Such a current could, depending on the application, lead to undervoltage of the driver secondary voltage VISOx to VEx (15V).

  Note that it is possible to modify the number of TVS in a chain. The active clamping efficiency can be improved by increasing the number of TVS used in a chain if the total breakdown voltage remains at the same value. Note also that the active clamping efficiency is highly dependent on the type of TVS used (e.g. manufacturer).

- R_{aclx} and C_{aclx}: These parameters allow the effectiveness of the active clamping as well as the losses in the TVS and the IGBT to be optimized. It is recommended to determine the value with measurements in the application. Typical values are: R_{aclx}=0…150Ω and R_{aclx}*C_{aclx}=100ns…500ns. R_{aclx}=0Ω is recommended to improve the effectiveness of active clamping (usually recommended).

- D_{1x} and D_{2x}: it is recommended to use Schottky diodes with blocking voltages >35V (>1A depending on the application).

  Please note that the diodes D_{1x} and D_{2x} must not be omitted if Advanced Active Clamping is used. If active clamping is not used, the diodes D_{1x} can be omitted. The pin ACLx must then be left open.

Gate turn-on (GHx) and turn-off (GLx) terminals

These terminals allow the turn-on (GHx) and turn-off (GLx) gate resistors to be connected to the gate of the power semiconductor. The GHx and GLx pins are available as separated terminals in order to set the turn-on and turn-off resistors independently without the use of an additional diode. Please refer to the driver data sheet /3/ for the limit values of the gate resistors used.

A resistor between GLx and COMx of 4.7kΩ (other values are also possible) may be used in order to provide a low-impedance path from the IGBT gate to the emitter/source even if the driver is not supplied with power. No static load (e.g. resistors) must be placed between GLx and the emitter terminal VEx.

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Note however that it is not advisable to operate the power semiconductors within a half-bridge with a driver in the event of a low supply voltage. Otherwise, a high rate of increase of V_{CE} may cause partial turn-on of these IGBTs.

How Do 2SC0635T SCALE-2 Drivers Work in Detail?

Power supply and electrical isolation

The driver is equipped with a DC/DC converter to provide an electrically insulated power supply to the gate driver circuitry. All transformers (DC/DC and signal transformers) feature basic isolation to IEC 61800-5-1 and IEC 60664-1 between primary side and either secondary side as well as between both secondary sides.

Note that the driver requires a stabilized supply voltage.

Power-supply monitoring

The driver's primary side as well as both secondary-side driver channels are equipped with a local undervoltage monitoring circuit.

In the event of a primary-side supply undervoltage, the power semiconductors are driven with a negative gate voltage to keep them in the off-state (the driver is blocked) and the fault is transmitted to both outputs SO1 and SO2 until the fault disappears.

In case of a secondary-side supply undervoltage, the corresponding power semiconductor is driven with a negative gate voltage after the delay in IGBT turn-off (refer to "Input for adjusting the turn-off delay in fault condition (CSHDx)") and a fault condition is transmitted to the corresponding SOx output. The SOx output is automatically reset (returning to VCC) after the blocking time.

IGBT and MOSFET operation mode

The driver features two operation modes:

- The first mode is the default IGBT setup with both a positive (regulated) turn-on voltage of 15V (typical value) and a second (non-regulated) turn-off voltage (see Fig. 7).

- The second mode has been specifically designed for ultra-fast MOSFET switching. It incorporates a single turn-on voltage only. The turn-off voltage is set to 0V. This MOSFET mode is activated by connecting the secondary-side terminals COMx and VEx. If 2SC0635T drivers are to be used in the MOSFET mode, please refer to the Application Note AN-1101 /4/. Note that the secondary supply voltage applied between VISOx and VEx must be higher than 10V when using 2SC0635T in the MOSFET operation mode.

V_{CE} monitoring / short-circuit protection

Each channel of the 2SC0635T driver is equipped with a V_{CE} monitoring circuit. The recommended external circuitry is shown in Fig. 7. The resistor R_{thx} can be used to define the static turn-off threshold together with R_{vceix} and R_{divx}. It is recommended to choose threshold levels of about 50V for 3300V IGBTs or 140V for 4500V IGBTs. In this case, the driver will safely protect the IGBT against short circuit, but not necessarily against overcurrent. Overcurrent protection has a lower timing priority and it is recommended to implement it within the host controller.

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During the response time, the V_{CE} monitoring circuit is inactive. The response time is the time that elapses after turn-on of the power semiconductor until the collector voltage is measured (see Fig. 9).
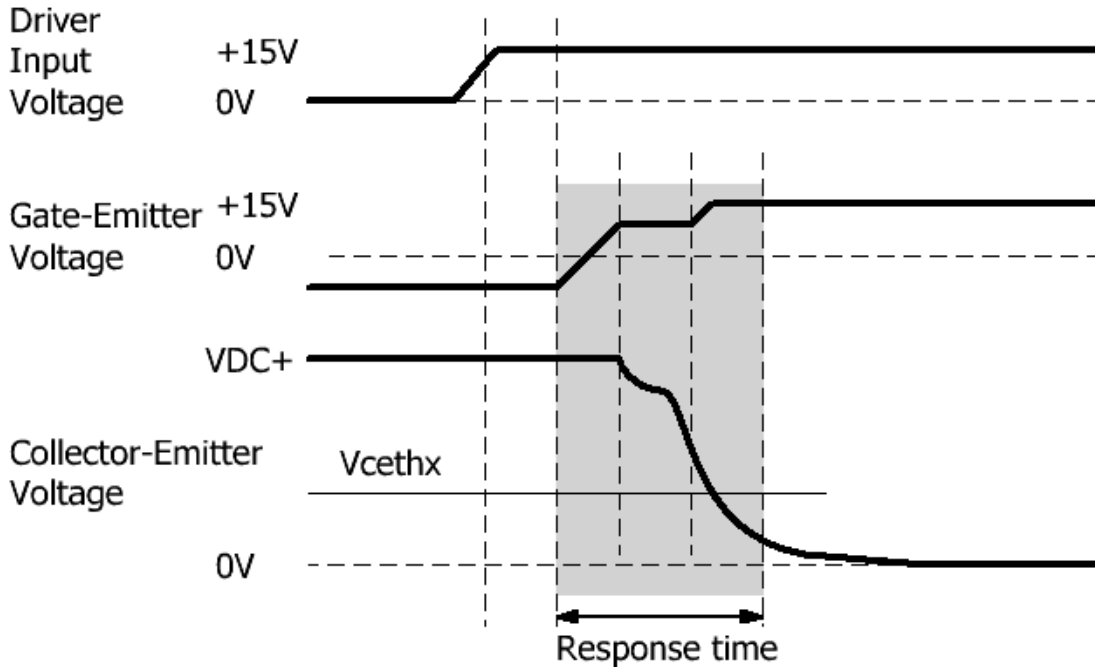

Fig. 9   Turn-on characteristic of an IGBT

Both IGBT collector-emitter voltages are measured individually. V_{CE} is checked after the response time at turn-on to detect a short circuit or overcurrent. If the measured V_{CE} at the end of the response time is higher than the threshold V_{CEthx}, the driver detects a short circuit or overcurrent. The fault status is immediately transferred to the corresponding SOx output of the affected channel. After the fault turn-off delay time has elapsed, the driver turns the corresponding power semiconductor off. The power semiconductor is kept in the off state (non-conducting) and the fault is shown at pin SOx as long as the blocking time T_b is active.

The blocking time T_b is applied independently to each channel. T_b starts as soon as V_{CE} exceeds the threshold of the V_{CE} monitoring circuit outside the response time span.

Desaturation protection with sense diodes

Desaturation protection with sense diodes is not recommended for IGBT voltage classes of 3300V and 4500V with 2SC0635T.

Parallel connection of 2SC0635T

If parallel connection of 2SC0635T drivers is required, please refer to the Application Note AN-0904 /5/.

3-level or multilevel topologies

In applications with multi-level topologies, the turn-off sequence of the individual power semiconductors usually needs to be controlled by the host controller in case of a detected fault condition (e.g. short-circuit, over-current). This is especially true if no Advanced Active Clamping or Dynamic Advanced Active Clamping scheme is implemented.

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In that case, the turn-off delay in the fault condition of the different driver's channels can be adjusted to match the corresponding timing specifications. It is in particular possible to determine a specific turn-off delay for the inner IGBTs of a 3-level NPC topology as described in the section: "Input for adjusting the turn-off delay in fault condition (CSHDx)". The driver's response time can also be adapted accordingly if required.

Note however that Advanced Active Clamping offers simple and safe protection that allows excessive collector-emitter overvoltages to be avoided in case of wrong commutation sequences in the short-circuit condition of 3-level converter topologies (refer to /6/ and /7/ for more information).

Bibliography

/1/   Paper: Smart Power Chip Tuning, Bodo's Power Systems, May 2007

/2/   "Description and Application Manual for SCALE™ Drivers", CONCEPT

/3/   Data sheet SCALE™-2 driver core 2SC0635T, CONCEPT

/4/   Application Note AN-1101: Application with SCALE™-2 Gate Driver Cores, CONCEPT

/5/   Application Note AN-0904: Direct Paralleling of SCALE™-2 Gate Driver Cores, CONCEPT

/6/   Application Note AN-0901: Methodology for Controlling Multi-Level Converter Topologies with SCALE™-2 IGBT Drivers, CONCEPT

/7/   Paper: Safe Driving of Multi-Level Converters Using Sophisticated Gate Driver Technology, PCIM Asia, June 2013

Note: The Application Notes are available on the Internet at www.igbt-driver.com/go/app-note and the papers at www.IGBT-Driver.com/go/paper

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The Information Source: SCALE-2 Driver Data Sheets

CONCEPT offers the widest selection of gate drivers for power MOSFETs and IGBTs for almost any application requirements. The largest website on gate-drive circuitry anywhere contains all data sheets, application notes and manuals, technical information and support sections: www.IGBT-Driver.com

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CONCEPT has more than 25 years experience in the development and manufacture of intelligent gate drivers for power MOSFETs and IGBTs and has already implemented a large number of customized solutions.

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Ordering Information

The general terms and conditions of delivery of CT-Concept Technologie GmbH apply.

Type Designation	Description
2SC0635T2A0-45	Dual-channel SCALE-2 driver core

Product home page: www.IGBT-Driver.com/go/2SC0635T

Refer to www.IGBT-Driver.com/go/nomenclature for information on driver nomenclature

Information about Other Products

For other driver cores:

Direct link: www.IGBT-Driver.com/go/cores

For other drivers, product documentation, evaluation systems and application support

Please click onto: www.IGBT-Driver.com

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